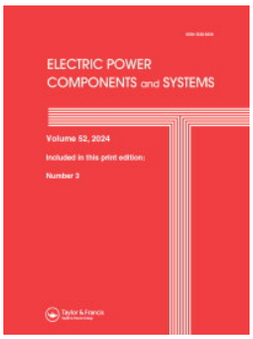


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# Hybrid-Clamping SVPWM Scheme for a Four-Level Open-End Winding Induction Motor Drive

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CONTENTS



**Abstract**—An open-end winding arrangement is fed with two typical 2-level voltage source inverters (VSIs) on either side to accomplish multilevel inversion. Two voltage source modules (VSIs) DC-link voltages are kept at a 2:1 ratio to realize the open-end winding induction motor (OEW-IM) power circuit's four-level configuration. However, the higher DC-link voltage capacitor overcharges its lower DC-link voltage counterpart in the 4-level power circuit configuration. This article proposes a new hybrid-clamping space vector PWM (SVPWM) approach to prevent overcharging. Based on the sample moment, the suggested SVPWM technique clamps one inverter and switches to another inverter. Additionally, it clamps one of the inverter's switching phases. The proposed PWM method has been found to reduce switching power loss in contrast to earlier SVPWM methods. The proposed SVPWM scheme for the 4-level OEW-IM drive is tested and verified using an experimental laboratory setup.

Keywords: induction motor, open-end winding, overcharging, SVPWM
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## 1. INTRODUCTION

Multilevel inverters (MLIs) have been used in medium-voltage and high-power industrial applications. Several MLI topologies have been presented in the literature, with neutral-point-clamped, flying-capacitor (FC), and cascaded converter topologies being the most frequently employed. Low $dv/dt$, an improved harmonic profile, and lower switch-blocking voltage are the primary advantages of MLIs [1].

Due to its simplicity and fault tolerance, the dual-inverter configuration has recently gained popularity among cascaded converters [2]. The dual-inverter configuration uses two 2-level VSIs to achieve the multilevel output. The topology does not have neutral-point voltage fluctuations like in the diode-clamped converter. It uses fewer capacitors and DC sources than flying capacitors and cascaded converters. The dual-inverter configuration is more reliable

because if anyone inverter fails to operate, the second inverter is used to run the load at a reduced power level [3].

The dual-inverter-fed OEW-IM has potential application in more electric craft, electric vehicles, renewable energy systems, and other industrial applications of induction

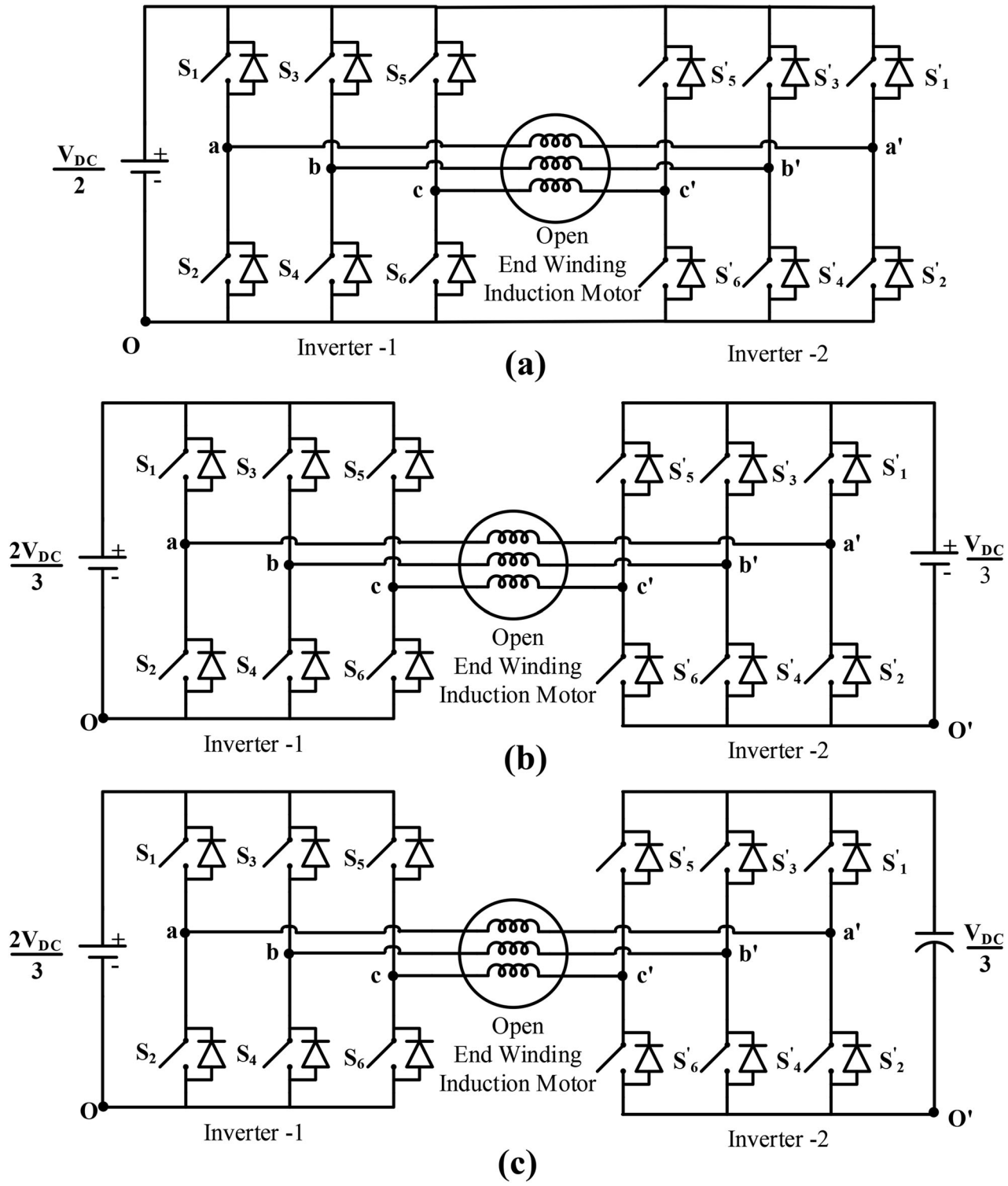


**FIGURE 1.** Dual-inverter-fed OEW-IM circuit configurations.

motor drive [4–6]. Three different power source arrangements proposed in the literature for the dual-inverter-fed OEW-IM are shown in Figure 1. The power circuit configurations of OEW-IM have either common DC-links (Figure 1(a)), isolated DC-links (Figure 1(b)), or DC-links with flying capacitors (Figure 1(c)) [7–9].

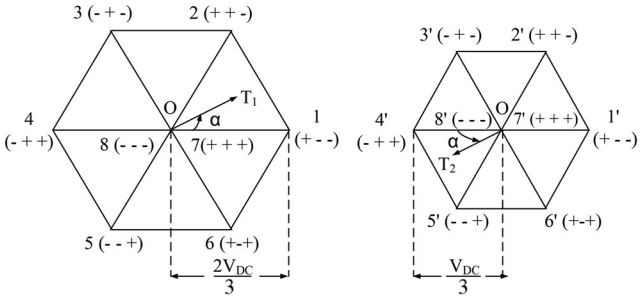


**FIGURE 2.** Space-vector diagrams of Inverter-1 (left) & Inverter-2 (right).

Figure 1(a) lets zero-sequence currents (ZSCs) flow in the stator winding of the motor and does a 3-level multi-level inversion. Either by changing the way the circuit is setup [10] or by using SVPWM techniques [7], the ZSCs can be suppressed. However, the circuit configuration calls for more devices to be added [10], the SVPWM technique loses its advantage (a 15% boost in DC-link voltage) [7], and more ripple in the motor phase current.

By isolating the power sources, Figure 1(b) configuration prevents the flow of zero-sequence currents. To achieve the four-level inversion, the voltage ratio of the

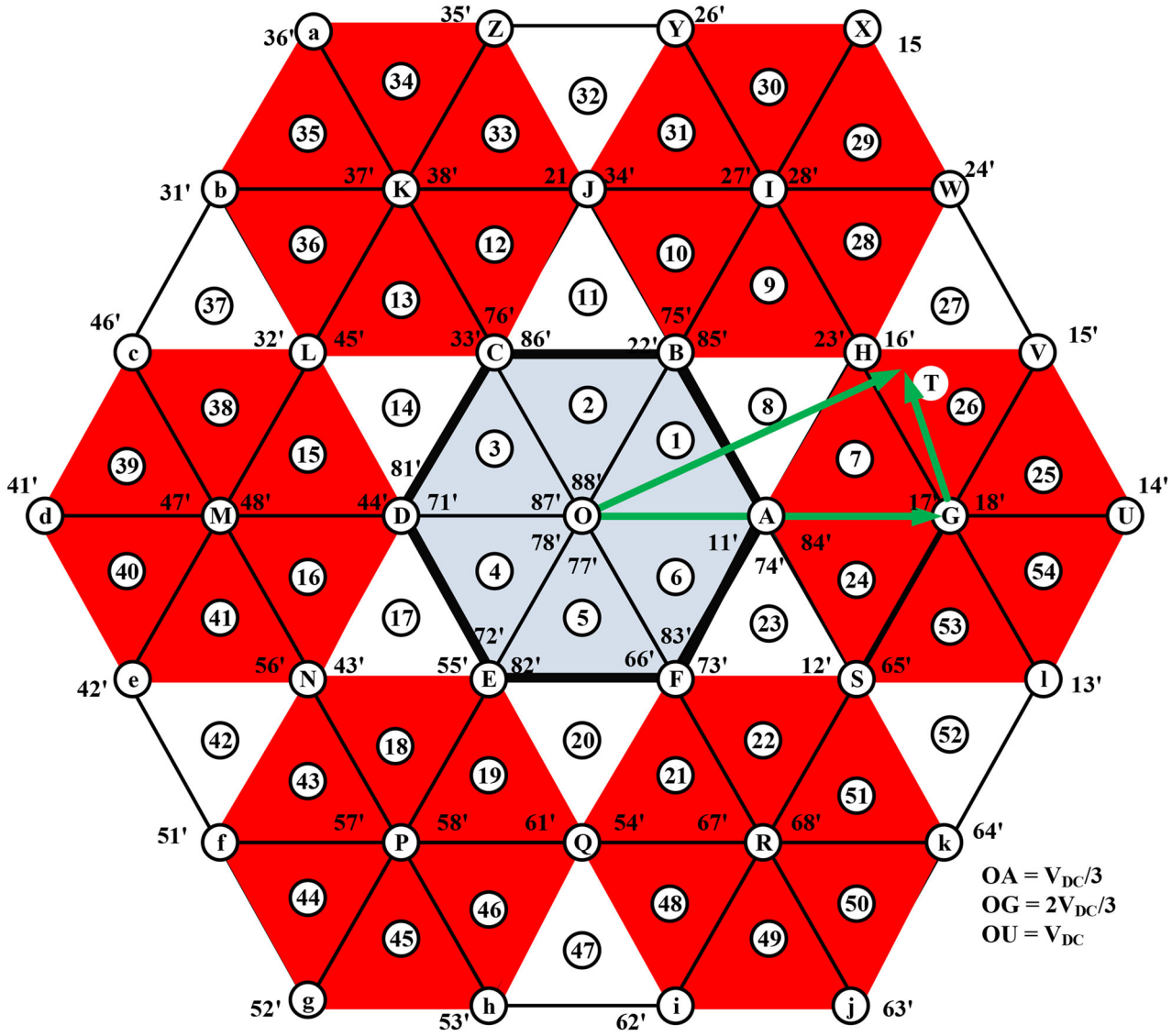


**FIGURE 3.** 4-level OEW-IM space vector diagram.

individual power supply is maintained at 2:1. A biased SVPWM [11] is suggested in the literature to reduce the motor phase current ripple. However, in some switching vector combinations, the higher DC-link voltage capacitor (HDC-LVC) overcharges its counterpart lower DC-link voltage capacitor (LDC-LVC).

The overcharging of the LDC-LVC (capacitor having a DC-link voltage of $V_{DC}/3$) can be evaded by employing decoupled SVPWM methods [11]. Decoupled SVPWM schemes can switch both inverters; however, this comes at the expense of increased switching power loss (SPL). In the literature, phase-clamped SVPWM approaches [12–14] are also mentioned to lower the SPL of a dual-inverter system with an OEW-IM drive.

A method to avoid overcharging new topologies with asymmetric power supplies is also proposed in the Ref. [15, 16]. However, the topology described in Ref. [15] provides a path for zero-sequence current to circulate. The topology [16] is suitable only for 6n-pole induction motor drives.

The circuit configuration shown in Figure 1(c) uses the FC and is charged using the inverter-1. However, the OEW-IM drive's efficiency decreases since the FC is charged *via* the motor's phase windings [17].

After reviewing the relevant literature, it is clear that none of those mentioned earlier methods for reducing the current ripple in a four-level OEW-IM drive is optimal. The approach described in Ref. [14] develops hybrid SVPWM techniques by combining decoupled SVPWM with biased SVPWM. The hybrid SVPWM method switches all phases in the switching inverter using the center-spaced SVPWM method.

This article introduces the phase-clamped SVPWM technique to reduce the SPL further and improve the performance of the SVPWM techniques proposed in Ref. [14]. The phase clamping and the arrangement of the circuit configuration in Figure 1(b) create asymmetry. The proposed SVPWM technique is used to make waveform symmetry possible, even though the power circuit and PWM technique are not symmetrical.

The proposed SVPWM method is tested with the experimental setup and simulated with MATLAB/SIMULINK software. By considering Total Harmonic Distortion (THD), weighted THD (WTHD), switching power loss (SPL), conduction power loss (CPL), total dual inverter loss (TDIL), and the torque-ripple as performance indices, its performance is compared to that of the existing SVPWM techniques. The following section explains the four-level (4-L) OEW-IM.

## 2. 4-LEVEL OPEN-END WINDING INDUCTION MOTOR

The four-level OEW-IM power circuit feeds two 2-level VSIs on both sides of an IM, either by removing the star neutral point or the delta end-connections while maintaining a 2:1 DC-link voltage ratio, as illustrated in Figure 1(b). It is called a dual-inverter system because it has two 2-level VSIs. Each inverter has eight switching vectors, as shown in Figure 2. Figure 3 shows the dual-inverter-fed OEW- IM vector diagram with 64 switching vector possibilities in 37 locations.

The inverter-1 toggles between $+V_{DC}/3$ and $-V_{DC}/3$, whereas the inverter-2 switches between $+V_{DC}/6$ and $-V_{DC}/6$. Table 1 displays the resulting voltage levels between the OEW-IM phases. It can be shown in Table 1 that OEW-IM can accomplish four levels throughout the motor phase winding when using a power supply with a 2:1 ratio.

| **Pole voltage of inverter-1** $(v_{ao})$ | **Pole voltage of inverter-2** $(v_{a'o'})$ | **Phase voltage of OEW-IM** $(v_{aa'} = v_{ao} - v_{a'o'})$ |
|---|---|---|
| $+V_{DC}/3$ | $+V_{DC}/6$ | $+V_{DC}/6$ |
| $+V_{DC}/3$ | $-V_{DC}/6$ | $+V_{DC}/2$ |
| $-V_{DC}/3$ | $+V_{DC}/6$ | $-V_{DC}/2$ |
| $-V_{DC}/3$ | $-V_{DC}/6$ | $-V_{DC}/6$ |

**TABLE 1.** Voltage levels across the OEW-IM.

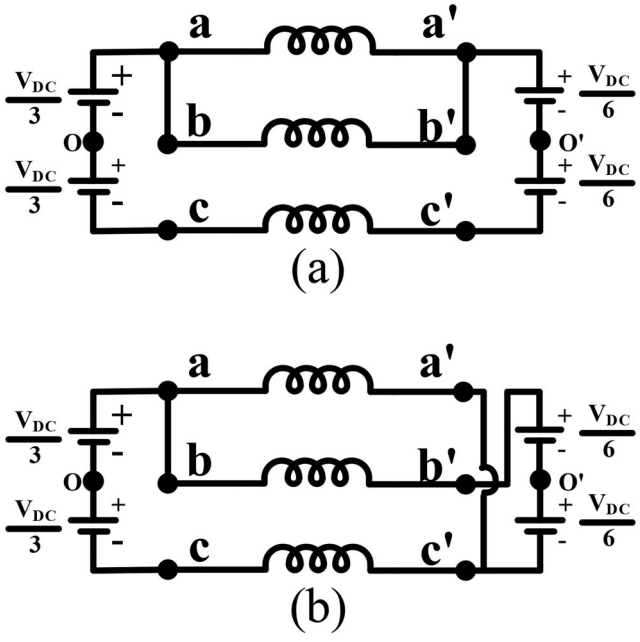


**FIGURE 4.** OEW-IM equivalent circuit diagram for switching vector combination (a) 22' and (b) 23'.

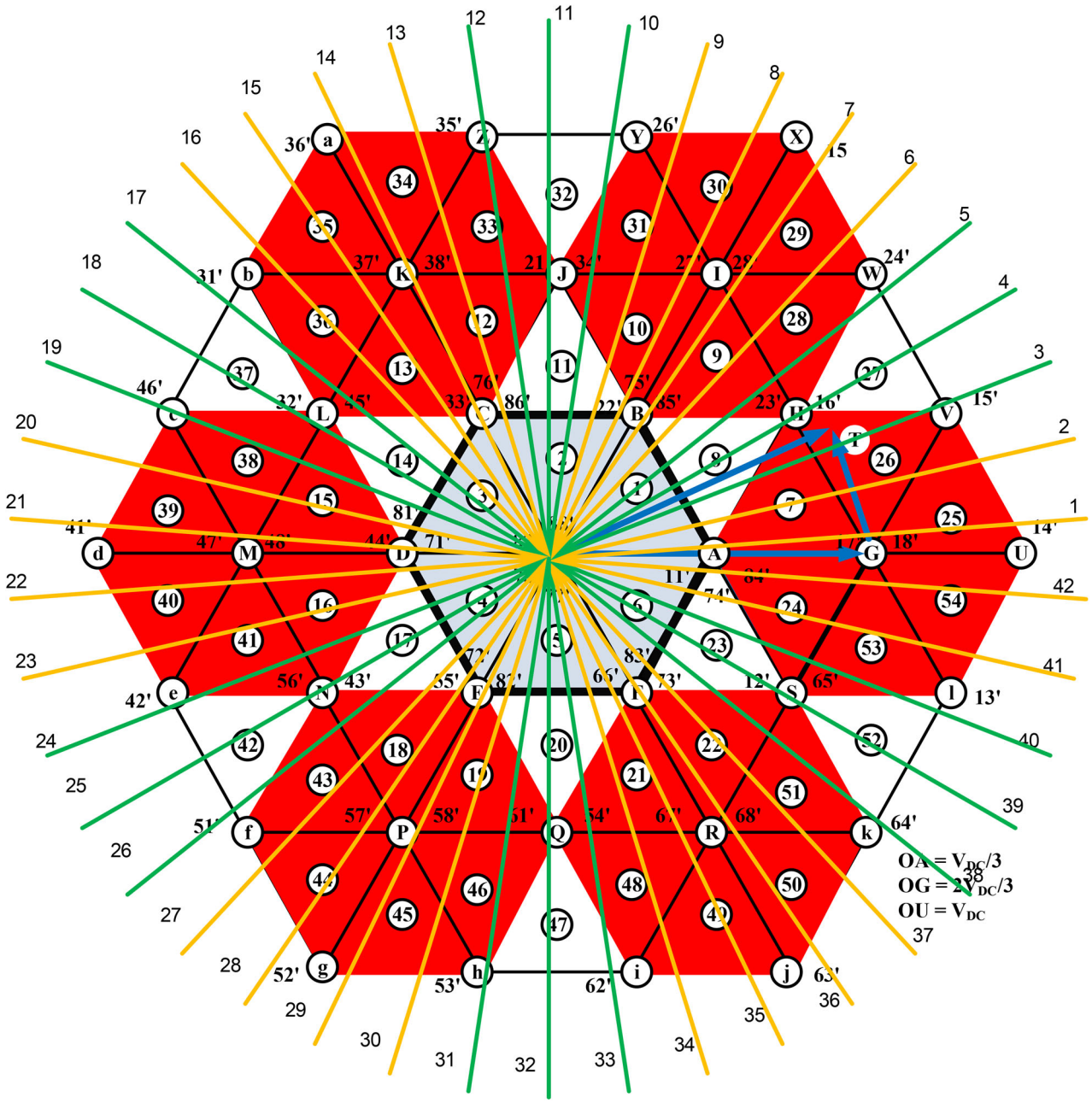


**FIGURE 5.** Principle of operation of proposed SVPWM technique.

As said earlier, in some switching vector combinations, the LDC-LVC sees the HDC-LVC directly [11], which causes the LDC-LVC to be overcharged. The troublesome combinations of switching vectors are (see Figure 3) 11, 22, 33, 44, 55, and 66. The switching vector combinations at H, J, L, N, Q, and S also result in the LDC-LVC being overcharged by its opposite when the motor is loaded. Figures 4(a) and 4(b) show the OEW-IM equivalent circuit diagrams for the switching vector combinations 22′ and 23′.

It is evident from Figure 4 that, for the switching vector combinations stated above, the counterpart capacitor over-charges the lower DC-link voltage capacitor. The following section describes how to use the proposed SVPWM technique to eliminate the charging combinations mentioned above.

## 3. PROPOSED SPACE VECTOR PWM STRATEGY

The modulating waveforms for the dual-inverter system are produced using the reference voltage vector

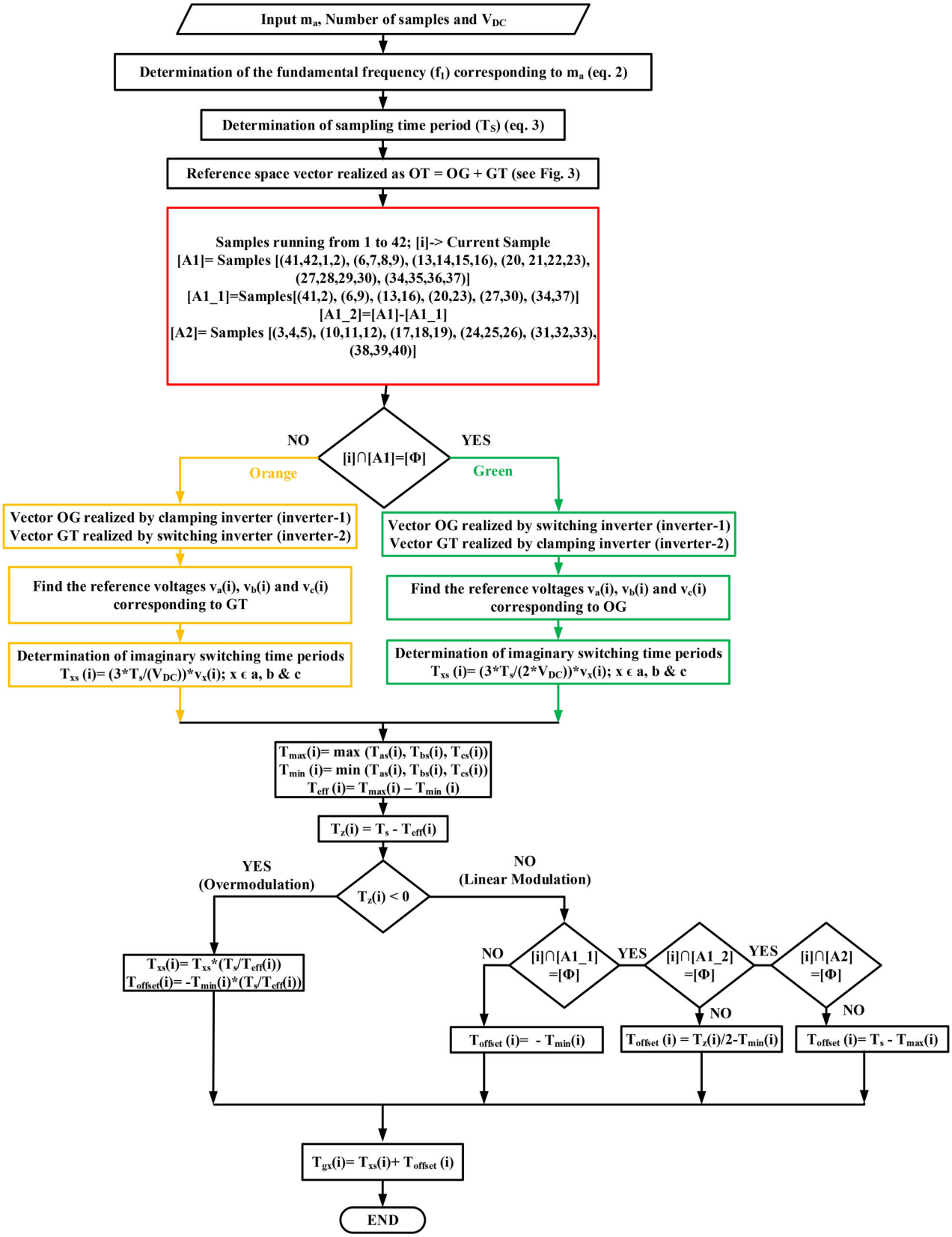


**FIGURE 6.** Flowchart of proposed SVPWM strategy.

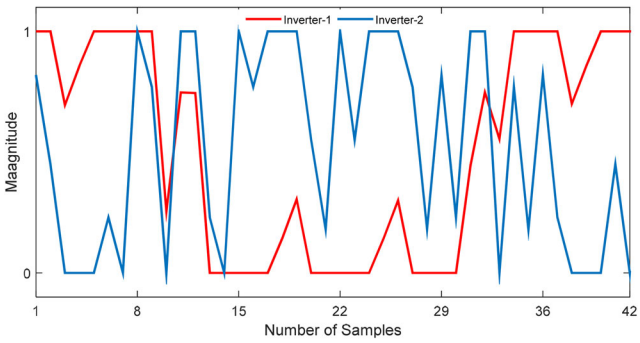


**FIGURE 7.** Modulating the waveforms of the proposed SVPWM technique.

($\overline{\mathbf{OT}}$) illustrated in Figure 3. The length of the voltage vector is determined by the modulation index ($\boldsymbol{m_a}$). According to Eq. (1), the modulation index ($\boldsymbol{m_a}$) is defined.

$$m_a = \frac{|\mathrm{OT}|}{OU} \tag{1}$$

where **OU** = DC link voltage of the dual-inverter setup.

The modulation index decides the operating frequency ($\boldsymbol{f}$) of the OEW-IM drive and controls the output voltage of the dual-inverter system. The limit of the linear modulation index at the rated supply conditions (i.e., voltage and frequency) of the OEW-IM is $\sqrt{3}/2$. The

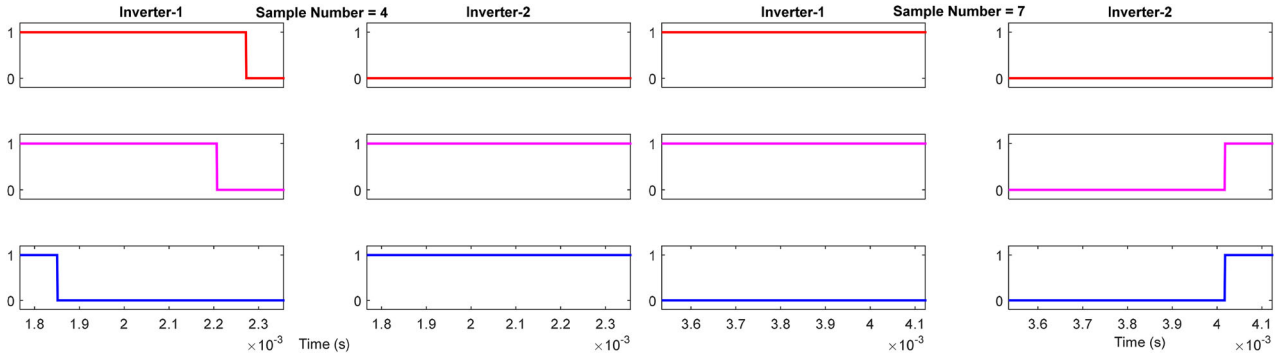


**FIGURE 8.** Pole voltages at sample numbers 4 (left) and 7 (right).

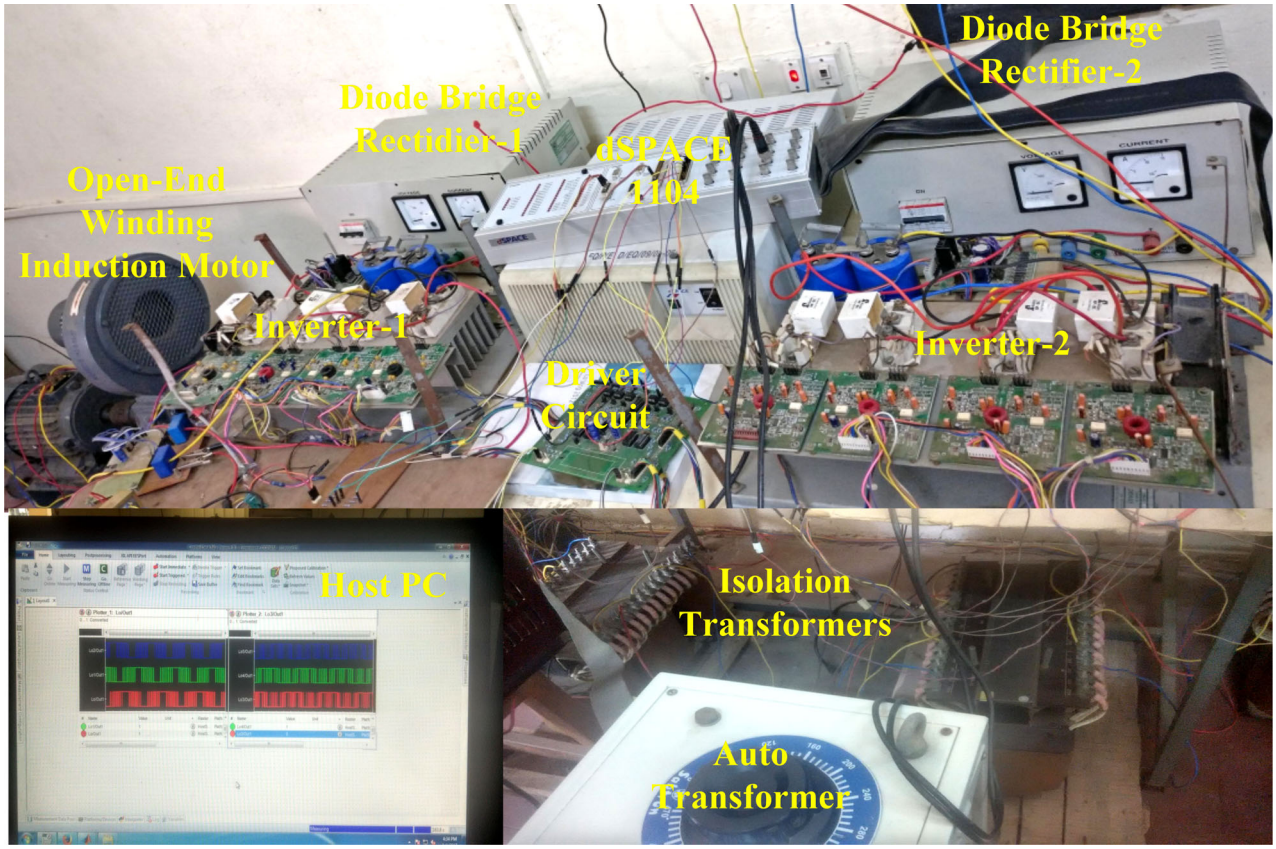


**FIGURE 9.** A view of the experimental setup of a 4-level OEW-IM.

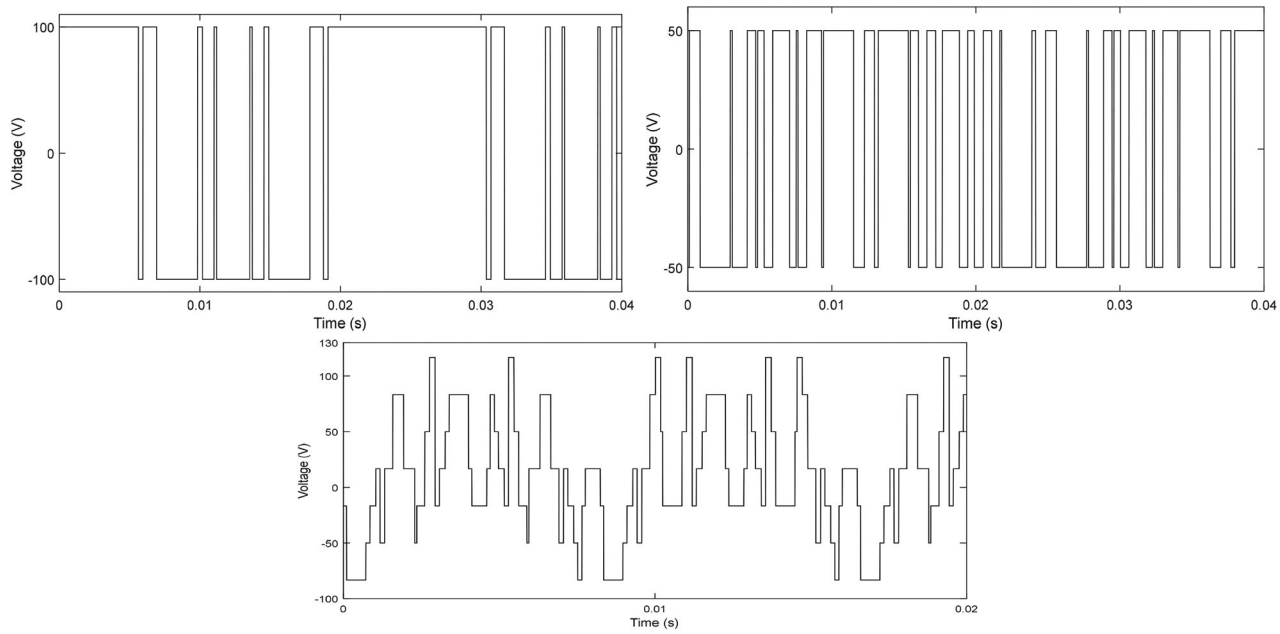


**FIGURE 10.** Pole voltage of inverter-1 (top), inverter-2 (middle) and common mode voltage (bottom) of OEW-IM drive at $m_a = 0.7$.

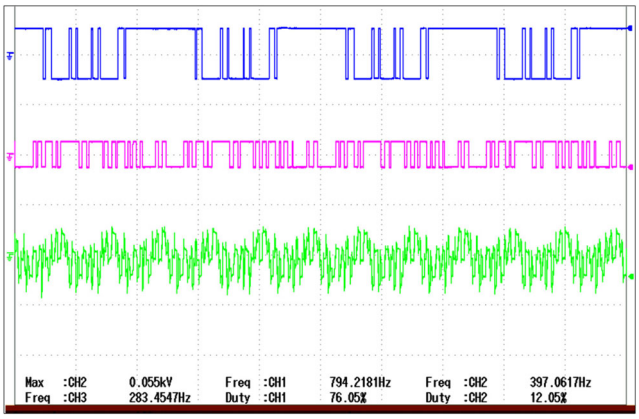


**FIGURE 11.** Experimental pole-voltage of inverter-1 (top), inverter-2 (middle) and common mode voltage (bottom) of OEW-IM drive at $m_a = 0.7$.

operating frequency of the OEW-IM can be calculated as follows:

$$f = \frac{m_a \times 50}{\sqrt{3}/2} \tag{2}$$

To obtain the waveform symmetries, the voltage vector is sampled 42 times every cycle [11]. The dual-inverter system's sampling period ($T_s$) is given as,

$$T_s = \frac{1}{f \times 42} \tag{3}$$

The $\overline{\mathbf{OT}}$ is the vector addition of the voltage vectors **OG** and **GT** (Figure 3). One inverter must be clamped, and the second inverter must be switched around the offset of the clamped inverter to produce the least current ripple, reduce SPL, and optimize the harmonic profile of OEW-IM phase voltage.

The ideal situation is achieved by clamping inverter-1 (i.e., the inverter with an HDC-LV) and switching inverter-2. Hence, the **OG** and **GT** voltage vectors are respectively realized by inverter-1 and inverter-2.

However, if inverter-1 is clamped, as indicated in Ref. [11] for specific combinations of space vectors, the LDC-LVC is overcharged by the HDC-LVC. Additionally, not all space vector combinations are achieved (see Figure 3, white shaded area).

The vector **OT** in the white-shaded area is realized by: (i) switching the two inverters or (ii) switching the inverter-1 around the clamped inverter-2. However, because both inverters are switching in the former case, SPL is more significant than in the latter PWM [14].

As said earlier, the entire space vector diagram was sampled 42 times over a cycle. The space vector diagram corresponding to these 42 samples can be obtained, as shown in Figure 5. The 42 samples are colored either green or orange. The green-colored samples cover the white-shaded area where inverter-1 is switched around the clamped inverter-2 to avoid overcharging the lower DC-link voltage capacitor. The orange-colored samples cover the remaining space vector locations, where inverter-2 switched around the clamped inverter-1 [14].

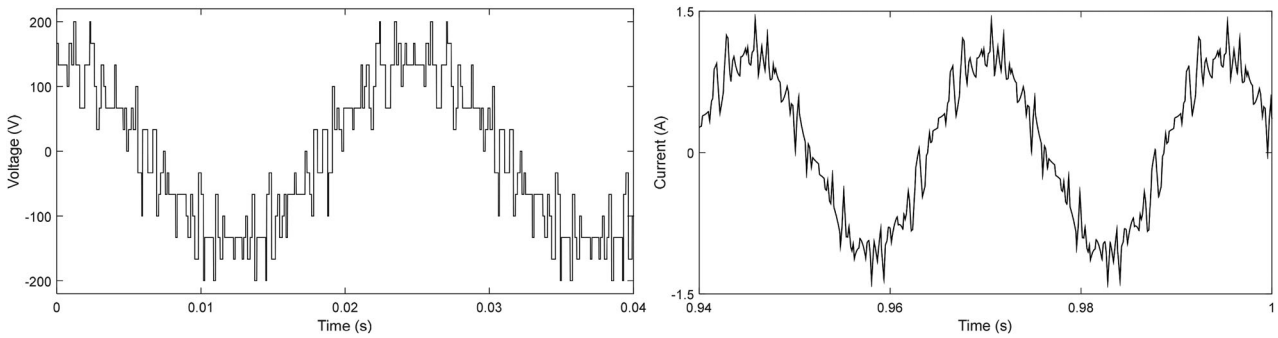


**FIGURE 12.** Simulate OEW-IM phase aa' voltage (left) and current (right) at a $m_a = 0.7$.

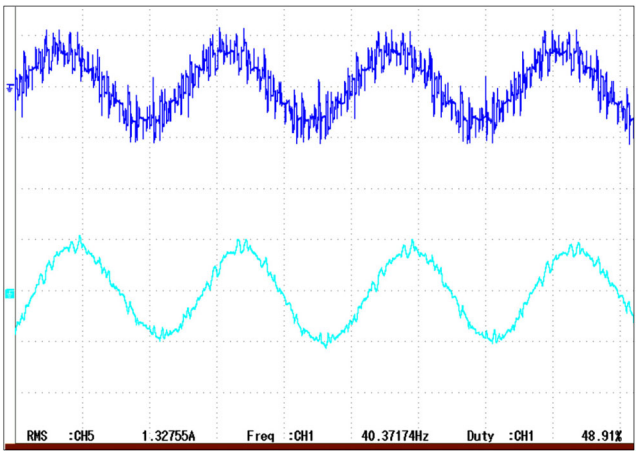


**FIGURE 13.** Experimental OEW-IM phase aa' voltage (top) and current (bottom) at a $m_a = 0.7$.

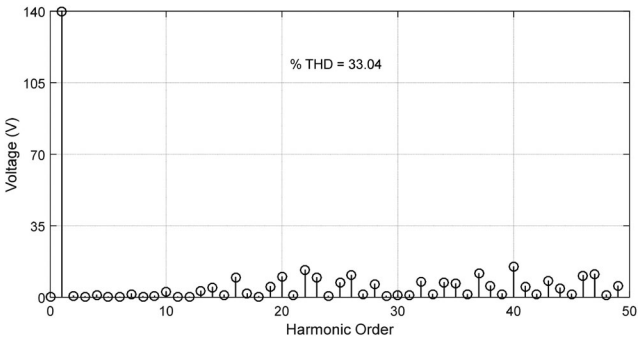


**FIGURE 14.** Simulated harmonic analysis of phase-aa' voltage at $m_a = 0.7$.

The SVPWM scheme suggested in Ref. [18] uses imaginary switching periods to realize the gating signal for the semiconductor devices. The same algorithm was extended to this article. The algorithm uses an offset period ($\boldsymbol{T_{offset}}$) to introduce center space switching or 120° phase clamp switching, as shown in Figure 6.

To reduce the SPL and to achieve the waveform symmetries, the $\boldsymbol{T_{offset}}$ for the green-colored sample is kept as $\boldsymbol{T_s}$-$\boldsymbol{T_{max}}$. The $\boldsymbol{T_{offset}}$ for the samples numbered 1, 7, 8, 14, 15, 21, 22, 28, 29, 35, 36, and 42 is $\frac{T_0}{2} - \boldsymbol{T_{min}}$ (i.e., center spacing SVPWM). For the 2, 9, 16, 23, 30, and 37 samples, the $\boldsymbol{T_{offset}}$ is $-\boldsymbol{T_{min}}$, and for the remaining orange-colored samples, the $\boldsymbol{T_{offset}}$ is $\boldsymbol{T_s}$-$\boldsymbol{T_{max}}$ (i.e., 120° phase clamp SVPWM). Figures 7 and 8, respectively, show the modulating waveform and pole voltages of the proposed SVPWM technique.

Figure 7 shows that both inverters are clamped based on their sample period. It also may be observed from Figure 8 that either inverter-1 (sample number = 7) or inverter-2 (sample number = 4) are clamped, and switching inverter phase-A is clamped (sample number = 7), resulting in a reduction of the SPL.

## 4. RESULTS AND DISCUSSION

The proposed SVPWM approach is initially tested on two 2-level VSIs fed by a 3-phase, 5-HP, and 400 V, 50 Hz, and a 1445 RPM OEW-IM with open-loop ***v/f*** control. A *dSPACE1104* controller is used to generate the dual-inverter system's gating signals, and the experimental setup is shown in Figure 9.

The dual-inverter system's total DC-link voltage for testing is selected as 300 V (|OU| in Figure 3). The total DC-link voltage is divided into a 2:1 ratio to operate at four levels. This results in inverter-1 and inverter-2 having corresponding DC-link voltages of 200 V and 100 V. The OEW-IM simulation parameters are stator resistance ($R_s$) = 4.215 Ω; rotor resistance refereed to the stator ($R_r'$) = 4.185 Ω; stator and rotor leakage reactance ($x_{ls} = x_{lr}'$) = 5.502 Ω; magnetizing reactance ($X_m$) = 162.3 Ω; Motor inertia ($J$) = 0.0131 Kg− m$^2$; Friction coefficient ($B$) = 0.002985 N − m − s.

### 4.1. Results from Experimentation and Simulation

This section shows the experimental and simulation results at a $\boldsymbol{m_a}$ of 0.7 and 1. The modulation index is above 0.866,

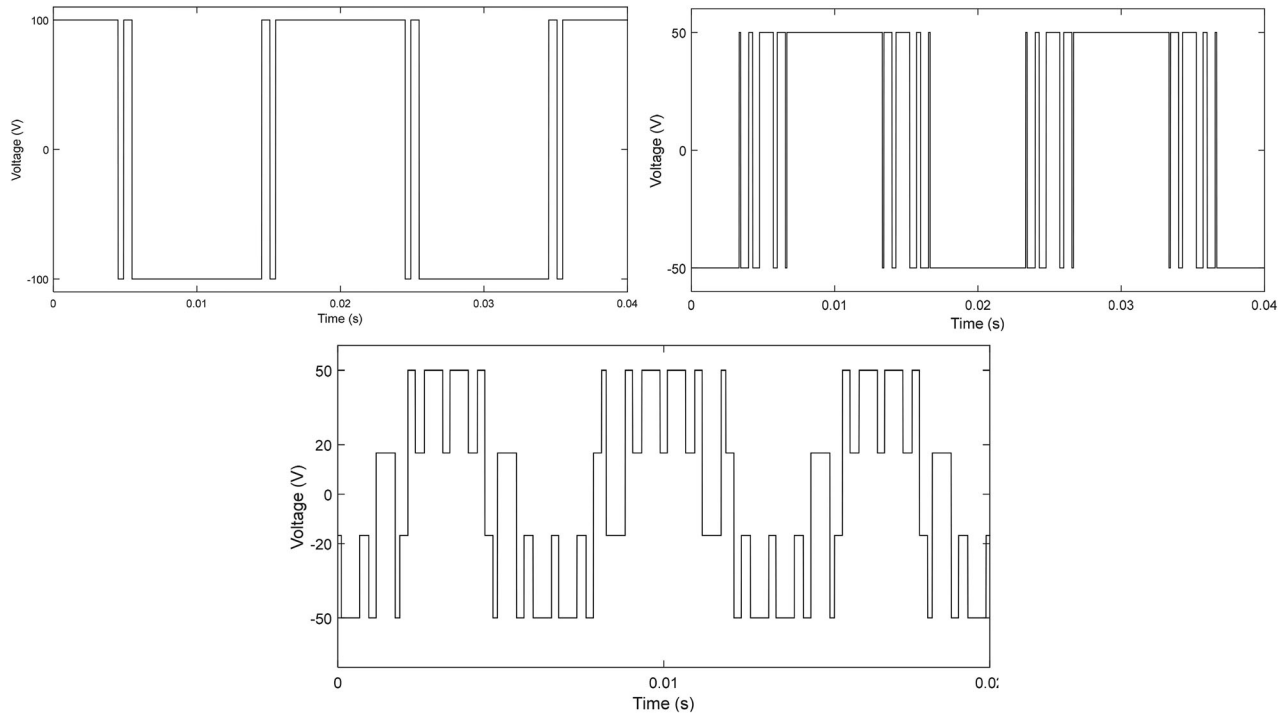


**FIGURE 15.** Pole voltage of inverter-1 (top), inverter-2 (middle) and common mode voltage (bottom) of OEW-IM drive at $m_a = 1$.

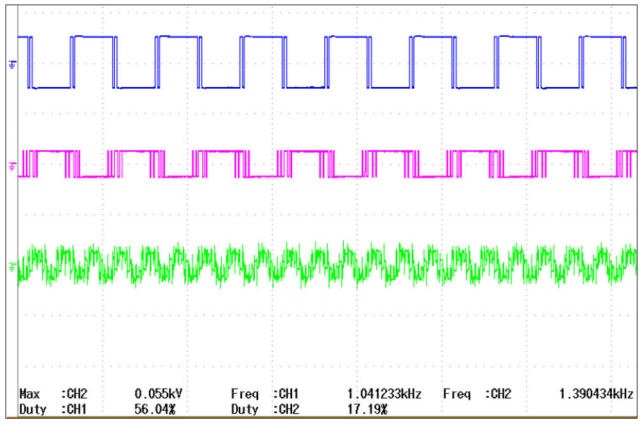


**FIGURE 16.** Experimental pole-voltage of inverter-1 (top), inverter-2 (middle) & common mode voltage (bottom) of OEW-IM drive at $m_a = 1$.

and the OEW-IM operates at a rated supply frequency (i.e., 50 Hz).

Figure 10 depicts the simulated pole voltages of inverter-1 and inverter-2 and the common mode voltage existing between the two common points of DC-source OO' (see Figure 1(b)) of OEW-IM at a modulation index of 0.7. The corresponding experimental results are shown in Figure 11.

The simulated and experimental phase - voltage and current of the OEW-IM drive at a $\boldsymbol{m_a} = 0.7$ are shown in Figures 12 and 13, respectively. The FFT of OEW-IM phase-aa' voltage is shown in Figure 14.

The experimental & simulated results of OEW-IM pole voltages, common-mode voltage, phase-voltage aa', and current, respectively, are shown in Figures 15–18 at $\boldsymbol{m_a} = 1$. From Figures 10–18, it may be observed that the simulation results of the proposed SVPWM technique are validated with the help of experimental results. The suggested SVPWM approaches will significantly minimize the SPL of the dual-inverter system, as demonstrated by experimental pole voltages.

### 4.2. Dynamics of Lower DC-Link Voltage Capacitor

As described in section 2, the LDC-LVC is overcharged by its counterpart for certain switching vector combinations. The SVPWM approach suggested here eliminates troublesome switching vector combinations. When the $\boldsymbol{m_a}$ value is close to 0.6, and the OEW-IM is loaded, the mild charging switching vector combinations may overcharge the LDC-LVC by its counterpart.

The OEW-IM drive ran at a $\boldsymbol{m_a}$ of 0.6 to demonstrate the effectiveness of the planned SVPWMs in preventing the overcharging of LDC-LVC. Figure 19 depicts the corresponding DC-link voltages and motor currents when the

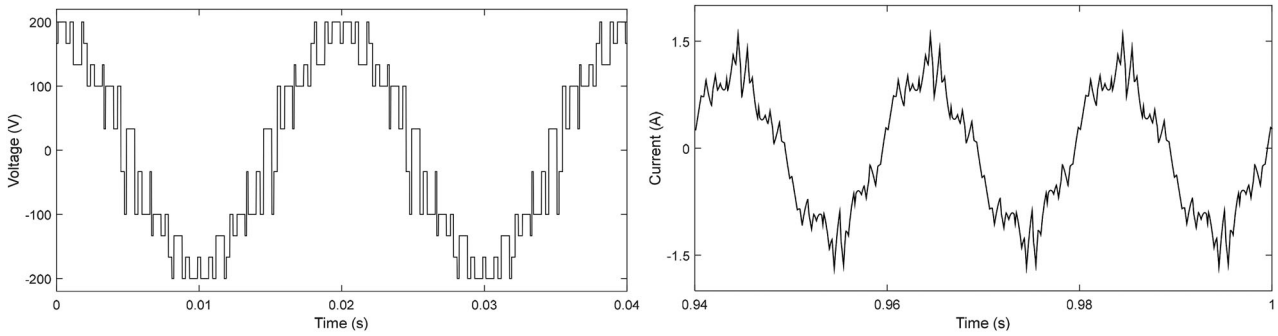


**FIGURE 17.** Phase-aa' voltage (top) and current (bottom) of the OEW-IM simulation at a $m_a = 1$.

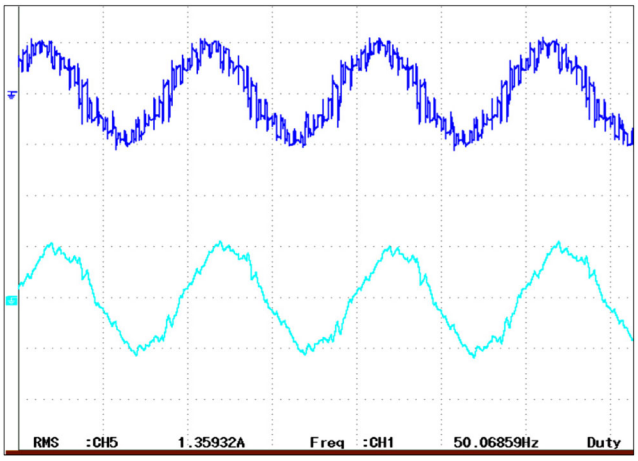


**FIGURE 18.** Experimental OEW-IM phase-aa' voltage (top) & current (bottom) at a $m_a = 1$.

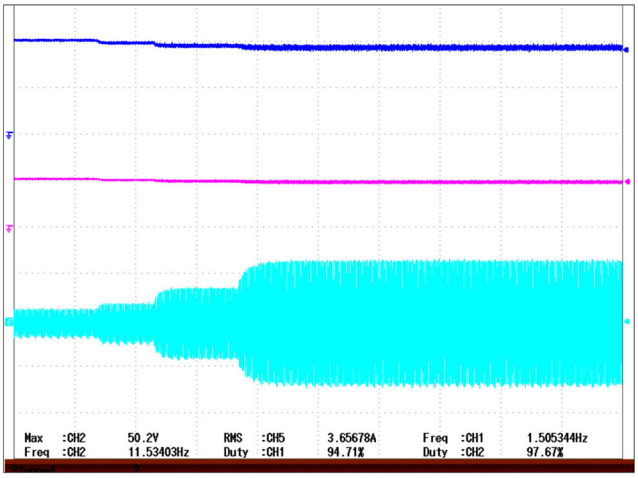


**FIGURE 19.** Experimental balanced DC-Link capacitor voltages of inverter-1 (top), inverter-2 (middle) and OEW-IM phase aa' current (bottom) at $m_a = 0.6$.

motor is loaded. Figure 19 reveals that the DC-link voltage of inverter-2 remains constant even when the OEW-IM drive is loaded.

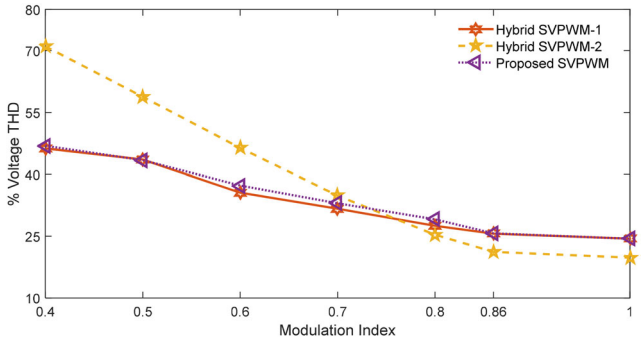


**FIGURE 20.** %Voltage THD of OEW-IM.

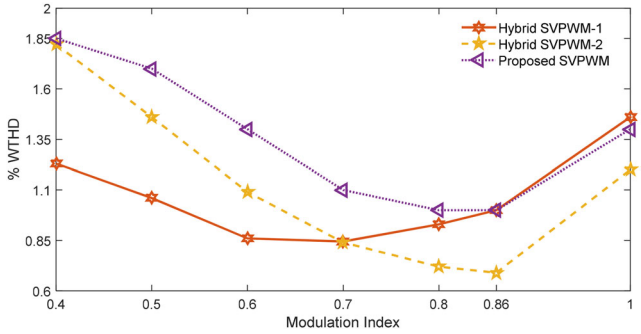


**FIGURE 21.** % WTHD of OEW-IM.

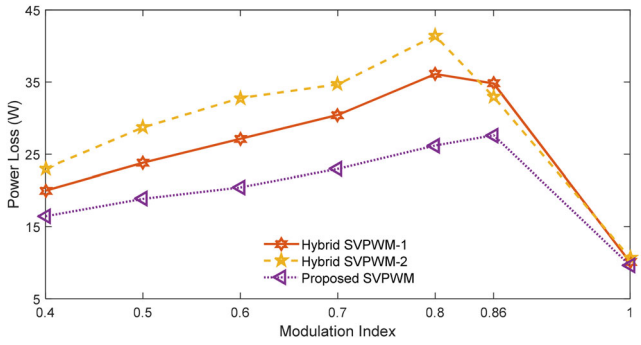


**FIGURE 22.** Total switching power loss of the dual-inverter system.

### 4.3. Performance Evaluation

THD in phase voltage, WTHD, SPL, CPL, TDIL, and torque ripple are performance indicators that are taken to evaluate the OEW-IM drive's performance (Figures 20–25, respectively). The new and existing SVPWM [14] approaches are compared on all performance metrics. The THD and WTHD are calculated at no-load on the OEW-IM. While calculating the switching and conduction power losses, the motor is loaded at 20 N-m for the entire range of modulation index.

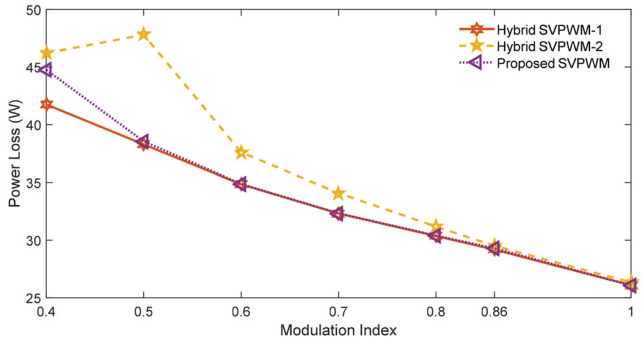


**FIGURE 23.** Total conduction power loss of the dual-inverter system.

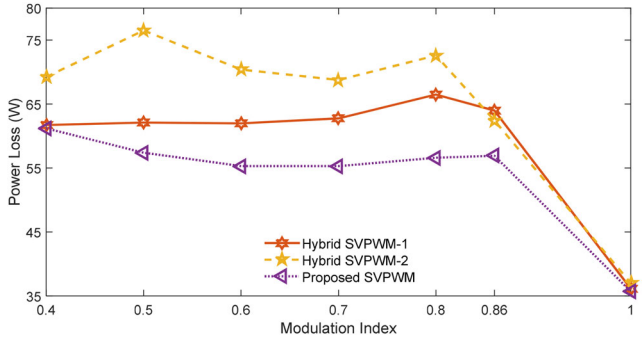


**FIGURE 24.** Total dual-inverter loss vs. $m_a$.

From Figure 20, it is observed that the proposed SVPWM phase voltage THD is comparable to the hybrid SVPWM-1 and lower than hybrid SVPWM-2 in the low and medium speed range of OEW-IM. However, the proposed SVPWM introduces one-phase clamping in the switching inverter; hence, the WTHD is slightly higher than the existing SVPWMs in Figure 21. The loss model used in Ref. [15] is used to calculate both the CPL and SPL of the dual inverter system.

Figures 22 through 24 illustrate, respectively, the SPL, CPL, and TDIL of the dual-inverter system of the OEW-IM drive. Figure 22 shows that the SPL rises linearly with $\boldsymbol{m_a}$ and falls after it reaches a linear modulation limit (i.e., 0.866). And it may observe that the SPL is lower than the hybrid SVPWM techniques. While the TDIL of the dual-inverter system (in Figure 24) exhibits the same SPL pattern, the conduction loss (in Figure 23) is comparable to that of the other two SVPWMs. From Figure 25, it may observe that the steady-state torque ripple is the same for the three SVPWMs. It can be seen from the performance

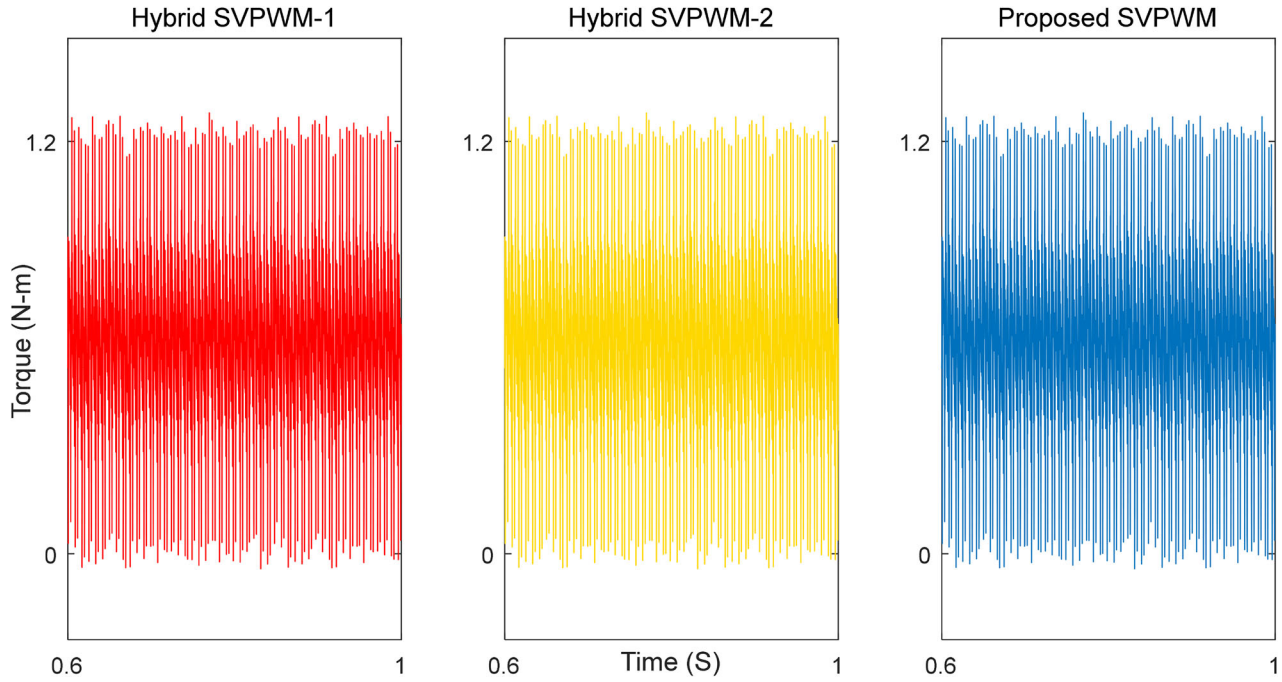


**FIGURE 25.** Torque ripple at $\boldsymbol{m_a} = 0.7$.

indices that the proposed SVPWM voltage THD is on par with one of the existing SVPWMs and decreases switching and total dual-inverter system power loss.

## 5. CONCLUSIONS

This article suggests a new SVPWM scheme for driving a 4-level open-end wound induction motor. The voltage THD of the proposed SVPWM is almost the same as that of the Hybrid SVPWM-1 technique and better than that of the Hybrid SVPWM-2 technique in the low and medium speed range of OEW-IM drive. Also, the proposed SVPWM scheme achieves waveform symmetry, prevents overcharging of the lower DC-link voltage capacitor, and reduces switching power loss and overall dual-inverter loss compared to existing SVPWM techniques.

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## REFERENCES

[1] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9479–9502, Oct. 2019. DOI: 10.1109/TPEL.2018.2890649.

[2] V. T. Somasekhar, M. R. Baiju, K. K. Mohapatra, and K. Gopakumar, "A multilevel inverter system for an induction motor with open-end windings," presented at the IEEE 2002 28th Annu. Conf. Ind. Electron. Soc. IECON 02, vol. 2, 2002. pp. 973–978.

[3] H. K. Patnana and S. Veeramraju Tirumala, "A cost-effective and fault-tolerant brushless direct current drive with open-stator windings for low power electric vehicles," *Int. J. Circ. Theor. Appl.*, vol. 49, no. 9, pp. 2885–2908, 2021. DOI: 10.1002/cta.3048.

[4] U. R. Muduli, A. R. Beig, R. K. Behera, K. A. Jaafari, and J. Y. Alsawalhi, "Predictive control with battery power sharing scheme for dual open-end-winding induction motor based four-wheel drive electric vehicle," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5557–5568, Jun. 2022. DOI: 10.1109/TIE.2021.3091919.

[5] S. Jain, A. K. Thopukara, R. Karampuri, and V. T. Somasekhar, "A single-stage photovoltaic system for a dual-inverter-fed open-end winding induction motor drive for pumping applications," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4809–4818, Sept. 2015. DOI: 10.1109/TPEL.2014.2365516.

[6] L. Vattuone, S. Kouro, G. Estay, and B. Wu, "Open-end-winding PMSG for wind energy conversion system with dual boost NPC converter," presented at the 2013 IEEE Int. Conf. Ind. Technol. (ICIT), Cape Town, South Africa, 2013, pp. 1763–1768.

[7] V. T. Somasekhar, S. Srinivas, and K. K. Kumar, "Effect of zero-vector placement in a dual-inverter fed open-end winding induction motor drive with alternate sub-hexagonal center PWM switching scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1584–1591, May 2008. DOI: 10.1109/TPEL.2008.921170.

[8] V. T. Somasekhar, K. Gopakumar, M. R. Baiju, K. K. Mohapatra, and L. Umanand, "A multilevel inverter system for an induction motor with open-end windings," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 824–836, Jun. 2005. DOI: 10.1109/TIE.2005.847584.

[9] J. Ewanchuk, J. Salmon, and C. Chapelsky, "A method for supply voltage boosting in an open-ended induction machine using a dual inverter system with a floating capacitor bridge," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1348–1357, Mar. 2013. DOI: 10.1109/TPEL.2012.2207741.

[10] V. T. Somasekhar, K. Gopakumar, A. Pittet, and V. T. Ranganathan, "PWM Inverter switching strategy for a dual two-level inverter fed open-end winding induction motor drive with a switched neutral," *IEE Proc. Electr. Power Appl.*, vol. 149, no. 2, pp. 152–160, Mar. 2002. DOI: 10.1049/ip-epa:20020127.

[11] B. Venugopal Reddy, V. T. Somasekhar, and Y. Kalyan, "Decoupled space-vector PWM strategies for a four-level asymmetrical open-end winding induction motor drive with waveform symmetries," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5130–5141, Nov. 2011. DOI: 10.1109/TIE.2011.2116759.

[12] S. Lakhimsetty and V. Somasekhar, "Discontinuous decoupled SVPWM schemes for a four-level open-end winding induction motor drive with waveform symmetries," *IET Power Electron.*, vol. 11, no. 2, pp. 280–292, 2018. DOI: 10.1049/iet-pel.2017.0096.

[13] S. Lakhimsetty, N. Surulivel, and V. T. Somasekhar, "Improvised SVPWM strategies for an enhanced performance for a four-level open-end winding induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2750–2759, Apr. 2017. DOI: 10.1109/TIE.2016.2632059.

[14] S. Lakhimsetty, P. Hema Kumar, and V. T. Somasekhar, "Hybrid space-vector pulse width modulation strategies for a four-level open-end winding induction motor drive with an improvised harmonic performance and balanced DC-link capacitors," *Int. Trans. Electr. Energy Syst.*, vol. 31, pp. e12814, 2021.

[15] S. Lakhimsetty and V. T. Somasekhar, "A four-level open-end winding induction motor drive with a nested rectifier–inverter combination with two DC power supplies," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8894–8904, Sept. 2019. DOI: 10.1109/TPEL.2018.2884023.

[16] V. T. Somasekhar, B. Venugopal Reddy, and K. Sivakumar, "A four-level inversion scheme for a 6n-pole open-end winding induction motor drive for an improved DC-link utilization," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4565–4572, Sept. 2014. DOI: 10.1109/TIE.2013.2288212.

[17] S. Chowdhury, P. W. Wheeler, C. Patel, and C. Gerada, "A multilevel converter with a floating bridge for open-end winding motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5366–5375, Sept. 2016. DOI: 10.1109/TIE.2016.2561265.

[18] D.-W. Chung, J.-S. Kim, and S.-K. Sul, "Unified voltage modulation technique for real-time three-phase power conversion," *IEEE Trans. Ind. Appl.*, vol. 34, no. 2, pp. 374–380, Mar.–Apr. 1998. DOI: 10.1109/28.663482.

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