A Phase-Clamped Proportional Duty Decoupled SVPWM Technique for a Four-Level Open-End Winding Induction Motor Drive

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***Abstract*: A dual two-level inverter fed an open-end winding induction motor (OEW-IM) can provide four-level inversion if the inverter's DC-link voltages are in a 2:1 ratio. Centre Spaced Decoupled Space Vector Pulse Width Modulation (CSDSVPWM) techniques were proposed for this drive to avoid the problem of overcharging the lower DC-link capacitor voltage. In this paper, a Phase Clamped Decoupled Proportional Duty SVPWM (PCDPD_SVPWM) technique is proposed for this drive, wherein the null vector combination is placed at the extreme edge of the sampling time period. This PWM technique clamps one phase of each inverter, lowering the switching frequency and, hence, the switching power loss. The motor phase voltage and current spectral performance are evaluated for the drive and compared between the proposed PCDPD-SVPWM and CSDSVPWM techniques.**

***Index Terms*: Null vector placement, Phase Clamping, Proportional Duty, Space Vector Modulation**

I. INTRODUCTION

The advantages of Multilevel Inverters over the conventional 2-level inverters are well documented [1 - 3]. The most common and popularly available multilevel inverter topologies are diode-clamped inverters, cascaded-H-bridge (CHB) inverters, and flying-capacitor (FC) inverters. The diode-clamped inverter is plagued with the problem of neutral point voltage fluctuations, complicated PWM switching design and additional clamping diode requirements. More DC capacitors are needed with capacitor voltage control in the FC inverter. The CHB inverter needs more H – Bridges as the voltage levels increase. Various PWM methods are available in the literature [4-6] to improve the voltage levels, lessen the converter switching loss and enhance the converter performance for specific applications.

The three-phase induction motor with its stator windings opened on either side (the so-called OEW-IM) can be used as an alternative for multilevel inversion to overcome some drawbacks. The main advantage of the OEW-IM drive is that multilevel voltage can be achieved with the two 2-level VSIs. In ref. [7], four-level inversion was realized with a dual-inverter fed OEW_IM, in which the input DC-link voltages are in the proportion of 2:1 (shown in Fig. 1). In general, the OEW_IM drive suffers from the problem of zero-sequence currents. However, employing isolated DC power supplies successfully overcomes this problem [8-9]. The circuit in Fig. 1 has a limitation in that the DC-link capacitor with a lower voltage is overcharged by the DC-link capacitor with a higher voltage. Two variants of Center Spaced Decoupled SVPWM (CSDPWM) strategies, called Equal-Duty (ED_CSDSVPWM) and Proportional-Duty (PD_CSDSVPWM) Decoupled PWM techniques are proposed to avoid this problem in the work described in [8]. However, both of these PWM schemes switch the dual inverters. This increases the dual-inverter system switching power losses.

To address this problem, this paper presents a Phase-clamped SVPWM, in which only two phases are switched, and one phase is clamped in a given sampling time period. This is accomplished by exploiting a well-known fact that SVPWM schemes offer a choice in the placement of the null vector. While the implementation of such a PWM scheme is straightforward in the case of a simple two-level VSI or an OEW_IM drive with two equal DC sources, it poses difficulties in the present case to obtain waveforms with half-wave, full-wave and quarter-wave symmetries despite the structural dissymmetry of the power circuit.

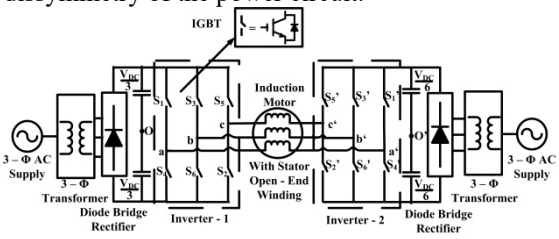

Fig. 1: Four-level OEW_IM

II. DUAL-INVERTER FED FOUR-LEVEL OEW_IM Drive

A three-phase induction motor can be converted into an OEW-IM by disconnecting either the neutral point (for a star-connected stator) or the end connections (for a delta of the stator). To achieve

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four-level inversion, the OEW_IM is fed with two 2-level inverters in a 2:1 ratio with different DC link voltages (Fig. 1). The DC link voltages of inverter-1 and 2, respectively are $2V_{DC}/3$ and $V_{DC}/3$ respectively. Fig. 2 shows inverter-1 & 2 space-vectors numbered 1 – 8 and 1' – 8' respectively.

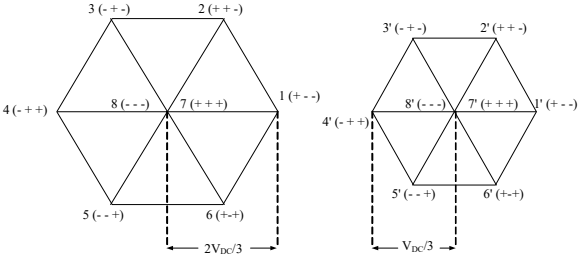


Fig. 2: Inverter 1 (left) & inverter 2 (right) space vector diagrams

Fig. 3 shows a total of 64 (8×8) switching vector combinations will result in the dual-inverter system, which is located in 37 space vector locations and has 54 sectors. The pole voltage of inverter – 1 (v_{ao}) having the possible values of $V_{DC}/3$ and $-V_{DC}/3$, similarly, the possible values of inverter – 2 ($\mathbf{v_{a'o'}}$) are $V_{DC}/6$ and $-V_{DC}/6$. The difference in pole voltages shows four distinct levels (Table 1), confirming this circuit is a four-level inverter.

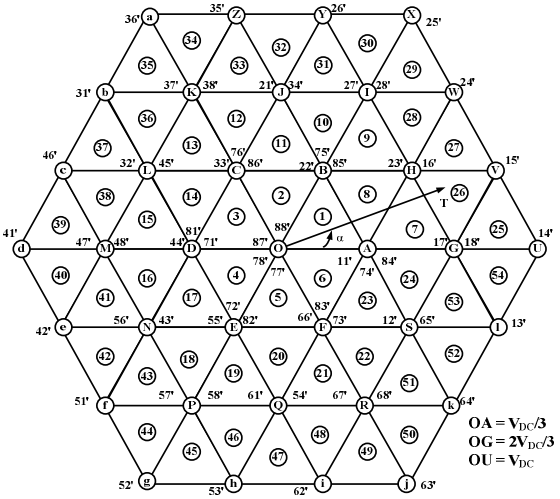


Fig. 3: Dual inverter system space vector diagram

Table I: Four-Level operation of OEW_IM

Pole voltage of inverter – 1 ($\mathbf{v_{ao}}$)	**Pole voltage of inverter – 2** ($\mathbf{v_{a'o'}}$)	**Difference in pole voltages** ($\mathbf{v_{aa'} = v_{ao} - v_{a'o'}}$)
$-V_{DC}/3$	$-V_{DC}/6$	$-V_{DC}/2$
$-V_{DC}/3$	$V_{DC}/6$	$-V_{DC}/6$
$V_{DC}/3$	$-V_{DC}/6$	$V_{DC}/6$
$V_{DC}/3$	$V_{DC}/6$	$V_{DC}/2$

III. PHASE CLAMPED DECOUPLED PROPORTIONAL DUTY SVPWM STRATEGY

Fig. 4 explains the basic principle of decoupled SVPWM technique. The reference space vector (**OT**) is synthesized with inverter-1 (**OT1**) and inverter-2 (**OT2**) given as $|V_{sr}|\angle\alpha$. These components' magnitude in proportion to DC-link voltages and the length of each vector is $|2V_{sr}/3|\angle\alpha$ and $|V_{sr}/3|\angle(180° + \alpha)$ respectively. The vector **OT₁** and **OT₂** are used to determine the instantaneous phase voltages of inverter – 1 ($v_{a1}{}^*, v_{b1}{}^*, v_{c1}{}^*$) and inverter – 2 ($v_{a2}{}^*, v_{b2}{}^*, v_{c2}{}^*$). The switching times for the switching devices (T_{ga1}, T_{gb1}, and T_{gc1}) of inverters 1 & 2 are obtained using the switching algorithm presented in [10].

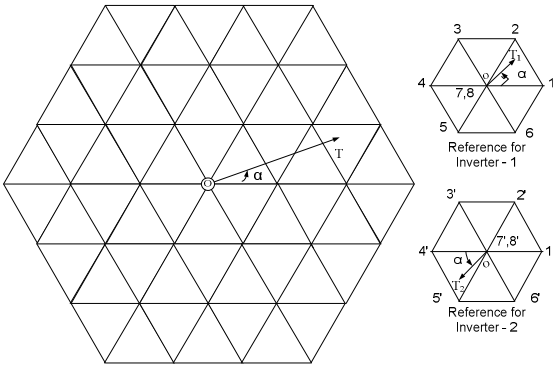


Fig. 4: Principle of operation of Center Spaced Decoupled PWM (CSDPWM) strategy (not drawn to scale)

Unlike the PWM strategy proposed in [8], which places the *effective period* (the sum of the active vector switching time intervals) in the center space, the proposed PCDPD_SVPWM strategy places the effective period at an extreme corner. This is accomplished by replacing the so-called *Offset period*, which is given by $(T_o/2 - T_{min})$ for the CSDSVPWM to either $(-T_{min}\ or\ T_s - T_{max})$ [9]. This maneuver reduces the commutations to *two per inverter*, i.e., in a sample interval, a total of four for the dual-inverter system. To ensure waveform symmetries, the following rules suggested in [11] are complied with:

a) The total samples are odd in one sector (i.e., 60^0). In the present work, this number is 5 (inverter-1) and 9 (inverter-2). In other words, a total of 30 (6x5) and 54 (6x9) samples are chosen per cycle.
b) Sampling is avoided along the boundaries of sectors.
c) A sample always exists on the lines, which divide any given sector into two halves (at 30^0, 90^0, etc.). However, to ensure quarter-wave symmetries, these samples should be synthesized with centre spacing [8]. This would lead to one extra switching per sector or 6 additional commutations in a cycle *per inverter* (or 12 additional commutations for the dual-inverter system), as shown in Fig. 5.

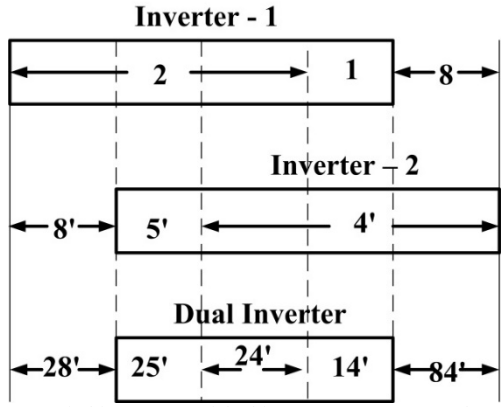
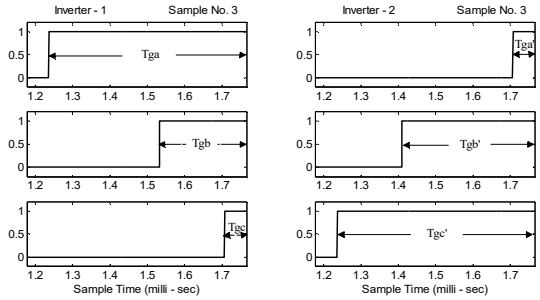


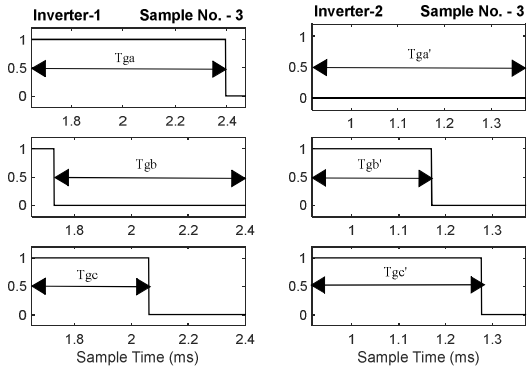
Fig. 5: Switching pattern of dual inverter system at sample No. 1

From the above discussion, it is evident that the CSDSVPWM would result in 252 switching transitions for the *dual inverter* system. In contrast, the proposed PCDPD_SVPWM scheme results in 203 switching transitions (2 switching operations per sample x number of samples (30 for inverter-1 and 54 for inverter-2) + 16 additional switching operations *per inverter*). Thus, the switching loss with the proposed PCDPD_SVPWM would be considerably lesser as the number of commutations is reduced by 19.44%.

Fig. 6 presents the typical switching sequences for the two schemes. The complete switching table for the dual-inverter scheme switched with the PCDPD_SVPWM scheme is presented in Table 2.



(a)



(b)

Fig. 6: Switching periods of inverter-1 & 2 at sample no. 3: (a) CSDSVPWM (b) PCDPD_SVPWM

Simulation studies are carried out using MATLAB for different values of modulation indices by assuming that the OEW_IM drive operates in open loop V/Hz control. A fixed number of samples (i.e., 30 and 54) are employed per cycle to implement the space vector modulation. The DC input voltages for inverters 1 and 2 are 200 V and 100 V, respectively.

Table II: Switching Sequence of PCDPD_SVPWM

Sample No.		Switching states	
Inverter - 1	Inverter - 2	Inverter - 1	Inverter - 2
1	1	2-1-8	4-5-8
	2		8-5-4
2	3	8-1-2	4-5-8
	4		8-5-4
3	5	7-2-1-8	7-4-5-8
4	6	1-2-7	5-4-7
	7		7-4-5
5	8	7-2-1	5-4-7
	9		7-5-4
6	10	3-2-7	5-6-7
	11		7-6-5
7	12	7-2-3	5-6-7
	13		7-6-5
8	14	8-3-2-7	8-5-6-7
9	15	2-3-8	6-5-8
	16		8-5-6
10	17	8-3-2	6-5-8
	18		8-5-6
11	19	4-3-8	6-1-8
	20		8-1-6
12	21	8-3-4	6-1-8
	22		8-1-6
13	23	7-4-3-8	7-6-1-8
14	24	3-4-7	1-6-7
	25		7-6-1
15	26	7-4-3	1-6-7
	27		7-6-1
16	28	5-4-7	1-2-7
	29		7-2-1
17	30	7-4-5	1-27
	31		7-2-1
18	32	8-5-4-7	8-1-2-7
19	33	4-5-8	2-1-8
	34		8-1-2
20	35	8-5-4	2-1-8
	36		8-1-2
21	37	6-5-8	2-3-8
	38		8-3-2
22	39	8-5-6	2-3-8
	40		8-3-2
23	41	7-6-5-8	7-2-3-8
24	42	5-6-7	3-2-7
	43		7-2-3
25	44	7-6-5	3-2-7
	45		7-2-3
26	46	1-6-7	3-4-7
	47		7-4-3
27	48	7-6-1	3-4-7
	49		7-4-3
28	50	8-1-6-7	8-3-4-7
29	51	6-1-8	4-3-8
	52		8-3-4
30	53	8-1-6	4-3-8
	54		8-3-4

The dual inverter system's modulation index (ma) is the ratio of the magnitude of the (**OT** in Fig. 3) to the sum of the individual DC input voltages of the inverters 1 and 2. Fig. 7 shows the modulating function of inverters -1 and 2.

Fig. 8 shows the inverter-1 & 2 pole voltages at m_a = 0.7. The corresponding motor phase current and voltage are shown in Fig. 9. Fig. 10 shows the motor phase voltage harmonic spectrum. Figures 11 and 12 show the THD in voltage and the Weighted THD (WTHD) of the motor phase voltage with the proposed PCDPD_SVPWM scheme along with the two variants of the CSDSVPWM scheme, namely the ED_CSDSVPWM & PD_CSDSVPWM. From these, the proposed PWM scheme has better spectral performance despite lower switching than the CSDSVPWM schemes.

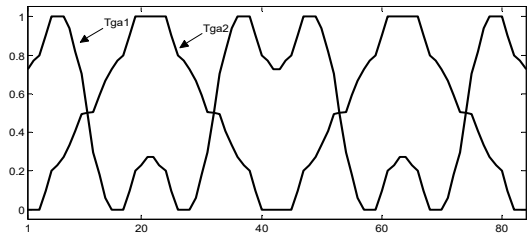


Fig. 6: Modulating waveforms of Inverter – 1 (T_{ga1}) and Inverter – 2 (T_{ga2})

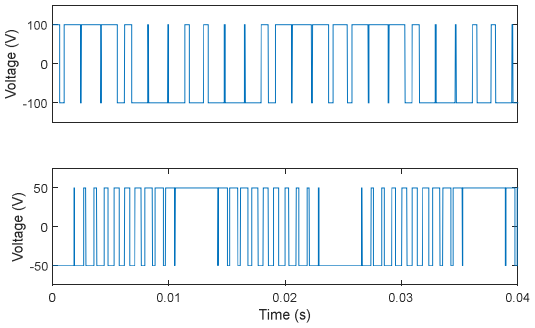


Fig. 8: Pole voltage of Inverter – 1 (Top) & 2 (Bottom)

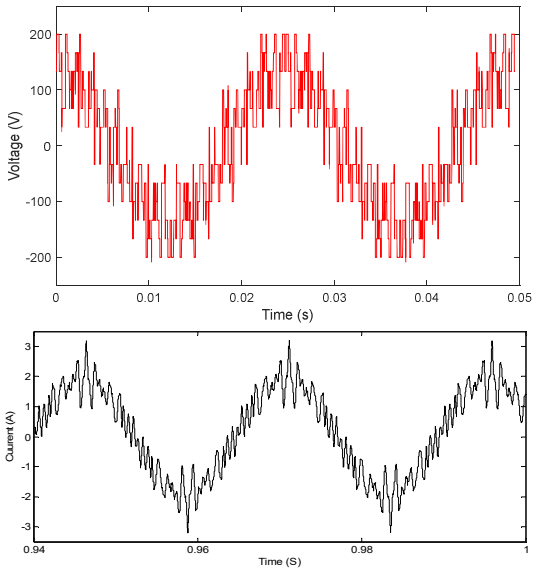


Fig. 9: OEW_IM phase voltage (Top) & current (Bottom)

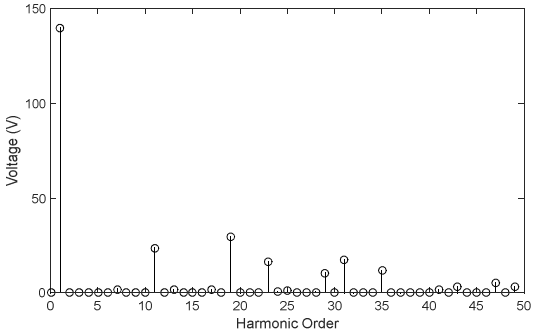


Fig. 10: Spectral of OEW_IM phase voltage at m_a = 0.7

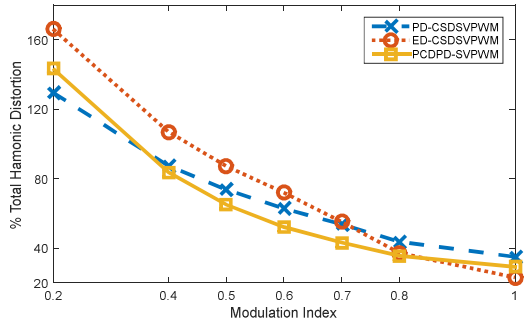


Fig. 11: Modulation Index vs Total Harmonic Distortion

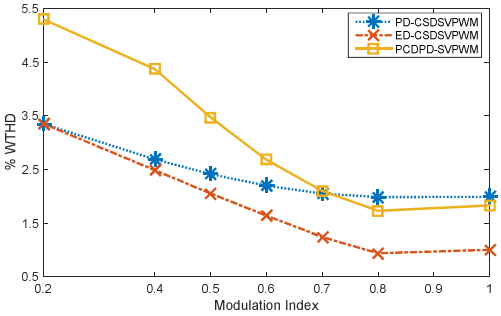


Fig. 12: Modulation index vs Weight Total Harmonic Distortion

IV. CONCLUSION

This paper proposes a Phase-Clamped Decoupled Proportional Duty SVPWM scheme, which lowers the switching power loss of semiconductor devices in a dual-inverter fed OEW_IM drive. This is accomplished by decreasing the number of commutations per sampling period. Despite the lower switching frequency, the spectral quality is better than the Center Spaced Decoupled SVPWM scheme. Despite an unsymmetrical power circuit, the proposed PWM scheme achieves the three-phase, half-wave and quarter-wave symmetries. Simulation results are presented, which demonstrate the effectiveness of the proposed PWM scheme.

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