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Improved T-Type and ANPC Multilevel Converters by Means of GaN-Based T-Cell Branch and Bidirectional Device

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***Abstract*—By integrating standard power electronic modules like the half-bridge and bidirectional unit, it is possible to create a T-type circuit that is versatile for use in both DC-AC and AC-DC applications. Using these, various arrangements of bidirectional DC-AC converters, including mid-point-clamped-based multilevel inverters (MLIs), can be constructed. However, realization of such T-type circuit in mid point-clamped MLIs with limited voltage blocking capability of the available wide-band-gap devices is challenging as these MLIs suffer from half dc-link voltage utilization at the ac output. In this paper, new opportunities of bidirectional and T-cell branch in MLIs with Gallium Nitride-high electron mobility transistors (GaN-HEMTs) are outlined. Thanks to the contribution of a front-end T-cell branch, the half dc-link voltage utilization factor of the conventional mid point-clamped-based MLIs is enhanced, whilst more number of output voltage levels can be generated facilitating incorporation of standard commercially available 650 V GaN-HEMTs. This results in the creation of new MLIs that feature smaller grid-interfaced filters, reduced overall losses, and improved power density. Moreover, with additional bidirectional GaN-based cell, application of such converters can be further broadened within new inductor-less dual-mode MLIs topologies operating over a wide range of input dc voltage changes. Theoretical analysis with several simulation and experimental results extracted from a 3 kW, 99.2% efficiency, 1.92 kW/L GaN-based prototype are given to corroborate the effectiveness and feasibility of the proposed solution.**

***Index Terms*—Gan-HEMTs, Power electronics building Blocks, multilevel inverters, Bidirectional switches.**

I. Introduction

Towards more reliable, compact, and highly efficient design of power converters, power electronics building blocks (PEBBs) with either a standard half-bridge or bidirectional module play an essential role. When it comes to wide-band-gap (WBG) devices, utilization of such standard circuits in modular power converters becomes more crucial as they can integrate gate driver, and protection circuit in power module with a reduced parasitic stray inductance [1]. Standard WBG-based half-bridge and bidirectional PEBBs with back-to-back (B2B) connection of two or four devices can be integrated into each other to create a T-cell branch [2].

While nearly all bidirectional dc-ac power electronics converters can be built utilizing these PEBBs, the variances in voltage ratings and the temperature-dependent nature of on-state parasitic resistance in Wide Bandgap (WBG) devices remain challenging. Utilizing SiC MOSFETs in such PEBBs can give the option to incorporate 1200 V WBG devices but at the cost of large reverse recovery loss in hard-switched operation, and poor power density of the entire system [3]. Gallium Nitride-high electron mobility transistors (GaN-HEMTs) are the other option among WBGs with zero reverse recovery loss, low parasitic resistance/capacitance with an ability to increase the power density. However, discrete utilization of them in bidirectional modules, while they are fabricated based on the lateral design of GaN-on-Si with a limited 650 V rated voltage of commercially available devices, still is a matter of challenge [4]. Fig. 1 shows a brief comparative study from temperature-dependency point of on-state resistance and conduction losses within two selected 650 V SiC and GaN-HEMTs devices configured as a bidirectional device.

Regarding such constraints, application of GaN-HEMTs in conventional three-level (3L) mid point-clamped-based grid-connected converters, i.e., single-phase T-type or active neutral point-clamped (ANPC) converters, needs further attention as such converters demand large dc-link input voltage, i.e., 800 V to realize a half dc-link voltage utilization at their ac

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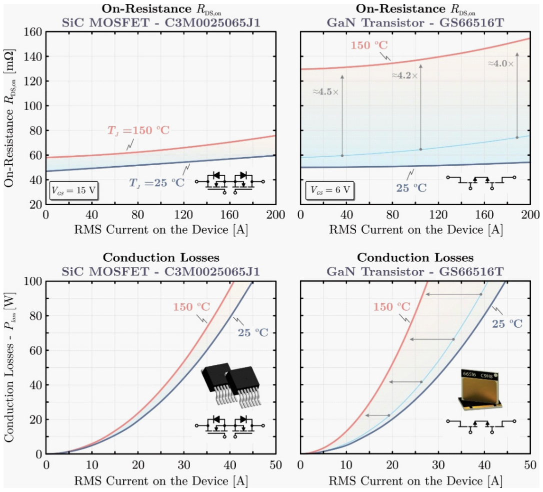


Fig. 1: A comparison of temperature-dependent on-state resistance and conduction losses of the bidirectional devices with discrete SiC and GaN-HEMTs-based devices.

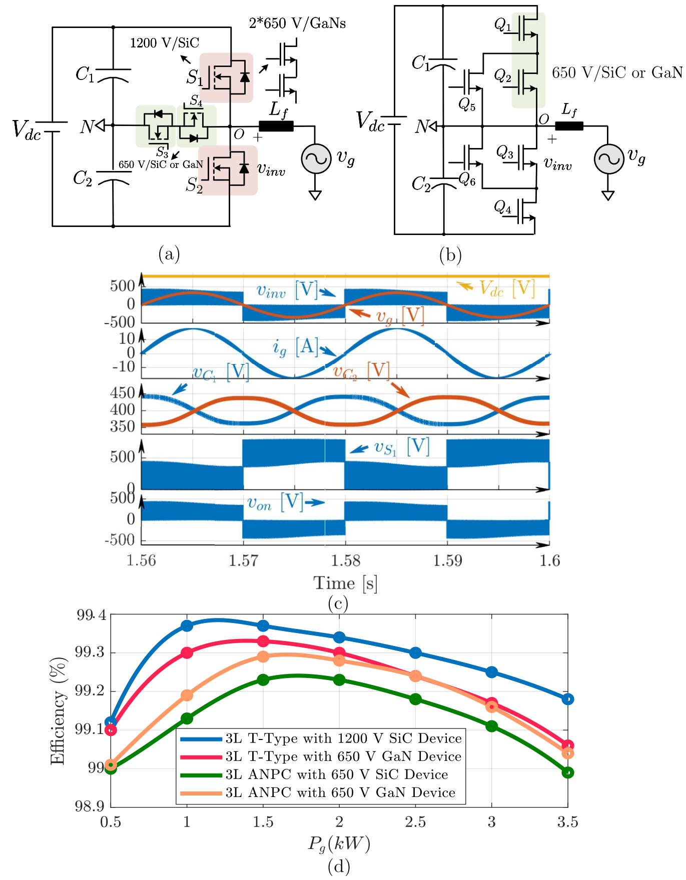


Fig. 2: Single-phase 3L grid-connected converters with WBG devices being fed through V_{dc}=800 V dc voltage based on a standard (a) T-Type, (b) ANPC structure, (c) detailed simulation results for a single-phase 3L T-type converter using PLECS at P_g=3 kW, L_f=1.2 mH, and f_{sw}=50 kHz, (d) overall efficiency comparison of 3L T-Type and 3L-ANPC converters with 1200 V SiC and 650 V GaN devices at f_{sw}=50 kHz.

output [5]. Herein, reduction of voltage stress among the devices with multilevel inverters (MLIs) is of interest to utilize standard half-bridge/T-type modules with GaN-HEMT devices [6]. With T-type and bidirectional devices, new opportunities for conventional mid point-clamped MLIs developing with GaN-HEMTs technology can be provided to improve the dc-link voltage utilization factor, power density and overall efficiency.

The paper is outlined by showing the existing problem of single-phase 3L grid-connected T-type/ANPC converter in utilization of GaN-HEMTs devices in Section II. Importance of additional T-type branch as a front-end active circuit to realize new MLIs is discussed in Section III. New derived topology of MLIs using additional bidirectional devices to realize a inductor-less dual-mode operation in presence of a large variation in input dc voltage is introduced in Section IV. And finally, the experimental results of a GaN-based five-level (5L) dual T-type converter are given in Section V followed by some conclusions in Section VI.

II. Single-Phase 3L T-Type/ANPC Converters: Problem Statement

3L T-type converter shown in Fig. 2(a) offers a mid point-clamped-based structure requiring around 800 V input dc voltage to feed a standard single-phase grid with 340 V peak voltage. Fig. 2(c) illustrates its detailed operation when around 3 kW power with 50 kHz switching frequency is injected into the grid. Even though delivering an appealing performance from overall efficiency point of view, its development using WBG devices is challenging as the half-bridge devices, i.e., S_1 and S_2, have to block 800 V stress voltage. Hence, utilization of either 1200 V SiC MOSFETs or two series connection of 650 V GaN-HEMTs is imperative. However, the very fast switching behaviour of GaN-HEMTs with a possible mismatch condition of C_{oss} for two discrete devices in series makes the realisation of T-type converters with 650 V GaN-HEMTs more costly and less reliable [4].

Concurrently, 3L ANPC converter shown in Fig. 2(b) is a feasible alternative for the above-mentioned 3L T-type converter as it needs three half-bridge-based PEBBs with a 400 V uniform stress over the devices. The efficiency performance of both 3L single-phase T-type and ANPC converters using 1200 V and 650 V SiC MOSFETs, and 650 V GaN-HEMTs, with part number of UF3C120040K3S, UF3C065030K4S, and GS66516T, respectively, have been demonstrated in Fig. 2(d). The results have considered semiconductor and grid-interfaced filter losses in PLECS environment confirming more than 99% of overall efficiency for both cases within a wide range of injected power [3]. Similar to 3L T-type converter, the input dc-link voltage of 3L-ANPC converter must be still 800 V to generate a 3L output with 400 V peak voltage. This can still enlarge the volume of the system with a poor overall efficiency as providing large dc-link voltage from a renewable energy-based resource like battery packs, fuel cells and photovoltaic (PV) panels needs additional measures and power processing stages.

TABLE I: Switching states of the proposed dual T-type 5L converter

v_{inv}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+V_{dc}/2$	0	0	0	1	1	0	1	0
$-V_{dc}/2$	0	0	0	1	1	0	0	1
$+V_{dc}$	0	1	0	0	0	0	1	0
$-V_{dc}$	1	0	0	0	0	0	0	1
0	0	0	1	1	1	1	0	0

III. New Hybridized MLIs With Additional T-Type Branch

In order to fully utilize the input dc-link voltage at the ac output of the above-mentioned mid point-clamped-based converters, the concept of additional T-type branch can be leveraged as can be seen from Fig. 3(a)-(c) [5]. Herein, using a dual T-type configuration shown in Fig. 3(a), 5L output voltage can be generated at the ac output, while its peak voltage is equal to V_{dc}. Through this configuration, four devices namely as S_1, S_2, S_3, and S_4 can withstand a voltage stress equals to V_{dc}, while the stress voltage across the bidirectional devices is $\pm V_{dc}/2$. Hence, utilization of commercial available GaN-HEMTs, i.e., 650 V GaN devices from GaN System or Transphorm manufacturers, can be facilitated for such a dual T-type converters. Table I outlines the details of switching states to generate each level of the output voltage. As can be seen, instead of transferring the voltage across the dc-link capacitors to the output in 3L configurations, series connection of such capacitors voltages can generate the top positive/negative output voltage levels.

The idea of applying a front-end T-type branch into the existing 3L ANPC converters [see Fig. 3(b)] can also offer the same advantages, i.e., full dc-link voltage utilization at the ac output with 5L output voltage. Interestingly, by feeding a 400 V input voltage to such an hybridized 5L ANPC/T-cell converter, the stress voltage of all the ANPC devices is only 200 V aiming at utilization of GaN devices with smaller footprints, i.e., EPC-based chips.

This concept can further be generalized as shown in Fig. 3(c), where any standard types of mid point-clamped-based MLIs with N number of output levels can be used as a back-end low-voltage stage with a front-end T-cell PEBB. Hence, the number of output voltage levels can be enhanced up to $N + 2$, while full dc-link voltage utilization at the ac output is attained.

An additional benefit of the front-end T-cell circuit in new MLI topologies is to apply the phase-shifted pulse width modulation (PS-PWM). Hence, depending on the number of output voltage levels, the apparent switching frequency of the ac output can be enhanced leading to utilizing a reduced size grid-interfaced filter with a lower value of effective switching frequency. Details of PS-PWM strategy applied to the proposed 5L dual T-type converter can be seen from Fig. 4, while the apparent switching frequency of 5L output voltage is two-time larger than effective switching frequency of the devices. Generation of multilevel waveform at the ac output with a reduced voltage stress over the devices and PS-PWM technique can significantly reduce the semiconductor conduction and switching losses [6]. Considering, $I_{g,rms}$ as the rms current injected to the grid, with $R_{on}(V_{dc})$ and

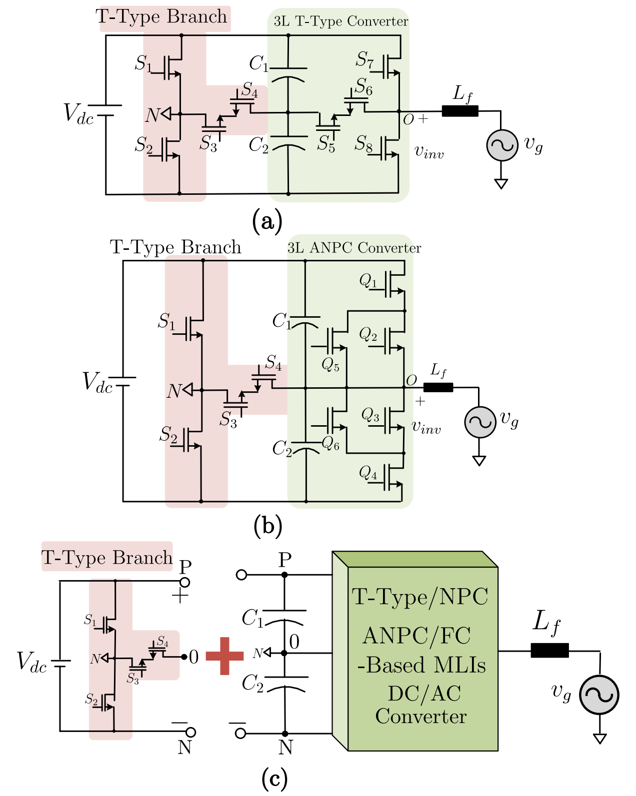


Fig. 3: New 5L grid-connected GaN-based converters for full dc-link voltage utilization based on (a) dual T-type converter, (b) a hybrid structure of T-type and ANPC converter, and (c) generalized concept for realization of new MLIs with full dc-link voltage utilization at the ac output.

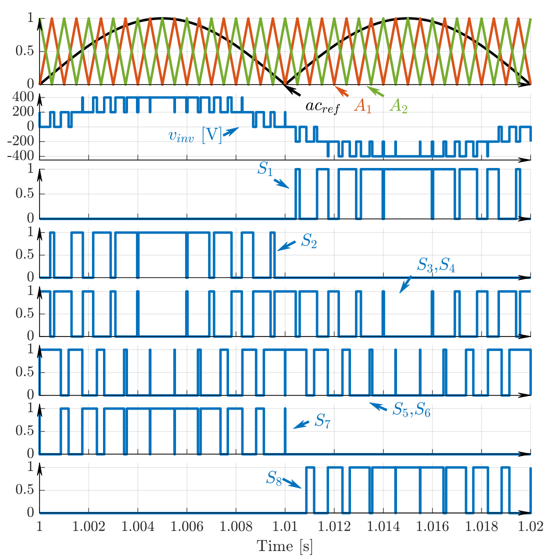


Fig. 4: Principle of PS-PWM for the proposed 5L dual T-type converter.

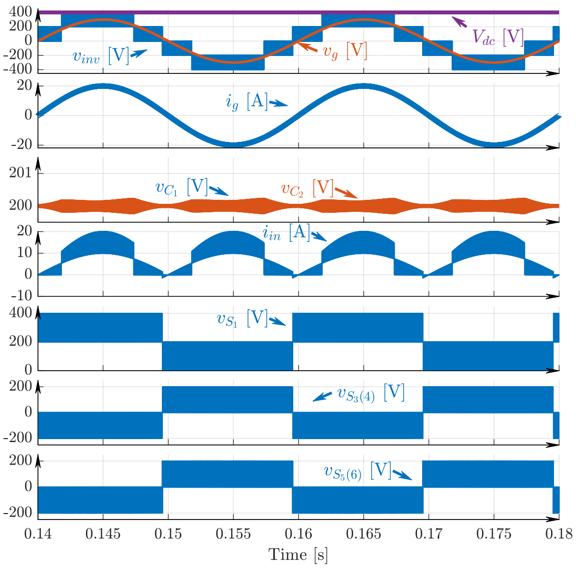
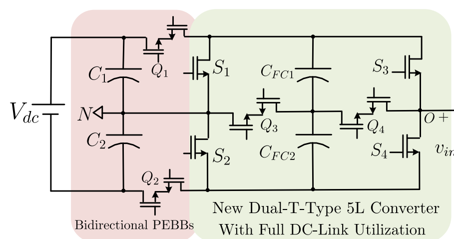


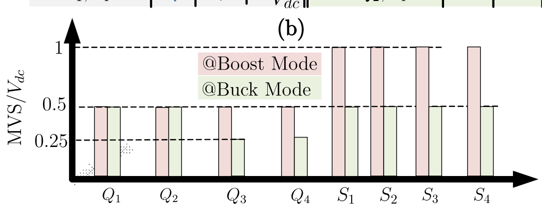
Fig. 5: Detailed simulation results of the proposed 5L dual T-type converter using PLECS at P_g=3 kW, L_f=1.5 mH, and f_{sw}=25 kHz.



(a)

Switching States	@Boost Mode ON Switches	C_{FC1}	C_{FC2}	v_{inv}	@Buck Mode ON Switches	C_{FC1}	C_{FC2}	v_{inv}
1	Q_1, Q_2, Q_3, Q_4	▲	▲	0	Q_3, Q_4	–	–	0
2	Q_1, Q_2, Q_3, S_3	▲	▲	$+\frac{V_{dc}}{2}$	Q_1, Q_4	▲	–	$+\frac{V_{dc}}{4}$
					Q_3, S_3	▼	–	
3	S_2, S_3	▼	▼	$+V_{dc}$	Q_1, S_3	–	–	$+V_{dc}/2$
4	Q_1, Q_2, Q_3, S_4	▲	▲	$-\frac{V_{dc}}{2}$	Q_2, Q_4	–	▲	$-\frac{V_{dc}}{4}$
					Q_3, S_4	–	▼	
5	S_1, S_4	▼	▼	$-V_{dc}$	Q_2, S_4	–	–	$-V_{dc}/2$

(b)



(c)

Fig. 6: New derivation of GaN-based 5L converter with DM functionality (a) the proposed DM-ANPC-5L converter using T-type and bidirectional PEBBs, (c) switching and capacitors states, (c) MVS rating of the devices in buck and boost operation modes.

$C_{oss}(V_{dc})$ as the voltage-dependent parasitic resistance and capacitance of a single device, the total semiconductor losses can be expressed as (1) [6]:

$$P_{semi} = I^2_{g,rms}\frac{R_{on}(V_{dc})}{A_{die}} + f_{sw}V^2_{dc}C_{oss}(V_{dc})A_{die}. \quad (1)$$

where, A_{die} is the die area of a given device. On the contrary, for such a $N+2$-level converter, the improvement of total losses can be stated by (2) as the device parasitics parameters highly depend on their stress voltage [6].

$$P_{semi} = I^2_{g,rms}\frac{R_{on}(\frac{V_{dc}}{N})}{A_{die}} + Nf_{sw}(\frac{V_{dc}}{N})^2C_{oss}(\frac{V_{dc}}{N})A_{die} \quad (2)$$

The performance of the proposed 5L dual T-type converter has also been verified using the PLECS and shown in Fig. 5. Here, the rated power is 3 kW, the input dc voltage is 400 V, while the size of output filter is only 1.2 mH with 25 kHz effective switching frequency to inject around 20 A maximum current to the grid. Thanks to the PS-PWM technique, the apparent switching frequency of the 5L output is 50 kHz resulting the same peak-to-peak ripple current across L_f as the 3L T-type converter. Lower capacitors ripple voltages compared to the 3L T-type counterpart and smooth waveform of the input current drown from the dc source with a dominated double-line frequency are the other important remarks taken from Fig. 5.

IV. Dual-Mode MLIs with Additional Bidirectional Devices

The proposed 5L dual T-type grid-connected in the previous section has been comprised of two standard T-cell branches with GaN-HEMTs. Even though its benefits to utilize a unity voltage conversion gain, its performance might be degraded when a wide varying input dc voltage, i.e., battery packs or PV modules with output terminal voltage of 400 V to 880 V is available. This comes from its static voltage gain as with large dc-link input voltage, i.e., more than 650 V, the stress voltage across the devices increases resulting the device failure.

The concept of dual-mode converter has already been proposed in [7] to fix such problem, when only by changing the modulation strategy and with a given topology, the operation mode of the converter can be changed from boost to buck mode and vice versa. Hence, when the dc-link voltage provided by PVs or batteries exceeds a limited range, the converter can give a half voltage conversion gain whilst generating the same number of output voltage levels with the same quality.

By adding two bidirectional devices with two extra dc-link capacitors as a front-end circuit to the proposed 5L dual T-type converter, such dual-mode functionality can be achieved. Details of such circuit with switching and capacitors states and the maximum voltage stress (MVS) over the devices are illustrated in Fig. 6. Herein, when the dc-link voltage is low, e.g., 400 V, the converter works in a boost operation mode with a switched-capacitor technique, while when the dc-link voltage is large, e.g., 800 V, the operation mode is changed to buck with a flying-capacitor (FC)-based technique. Details of the operation with the capacitors voltages of such converter can be seen from the PLECS simulation shown in Fig. 7. Considering M_{max} as the maximum modulation index, the

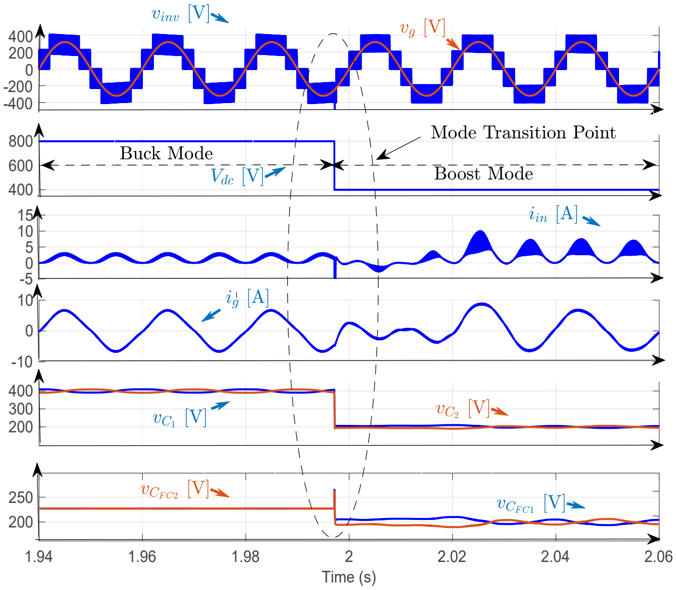


Fig. 7: Proposed dual-mode converter operation in boost and buck modes.

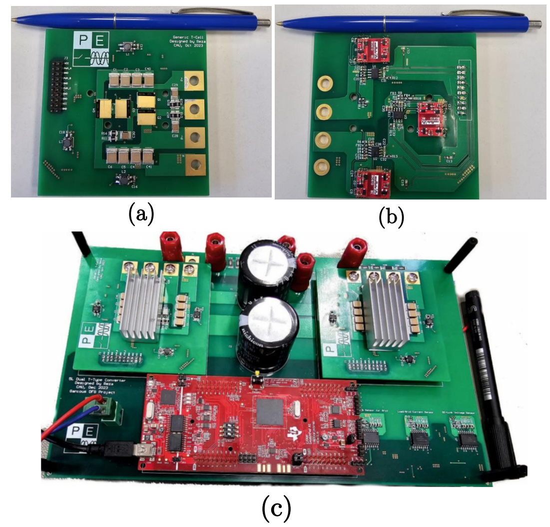


Fig. 8: A picture of the built prototype, (a) T-cell GaN-based branch (top-side), (b) T-cell GaN-based branch (bottom-side), (c) the resultant prototype of the proposed 5L dual T-type converter (Rated power: 3 kW, Power Density including the fan, heatsink and control board: 1.92 (kW/L)).

TABLE II: Main parameters used for the experimental prototype

Element	Type and Description
Power Switches	GS66516T
Microprocessor	DSP-TMS320F28379D
Switching Frequency/Rated Power	25 kHz(Effective)/ 3 kW
C_1, C_2,	0.47 mF/450 V
Gate Drivers	SI8271AB
Isolated dc/dc Converters	MGN1D050603MC-R7
HF Capacitors (220nF/1kV)	Multilayer Ceramic Capacitors

maximum voltage of the inverter, and the relationships of the capacitors voltages can be expressed as:

$$v_{inv} = \begin{cases} M_{max}V_{dc}, & \text{for boost mode} \\ 0.5M_{max}V_{dc}, & \text{for buck mode} \end{cases} \tag{3}$$

$$v_{FC1} \& v_{FC2} = \begin{cases} 0.5V_{dc}, & \text{for boost mode} \\ 0.25V_{dc}, & \text{for buck mode} \end{cases} \tag{4}$$

V. Experimental Results

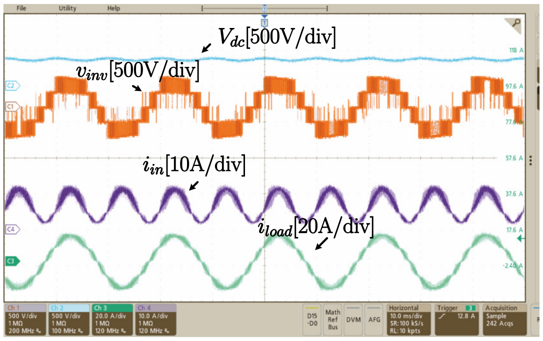
The 5L dual T-type converter shown in Fig. 3(a) with 650 V GaN-HEMTs devices is fabricated to develop the experimental results. Each of the dedicated T-cell branches is designed in a four-layer PCB with auxiliary gate driver circuit in the bottom side as depicted in Fig. 8(a) and (b), while a mother board depicted in Fig. 8(c) including the sensor board, heatsink, and DSP is designed to place two T-cell branches with dc-link capacitors within a compact area. Details of the components/parameters used for such experimental prototype designed for 3 kW power ratio and 1.92 (kW/L) power density are tabulated in Table II.

Applying a 400 V input voltage, the steady-state results of the resultant system showing the input dc voltage, the 5L output waveforms, the input current and the load current at 2.8 kW power are shown in Fig. 9(a). Following this, the balanced voltage of the dc-link capacitors and the voltage stresses over the bidirectional devices are given in Fig. 9(b) and (c). As can be seen, 650 V GaN-HEMTs are quite suitable for such a 5L dual T-Type converter with full dc-link voltage utilization at the ac output. The measured efficiency of the system at the rated power was around 99.2%, which shows almost similar performance as the conventional T-type converter with half dc-link utilization factor at the ac side.

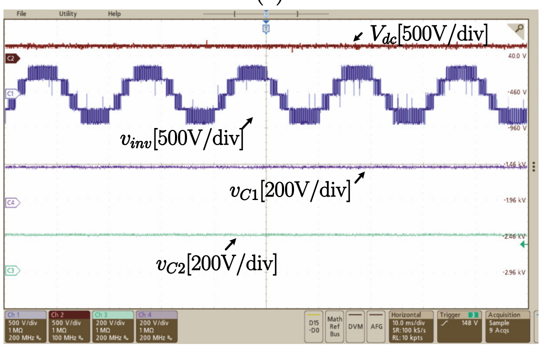
The dynamic performance of the proposed converter from 50% of rated power to full rated power can also be verified through Fig. 10(a), while a step change from 0.6 to 0.95 in maximum modulation index of the PS-PWM technique is applied in a DSP. The results show a perfect match with the simulation given in Fig. 6. The last experiment shown in Fig. 10(b) is also related to the dynamic response of the converter when suddenly it is connected to 400 V input voltage with a fast ramp trend under 1.35 kW loading condition. Double line frequency of the input current and nearly sinusoidal waveform of the load current with a 5L inverter output voltage can clearly be confirmed through these results.

VI. Conclusion

Application of GaN-HEMTs devices in conventional single-phase 3L mid point-clamped-based converters, i.e., T-type or ANPC converters, is restricted due to available chip packages of the devices with 650 V blocking voltage capability. The reason behind this is due to half dc-link voltage utilization of these converters, which requires 800 V input dc voltage to feed a 230 V rms grid voltage. Such shortcoming can be obviated using the concept of additional T-cell branch, where it can be integrated as a front-end active circuit to the conventional single-phase T-type or ANPC-based converters to achieve full



(a)



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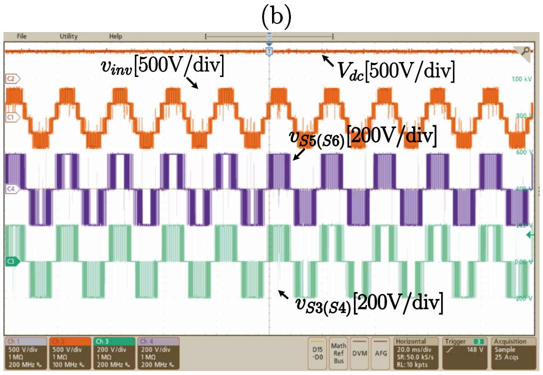
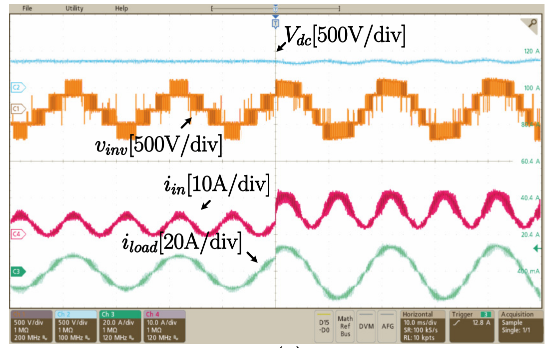


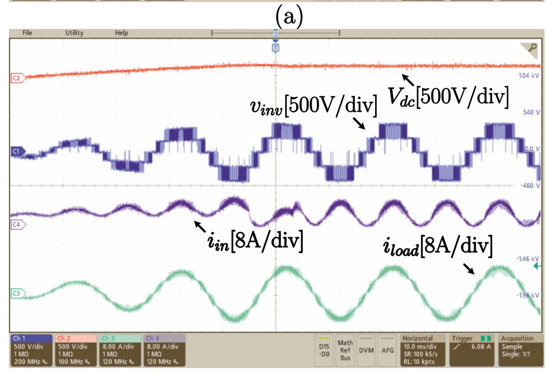
(c)

Fig. 9: Experimental results at the steady state 2.8 kW power showing 5L inverter output voltage and the input dc voltage with (a) the input and the load currents, (b) voltage stress across capacitors, and (c) voltage across bidirectional devices.

dc-link utilization at their ac output with a multilevel stair case waveform. Hence, utilization of commercially available 650 V GaN-HEMTs is possible with almost the same performance from the overall efficiency viewpoint as the conventional 3L WBG-based T-type/ANPC converters. Owing to possibility of applying PS-PWM in these circuits, the output filter size of the new converters can also be reduced with a reduction in effective switching frequency of the devices. The proposed solution can further be extended by utilizing front-end bidirectional devices as the resultant system offers a dual-mode operation suitable for wide varying input dc voltage resources with a 5L output voltage waveform. The proposed circuit operation with a 3 kW experimental prototype for a new 5L dual T-type converter are given to verify the correctness of the proposed solution.



(a)



(b)

Fig. 10: Experimental results in dynamic condition showing 5L inverter output voltage, the input dc voltage and the input and load currents (a) from 50% of rated power to the full rated power, (b) at the start-up condition from zero to the full dc-link voltage.

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