A New Common Ground Single-Phase Transformerless Five-Level Inverter for Photovoltaic Applications

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***Abstract*—The paper presents a new common ground single-phase transformerless five-level inverter for Photovoltaic (PV) applications. The topology is built with a minimum of six switches and three capacitors compared to various five-level inverter proposed in the literature and has the advantage of 100% dc-link utilization. The topology has the capability to supply both real power and reactive power. In order to achieve this, a simple level-shifted pulse width modulation scheme is used and proportional-resonant (PR) controller is developed to study the dynamic response of the system under input voltage as well as grid current changes. The performance of the proposed topology and their control scheme is validated through MATLAB simulation results. Finally, a detailed comparison is made with the recent five-level inverter topologies to highlight the merits of the proposed topology.**

***Index Terms*—five-level inverter, real power and reactive power, PR controller, Pulse width modulation.**

I. Introduction

Ever increasing demands on power generations, depleting nature of fossil fuels and rising global environmental pollution concerns inspire renewable energy-based power generations using wind energy, fuel cell and photovoltaic cells etc. Among these photovoltaic is a popular one and gaining attention in recent years due to drastic reduction in initial investment and better performance of PV panels. However, development of power electronic interface plays a major role in feeding power from PV panels into the load. This can be done by either single-stage direct DC/AC inverter operation or two-stage system consisting of a DC/DC boost stage between the PV and the inverter. In most of the cases, the two-stage system records poor efficiency compared to single-stage system due to more component count. On the other hand, leakage current is an important concern due to the flow of current through parasitic components between the PV panels and the grid [1]-[3]. Therefore, recent research has focused on trasformerless PV inverters with common ground to eliminate the issue due to common mode voltage and the flow of leakage current and avoid bulky transformers which increase the size and cost. In contrast to two-level operations, multilevel inverters are gaining attention even for low power applications due to their merits of reduced voltage stress across the device, low electromagnetic interference (EMI) and better quality of output voltage waveform with low total harmonic distortion(THD). The traditional neutral point-clamped (NPC) and half-bridge topologies are popular for industrial applications and capable to clamp common mode voltage(CMV) and minimize the filter. However, they suffer due to half utilization of dc source [3], [4]. Therefore, utilization of dc-link voltage is also a major concern to improve the overall performance of the system.

In view of the above shortcomings, considerable research has been carried out in the recent past for single-phase transformerless five-level inverters with reduced device counts, low leakage current and higher efficiency. Most of topologies are designed with common ground feature to eliminate the issue of leakage current with reduced components [5]-[12]. The topology based on switched capacitors has inherent boosting capability based on the modular nature [5]. But the devices used in these topologies are restricted to maximum peak inverse voltage of 1.5, which shows that they are not capable for a wide range of dc variations from the PV panels. Some of the authors proposed additional boost stage in the front-end [7]. However, these will be treated as a two-stage operation which leads to more cost.

From the literature, it can be noticed that each topology has its own merits and demerits. Therefore, for a wide range of operations, this paper aims at devising common ground single-phase five-level inverter for PV applications with reduced components. The salient features are:

1) Inherently self-voltage balancing capability leads to simple pulse width modulation operation.
2) Common ground eliminates the issue of leakage current problem.
3) Maximum of three switches in operation improves the overall efficiency of the system.
4) A simple closed-loop PR controller is proposed with real and reactive power capability.

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The complete operation and different states of voltage generations are described in section II. In addition, the logic for firing pulse generation using level-shifted pulse width modulation (LS-PWM) and the design of closed loop PR controller is also presented. The dynamic performance of the system under a wide range of input variations and load current changes are presented in section III. In section IV a comprehensive comparison of various five-level inverters is presented. Finally, section V offers recommendations.

II. Proposed Topology

Fig. 1 shows the proposed single-phase transformer less five-level inverter for PV applications. It consists of only six switching devices and three capacitors with inherent capacitor voltage balancing capability. In addition, the common grounding between the PV panels and the grid eliminates the issues of leakage current due to parasitic capacitance between PV panels and the ground which results in zero CMV. Here, switches S_1 to S_4 can be built easily with two simple H-bridge circuits and are able to handle higher power density as per industrial needs. The proposed topology can be operated in five distinct switching states as shown in Fig. 2. Table I illustrates this, and the various level generations and their description are as follows.

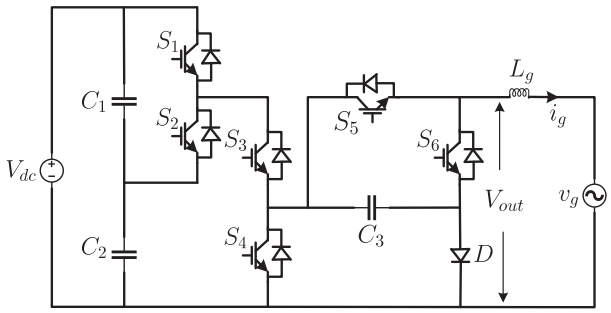

Fig. 1. Single-phase transformerless five-level inverter with common ground.

TABLE I
Switching States for Five-Level Output Voltage Waveform

Level	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	1	0	1	0	1	0
$V_{dc}/2$	0	1	1	0	1	0
0	0	0	0	1	1	0
$-V_{dc}/2$	0	1	1	0	0	1
$-V_{dc}$	0	0	0	1	0	1

A. Switching States Operation

The different switching states of the proposed topology are given below:

1) *State A*: During this state the input voltage is directly connected to the grid by turning on devices S_1, S_3 *and* S_5 and to generate maximum output voltage V_{out}=V_{dc} as shown in Fig. 2(a). During this condition the capacitor C_3 is floating and charges equal to the input voltage.

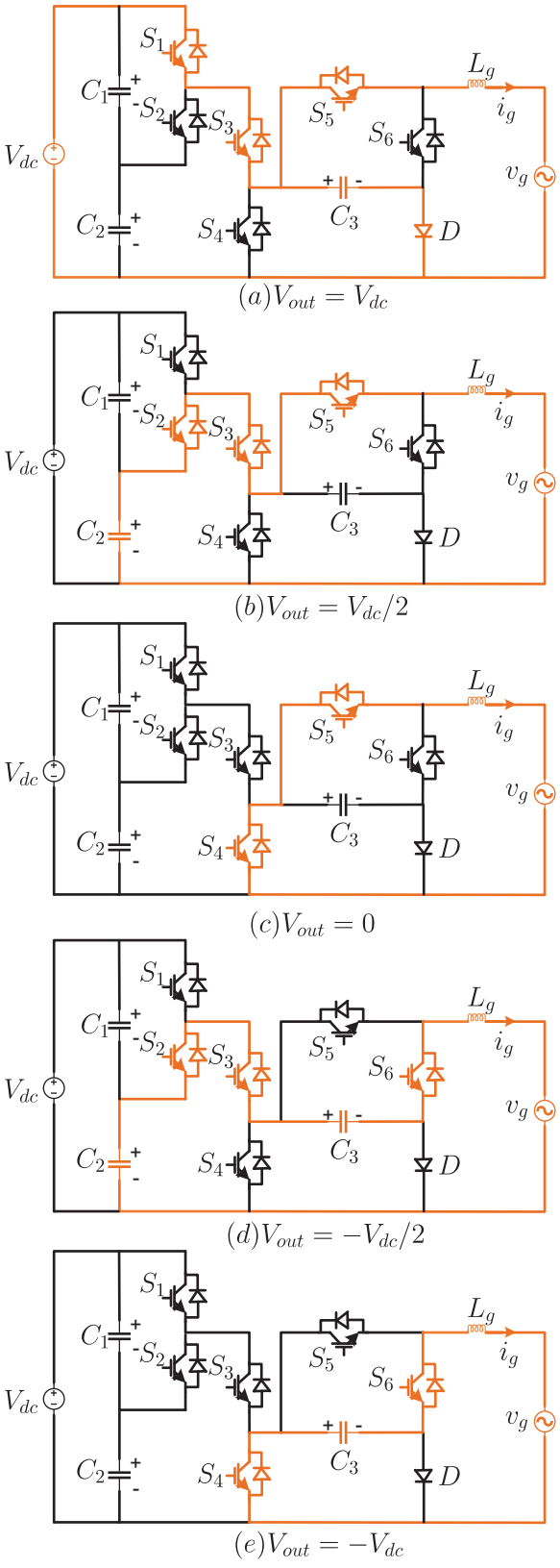

Fig. 2. Different switching states and the correspond current directions for output voltage generations.

2) *State B*: In this state, devices S_2, S_3 *and* S_5 are turned on to produce the output of the inverter which is equal to half the dc input where $V_{out}=V_{dc}/2$, as shown in Fig. 2(b).

3) *State C*: In this state, devices S_4 *and* S_5 are only triggered such that there is no power flow from the source and the capacitors. It seems that the output voltage is synthesized to zero voltage such that $V_{out}=0$, as shown in Fig. 2(c).

4) *State D*: During this state, capacitors C_2 *and* C_3 are connected in series in such a way that they produce half of negative output voltage by triggering devices S_2, S_3 *and* S_6. It can be noted that output is equal to $V_{out}=(V_{dc}/2-V_{dc})=-V_{dc}/2$, as shown in Fig. 2(d).

5) *State E*: Finally, switches S_4 *and* S_6 are triggered to produce the input voltage which is equal to the output voltage with the help of capacitor C_3 to synthesize $V_{out}=-V_{dc}$ as shown in Fig.2(e). During this state, C_3 supplies the load current and the remaining capacitors C_1 *and* C_2 are just floating and charges to V_{dc}.

Finally, it can be noticed that the need of blocking voltage of each device is a major concern in the development of topology in recent years to reduce the power loss and cost of the system. The proposed topologies demands four switches S_1, S_2 & S_4 to generate half of the input dc-link voltage and the devices S_3, S_5 & S_6 need to block full dc-link voltage. Moreover, it can be observed that a maximum of 3 devices is only in conduction which will increase overall efficiency of the proposed system.

B. Pulse Width Modulation Scheme

In this work, a simple level-shifted pulse width modulation scheme is implemented, as shown in Fig. 3. It consists of four carriers and one sinusoidal fundamental voltage waveform to produce output voltages in the range of V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$ & $-V_{dc}$. Simple logic gates are used to realize the five-level output voltage waveform to generate the switching signals as shown in Fig. 3.

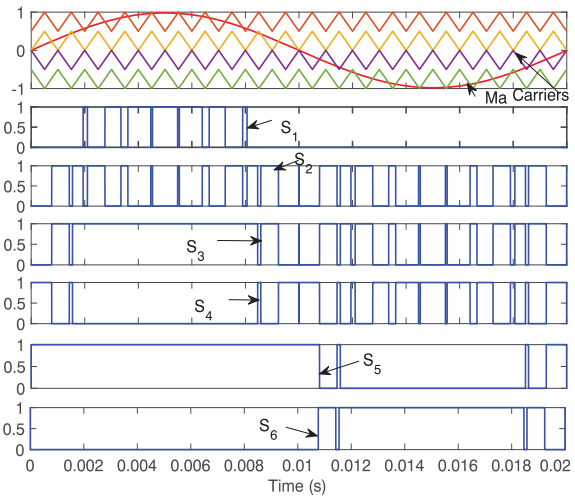

Fig. 3. Level-shifted pulse width modulation and the switching signal for each device S_1 to S_6.

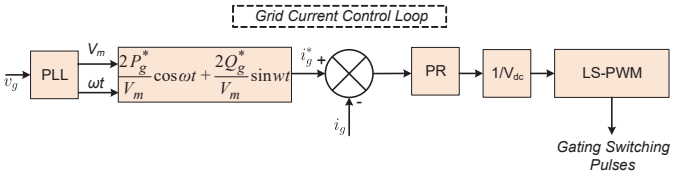

Fig. 4. Grid current control loop with PR controller.

C. Resonant Current Controller Design

In modern days, the development of proper control scheme is also very important for the sake of simplicity, easy implementation, and quick transient response. Owing to the above, in this work a simple PR current controller is implemented without involving any complexity in the controller like fuzzy, neuro or other optimization techniques-based controllers. Fig. 4 shows a simple PR controller which consists of a reference current generator and feedback from grid current to process the error through PR controller. The reference current is computed based on the requirement of real power and reactive power using equation 1.

$$i_g^* = \frac{2P_g^*}{V_m}\cos\omega t \pm \frac{2Q_g^*}{V_m}\sin\omega t \tag{1}$$

Simple phase-locked loop (PLL) is used to generate the reference ωt and V_m to compute the reference current i_{g^*}. This is compared with the actual measured grid current and the modulated sinusoidal output waveform to produce the desired grid current. One advantage of the PR controller is that it is capable of producing a fast transient response. A simple PR controller expression is used for the study to remove the steady-state error in the output waveform as given in [13].

$$G_{PR}(S) = K_p + \frac{K_i S}{S^2+\omega_0^2} \tag{2}$$

Moreover, the tuning of PR parameters K_p *and* K_i are done based on the procedure adopted in ref. [14].

III. Simulation Results

In this section, the simulation work is carried out in MATLAB software to study the performance of the proposed single-phase transformerless five-level inverter. The parameters used for the simulation are as follows; Input dc voltage (V_{dc})=400V, Grid voltage (v_g)=230V rms, Switching frequency (fs)=5kHz, and the fundamental sinusoidal supply frequency (f)=50Hz. Simple level-shifted pulse width modulation is implemented to realize the five-level output voltage waveform. First, the proposed topology is tested for input voltage changes from 400V to 500V for a constant load of 1 kW power, the corresponding measured inverter output voltage, grid voltage and grid current are shown in Fig. 5. It is noticed that as the input voltage rises, the magnitude of inverter output voltage and the grid current are increasing. In addition, the grid current is injected at unity power factor whereas both grid voltage and grid current is in phase as shown in Fig. 6.

TABLE II
COMPARISON OF VARIOUS FIVE-LEVEL PV INVERTERS (CGIS) WITH FULL DC UTILIZATION AND SOFT CHARGING CAPABILITY

TLI	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	**Proposed**
Switches	8	7	9	10	7	8	8	8	6
Diodes	0	0	0	0	2	2	0	0	1
Capacitors	4	3	3	2	2	4	2	3	3
Inductors	1	3	2	2	0	0	0	0	1

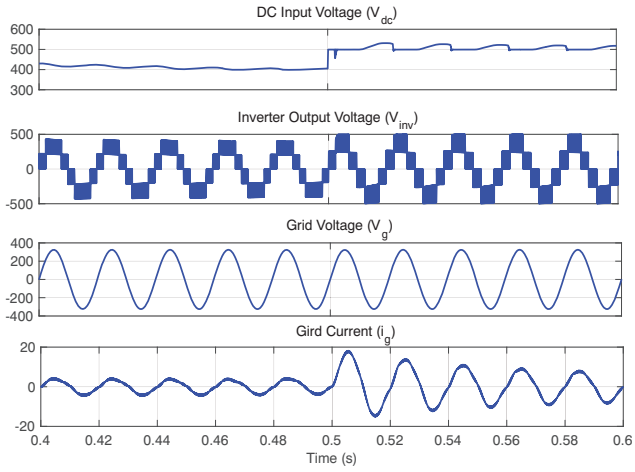

Fig. 5. Response of inverter output voltages, grid voltage and grid current during input voltage changes.

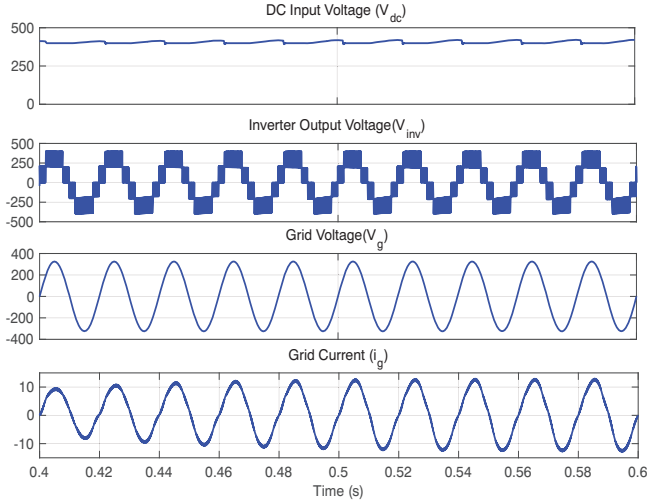

Fig. 6. Response of inverter output voltages, grid voltage and grid current at P=1 kW.

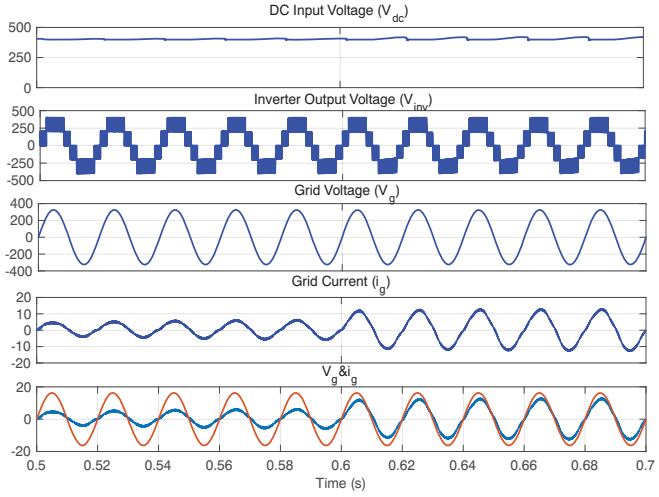

Fig. 7. Response of inverter output voltages, grid voltage and grid current during load changes from 1 kW to 2 kW.

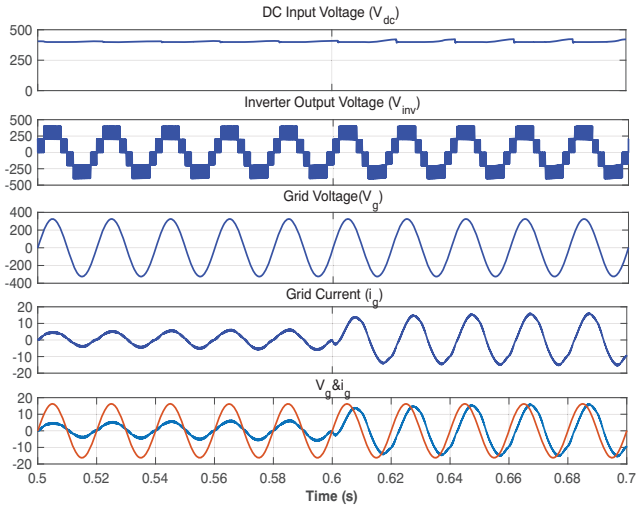

Fig. 8. Response of inverter output voltages, grid voltage and grid current during load changes from 1kW to (2+j1.5) kW.

Fig. 7 illustrates the response of inverter output voltage, grid voltage and their corresponding changes in grid current for load changes from 1 kW to 2 kW. Similarly, Fig. 8 shows the response of the inverter for load changes from UPF to lagging PF. It can be noticed that the PR controller is well regulated the injected grid current as per the reference current. This shows the developed controller is capable of providing fast transient response. Moreover, the proposed topology eliminates leakage current due to zero common mode voltage which is an added advantage. Finally, the proposed topology is most preferred for PV applications.

IV. COMPARATIVE ANALYSIS

Table II shows a precise comparison of various transformerless five-level inverter in terms of components, dc-link utilization, leakage current and common grounding features.

It is well noted that the number of devices and gate drivers is an important parameter that determines the compactness and cost of the inverter. The proposed topology has least switching devices compared to other five-level topologies mentioned in [5]-[12]. Some of the topologies don't require diodes, while the number of capacitors is higher. One of the critical requirements is that the selection of capacitors in most of the inverters should have low ripple and handle higher power density. Moreover, the number of devices in conduction is another criterion as a maximum of 3 devices made in conduction is an advantage of the proposed topology.

V. Conclusion

This paper presents a new single-phase common ground five-level transformer less inverter for PV applications. The proposed topology has a maximum of six switches compared to other five-level topologies in the recent literature, and this results in a reduction in size and cost, leading to higher efficiency. The proposed topology uses 100% dc input and has soft charging capability. Moreover, the topology is capable of providing reactive power support and alleviates the issue of leakage current problem due to common grounding between the PV and grid. It is evident that the proposed topology is most preferred for PV applications.

References

[1] W.J. Cha, K.T. Kim, Y.W. Cho, S.H. Lee, and B.H. Kwon, "Evaluation and analysis of transformerless photovoltaic inverter topology for efficiency improvement and reduction of leakage current," *IET Power Electronics*, vol. 8, no. 2, pp. 255–267, 2015.

[2] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes, and F. Blaabjerg, "Transformerless inverter topologies for single-phase photovoltaic systems: A comparative review," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 805–835, 2019.

[3] K. S. Kumar, A. Kirubakaran, and N. Subrahmanyam, "Bidirectional Clamping-Based H5, HERIC, and H6 Transformerless Inverter Topologies With Reactive Power Capability," *IEEE Transactions on Industry Applications*, vol. 56, no. 5, pp. 5119–5128, 2020.

[4] J. F. Ardashir, M. Gasemi, S. Peyghami, B. Rozmeh, and F. Blaabjerg, "A Novel Five-Level Transformer-less Inverter Topology with Common-Ground for Grid-Tied PV Applications," *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, 2021, pp. 1-10.

[5] S. S. Neti, V. Singh, S. Pattnaik, and V. Anand, "Common-Ground Single-Stage Transformerless Inverter using Switched-Capacitor for Single Phase PV Application," *2023 IEEE IAS Global Conference on Renewable Energy and Hydrogen Technologies (GlobConHT)*, Male, Maldives, 2023, pp. 1-7.

[6] V. Anand, V. Singh, J. Sathik, and D. Almakhles, "Single-stage Five-level Common Ground Transformerless Inverter with Extendable Structure for Centralized Photovoltaics," *in CSEE Journal of Power and Energy Systems*, vol. 9, no. 1, pp. 37-49, January 2023.

[7] R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, Y. P. Siwakoti, and S. S. Lee, "Switched-Boost Common-Ground Five-Level (SBCG5L) Grid-Connected Inverter With Single-Stage Dynamic Voltage Boosting Concept," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, Vancouver, BC, Canada, 2021, pp. 1014-1019.

[8] J. S. Mohamed Ali, A. Hota, N. Sandeep, and D. J. Almakhles, "A Single-Stage Common Ground-Type Transformerless Five-Level Inverter Topology," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 1, pp. 837-845, Feb. 2022.

[9] M. J. Sathik, N. Sandeep, D. J. Almakhles, and U. R. Yaragatti, "A Five-Level Boosting Inverter for PV Application," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 5016–5025, Aug. 2021.

[10] S. Dhara, A. Hota, S. Jain, and V. Agarwal, "A Transformerless 1-phase, 5-Level Half-Bridge PV inverter Configuration Based on Switched-Capacitor Technique," *IEEE Transactions on Industry Applications*, vol. 57, no. 2, pp. 1619–1628, Mar./Apr. 2021.

[11] A. Kadam, and A. Shukla, "A Multilevel Transformerless Inverter Employing Ground Connection Between PV Negative Terminal and Grid Neutral Point," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8897–8907, Nov. 2017.

[12] F. B. Grigoletto, "Five-Level Transformerless Inverter for Single-Phase Solar Photovoltaic Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 3411–3422, Dec. 2020.

[13] M. Parvez, M. F. M. Elias, and N. A. Rahim, "Performance analysis of PR current controller for single-phase inverters," *4th IET Clean Energy and Technology Conference (CEAT 2016)*, Kuala Lumpur, Malaysia, 2016, pp. 1-8.

[14] R. P. Aguilera, P. Acuna, G. Konstantinou, S. Vazquez, and J. I. Leon, "Basic control principles in power electronics: Analog and digital control design," *in Control of Power Electronic Converters and Systems*. San Francisco, CA, USA: Academic, 2018, ch. 2, pp. 31–68.