2024 IEEE 4th International Conference on Sustainable Energy and Future Electric Transportation (SEFET) | 979-8-3503-8399-7/24/$31.00 ©2024 IEEE | DOI: 10.1109/SEFET61574.2024.10718212

A New Single-Phase Switched Capacitor Based Five-Level Inverter With 200% DC Utilization

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***Abstract*—This paper introduces a new single-phase switched capacitor-based five-level inverter tailored for renewable energy applications, offering 200% DC utilization. The topology utilizes switched capacitors (SCs) alongside a simple T-type converter and a half-bridge circuit, eliminating the need for additional sensors to balance capacitors due to its self-balancing capability. Furthermore, a mid-point clamping neutral is incorporated to reduce leakage current and common-mode voltage, particularly beneficial for photovoltaic applications. A straightforward level-shifted pulse width modulation (LS-PWM) technique enables the realization of the five-level output voltage waveform. To validate the proposed topology's effectiveness, MATLAB/Simulink-based results are presented for both steady-state and dynamic conditions. Additionally, a comprehensive comparison is conducted to highlight the advantages of the proposed topology over recent alternatives documented in the literature.**

***Index Terms*—Multilevel inverter, T-type inverter, Switched capacitor, Pulse width modulation.**

I. Introduction

The increasing interest in multilevel inverters in industries and academia is now common compared to two-level inverters for medium and high-power applications due to the merits of reduced voltage stress, low electromagnetic interference, low total harmonic distortion, and good quality of supply. Multilevel inverters positively use lower-rated devices, which leads to higher efficiency and lower size compared to two-level inverters. Traditional inverters such as neutral point-clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) are more popular. Among them, the mid-point clamped NPC inverter is widely preferred for various industrial applications[1], [2]. However, balancing of the DC-link and the need for a higher number of clamping diodes for higher levels increase the numbers and complexity in control, resulting in more losses and reduction in efficiency of the system. On the other hand, an FC-based multilevel inverter demands more capacitors and has issues with tracking the capacitor voltages, and pre-charging all the capacitors becomes complex. CHB overcomes all the limitations of NPC and FC-based multilevel inverters. However, it demands more independent DC sources for increased levels.

Recently, the benefits of multilevel inverters have been extended to low-power applications of renewable sources such as fuel cells and photovoltaic systems[3], [4]. In order to overcome the drawbacks of conventional topologies, numerous research studies have focused on reduced part count multilevel inverters with features that boost their output voltage, either through front-end converters or switched capacitor-based concepts. This approach results in increased output voltage with reduced voltage stress across the switches, leading to higher efficiency. Therefore, it presents an advantageous proposition for low-power renewable applications.

In [5], a quasi-Z-source-based single-phase T-type five-level inverter was proposed with a boosting feature. However, the output is determined by the impedance source network of inverters and their shoot-through period. In [6], a five-level boost inverter using ten switches and a flying capacitor with mid-point-neutral clamping feature is proposed. In [7], a reduced switch count six-switch and three-capacitor-based five-level inverter is presented as the boosting feature. A different approach to reducing device count with three DC sources has been proposed in [8] for five-level operation. This modular topology can be extended for higher-level output voltage generations. In [9], a flying capacitor-based five-level inverter has been presented to address the issue of leakage current in transformerless inverters. However, it demands eleven switches, and capacitor voltage balancing increases the complexity in control. In [10], a T-type five-level inverter with a front-end boost converter is proposed. Still, the inverter is buck in nature, and its output is determined by the front-end boost converter. The topology presented in [11] combines the features of both the switched capacitor concept and the front-end boost converter to realize the five-level output voltage waveform. It is evident that the above topologies require more switches and front-end boost converters to produce the desired output voltage. Additionally, the structure is neither unique nor compact and requires more passive components, raising concerns about the reliability of the inverter for grid-connected operations.

To address the limitations of requiring more DC sources and switches, this paper introduces a new single-phase five-level inverter tailored for grid-connected renewable applications. The proposed topology is constructed with a T-type

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circuit and features 200% DC utilization using a concept involving two switched capacitors. Section II elaborates on the complete operation of the proposed topology and its generation of five-level output voltage. Section III showcases MATLAB/Simulink-based simulation results under both steady-state and dynamic conditions. A thorough comparison of various grid-connected five-level inverters is provided in Section IV. Finally, Section V concludes with remarks.

II. Proposed Topology

Fig. 1 depicts the proposed single-phase five-level inverter designed for grid-connected renewable applications. It is evident that the inverter consists of a mid-point-clamped T-type network and a single half-bridge circuit. Capacitors C_1 and C_2 serve as switched capacitors, eliminating the need for sensors or balancing circuits to charge them. The topology exhibits self-balancing charging capability during level generations. Furthermore, the structure is more compact and reliable compared to other topologies discussed in the previous section. For better comprehension, the complete operation of the inverter is delineated into five modes of operation, as illustrated in Fig. 2, and are as follows;

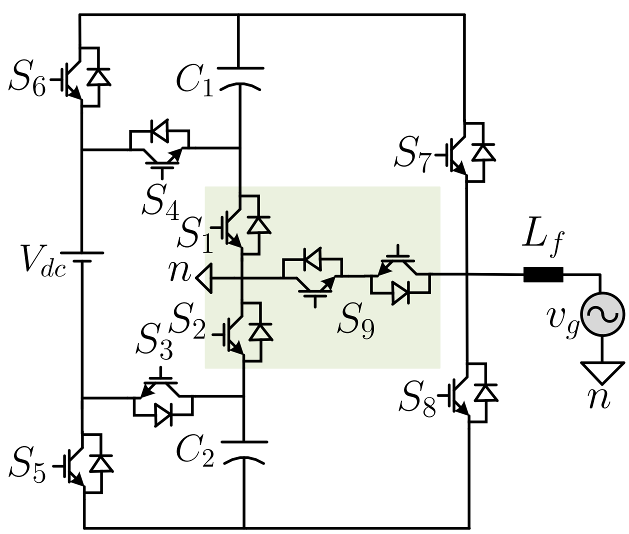

Fig. 1. Single-phase five-level inverter for grid-connected operation.

Mode 1: During this mode of operation, the output voltage V_o=+2V_{dc}. Switches S_2, S_3, S_4 & S_7 are conducting, and the output voltage is the sum of both the DC source V_{dc} and the capacitor voltage C_1.

Mode 2: During this mode of operation, the output voltage V_o=+V_{dc}. Switches S_2, S_3, S_6 & S_7 are conducting, and the output voltage is directly supplied from the DC source. During this period, capacitor C_1 is charged to the DC input voltage +V_{dc} by connecting it across the source through the activation of switch S_1.

Mode 3: During this mode of operation, the output voltage V_o=0. Only the bidirectional switches S_9 are in operation, with the mid-point clamping neutral directly shorted with the grid.

Mode 4: During this mode of operation, the output voltage V_o=-V_{dc}. Switches S_1, S_4, S_5 & S_8 are conducting, and the output voltage is directly supplied from the DC source. During this period, capacitor C_2 is charged to the DC input voltage -V_{dc} by connecting it across the source through the activation of switch S_2.

Mode 5: During this mode of operation, the output voltage V_o=-2V_{dc}. Switches S_1, S_3, S_4 & S_8 are conducting, and the output voltage is the sum of both the DC source -V_{dc} and the capacitor voltage C_2.

To realize the five-level output voltage waveform, a simple level-shifted pulse width modulation scheme (LS-PWM) is implemented, as depicted in Fig. 3. Four carriers and one fundamental sine waveform are compared to generate switching states for various levels of operation: +2V_{dc}, +V_{dc}, 0, -V_{dc} & -2V_{dc} as illustrated in Fig. 2. Furthermore, Table I highlights the switching sequence to generate the five-level output voltage waveform. In the table, a state of 0 signifies off, while 1 signifies on. Notably, in most modes of operation, the number of devices in conduction is less than half of the overall devices, demonstrating the topology's capability to operate at higher efficiency.

Additionally, a simple proportional resonant (PR) controller is implemented for grid-connected operation. The measured grid current, obtained with the assistance of a current sensor, is compared with the reference current, and the resulting error is processed through the PR controller to generate the modulating waveform (M_a), as depicted in Fig. 3. This modulating waveform is then compared with the carriers and processed through logic gates to produce the desired five-level output voltage waveform. One advantage of the PR controller is its capability to achieve a fast transient response. Furthermore, the tuning of the PR controller is carried out according to the procedure outlined in [12].

III. Simulation Results

In this section, a simulation study was conducted in the MATLAB/Simulink environment to demonstrate the operation of the proposed single-phase grid-connected five-level inverter. A DC source input voltage of 200V was selected to power the proposed topology, while a grid voltage of 230V_{rms} was assumed for the single-phase application. Initially, the performance of the topology was evaluated for varying loads ranging from 1 kW to (2+j1.5) kW.

Fig. 4 illustrates the measured waveforms of the five-level inverter output voltage, grid voltage, and their corresponding grid currents. It is evident that at 0.3 seconds, the injected current increased from approximately 7A to 15A during load changes, with the controller demonstrating rapid dynamics and settling within half a cycle. This underscores the effectiveness of the proposed PR controller for grid-connected operation. Furthermore, the inverter output reaches 400V, twice the DC source input considered for the study. This demonstrates that the switched capacitor-based five-level inverter is capable of operating at 200% DC utilization, presenting an additional advantage of the proposed topology.

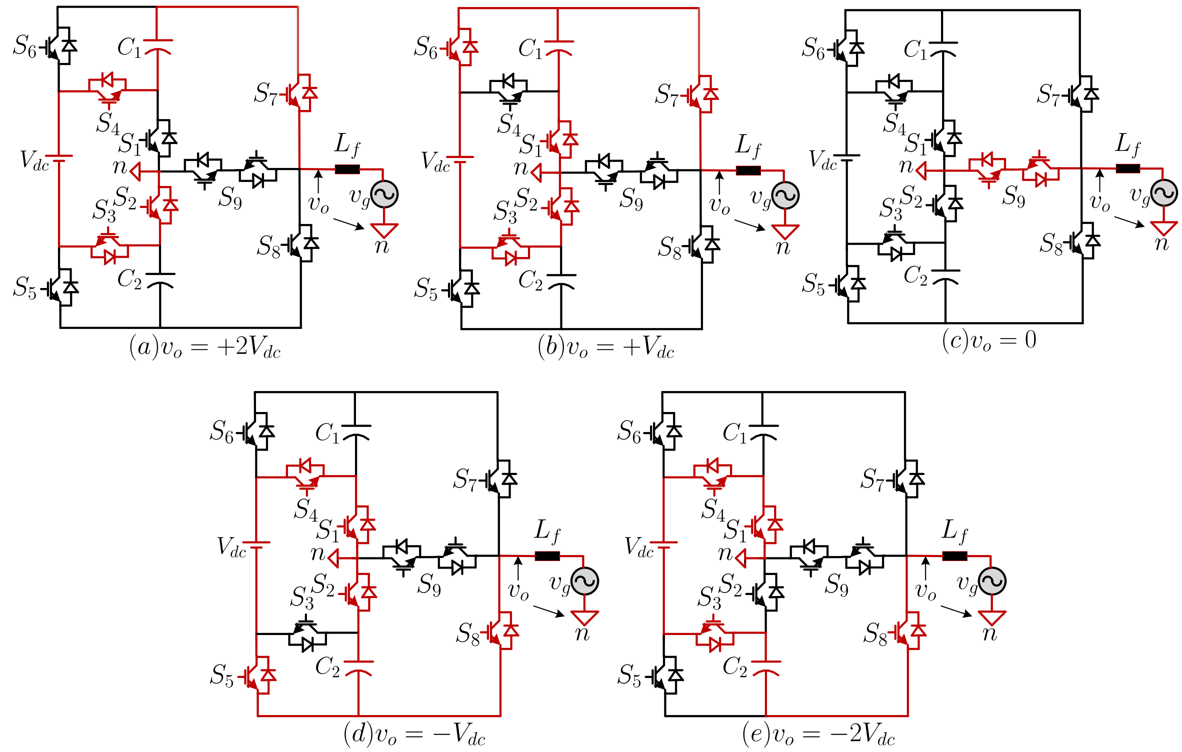

Fig. 2. Different modes of operation of five-level inverter.

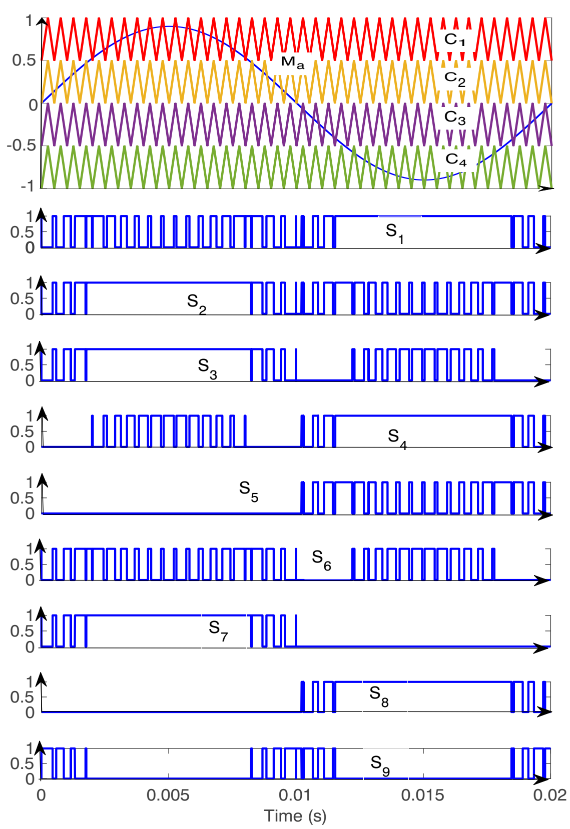

Fig. 3. Level-shifted pulse width modulation and the switching signal for each device S_1 to S_9.

In order to demonstrate the reactive power capability, the proposed topology was tested under different reference power conditions, including unity power factor, lagging power factor and leading power factor (PF). Fig. 5 depicts the response of the inverter output voltage, grid voltage, and their corresponding load current. It is evident that the current in phase (unity) with the voltage under resistive power lags the voltage under inductive power and leads the voltage under capacitive power. For better visibility, the current waveform is scaled up to 10 times. This highlights the superiority of the developed topology with the PR controller for grid-connected operations. Furthermore, Fig. 6 presents the measured voltage stress across the various switches. It can be observed that switches S_1 to S_6 experience a voltage level of 200V, while the maximum voltage across switches S_7 & S_8 is 600V, and switch S_9 is rated for a voltage of 400V. This demonstrates that most of the switches operate at reduced stress, showcasing an advantage of the proposed topology.

TABLE I
SWITCHING SEQUENCE FOR FIVE-LEVEL OUTPUT VOLTAGE WAVEFORM

Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
+2V_{dc}	0	1	1	1	0	0	1	0	0
+V_{dc}	1	1	1	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	1
-V_{dc}	1	1	0	1	1	0	0	1	0
-2V_{dc}	1	0	1	1	0	0	0	1	0

TABLE II
COMPARISON OF VARIOUS GRID-CONNECTED FIVE-LEVEL INVERTERS

Components	NPC	FC	CHB	[5]	[6]	[7]	[8]	[9]	[10]	[11]	Proposed
DC Sources	1	1	2	1	1	1	3	1	1	1	1
Swtiches	8	8	8	10	10	6	9	11	8	9	10
Divided Capacitors	2	4	2	0	0	0	0	0	2	0	0
Capacitors	0	6	0	2	1	3	0	3	0	2	2
Inductors	0	0	0	1	0	0	0	0	0	1	0
Diodes(excluding body diodes)	4	0	0	4	2	2	0	0	0	1	0
Drivers	8	8	8	10	10	6	9	11	8	9	9
Output Voltage	Buck	Buck	Buck	Buck/Boost	Boost	Boost	Buck	Buck	Buck	Boost	Boost

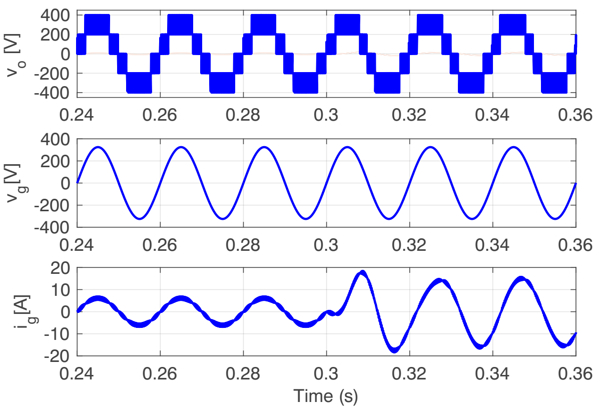

Fig. 4. Response of inverter output voltage, grid voltage and load currents.

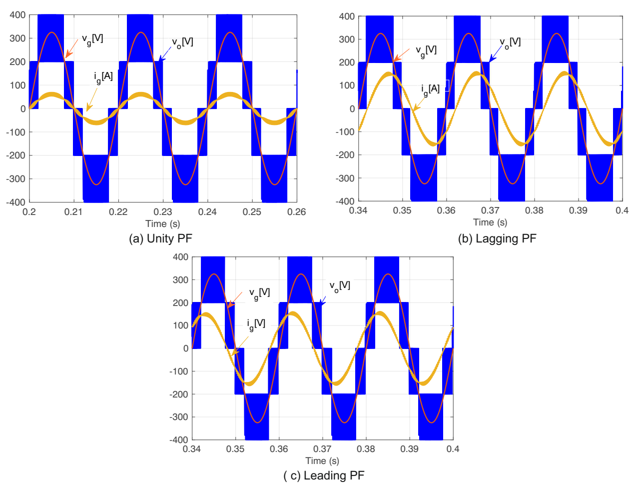

Fig. 5. Response of inverter output voltage, grid voltage and load currents during load changes under (a) Unity PF, (b) Lagging PF & (c) Leading PF.

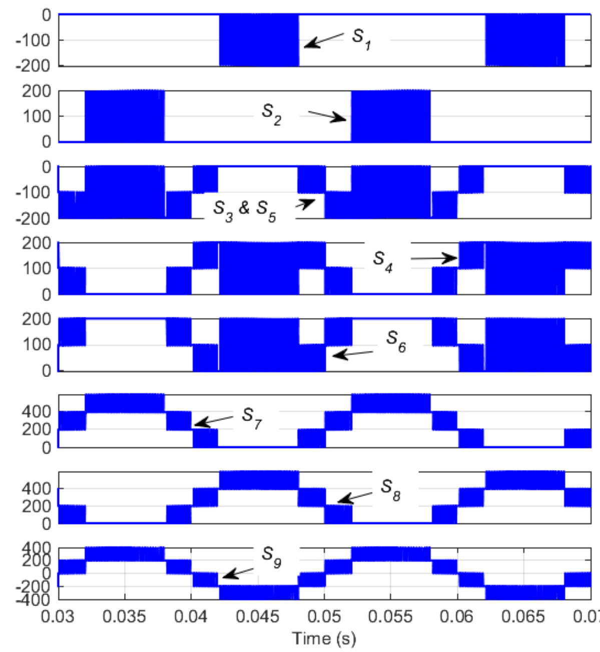

Fig. 6. Voltage stress across the switches

IV. COMPARATIVE ANALYSIS

In this section, a detailed comparison of various grid-connected five-level inverter topologies is conducted to demonstrate the merits of the proposed topology. Table II presents a comparison of well-known and commonly used five-level inverters such as NPC, FC, and CHB, alongside various five-level inverters proposed in recent years [5]-[11]. It is evident that the proposed topology is simple, compact, and requires only a single DC source compared to CHB and other references [8]. Most of the recently proposed topologies demand more devices and driver circuits compared to the proposed topology. The topologies proposed in [8], [9], and [10] are buck in nature. The topology proposed in [7] is competitive with the proposed topology in terms of device counts. However, the structure and the control scheme become complex. The proposed topologies which employ a reliable T-type structure and one half-bridge circuit attest to the merit of the topology. Moreover, the boosting factor is also 2 times compared to the other topologies, which serves as proof of the unique and compact structure of the topology.

Indeed, the switched capacitor topologies have limitations such as voltage balancing, switching losses, and limited scalability. For example, if the DC source has a voltage rating of 200V and the topology is designed for a certain power rating, such as 1 kW or 5 kW, the capacity of the inverter would be limited by these ratings. However, these limitations can be overcome by the self-balancing capability of the proposed topology and optimized system design, resulting in higher efficiency.

V. Conclusion

A new single-phase five-level inverter for grid-connected renewable applications has been presented. The proposed topology has the advantages of being simple, compact, and utilizing 200% DC through the switched capacitor boosting concept. The complete operation of the proposed topology is described. Level-shifted PWM is implemented to produce the desired output voltage. Simulation was performed in MATLAB software, and the accuracy of the proposed topology was tested through simulation results. The proposed topology is capable of providing reactive power support. Finally, a detailed comparison is made to highlight the significance of the proposed five-level inverter in terms of devices, output voltage capability, and effectiveness of the structure.

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