2024 Third International Conference on Power, Control and Computing Technologies (ICPC2T)

A New Single-Phase Fault-Tolerant T-Type Five-Level Inverter with 100% DC Utilization

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***Abstract*—The paper presents a new single-phase fault-tolerant five-level inverter with 100% DC utilization. Self-balancing of dc capacitors with reduced device counts and compact T-type structure will enhance the overall reliability of the proposed topology. A simple half-bridge circuit with two additional semiconductor devices were added to the topology to obtain more redundant states which can support the five-level generation under most of the fault conditions. Moreover, the waveform quality and the power handling capability is ensured under various open/short circuit fault conditions of the proposed topology with the help of redundant switches and modified pulse width modulation scheme. Further, reduced device count and minimum number of conducing devices in each cycle ensure the highest efficiency with its counter parts. The proposed circuit is tested through MATLAB/Simulink environment for various open circuit fault conditions and the results are presented. Finally, a comprehensive comparison is made to highlight the merits of the proposed topology.**

***Index Terms*—Fault-tolerant, T-type structure, Multilevel inverter, switch faults, Pulse width modulation.**

I. Introduction

There is ever increasing interest in multilevel inverters (MLIs) because of their use in various industrial applications, renewable grid connected systems, aircraft, marine propulsion, FACTs, high voltage system etc. This is mainly due to their ability to produce output voltage close to sinusoidal waveforms at lower electromagnetic interface, low stress across the device and low total harmonic distortion (THD). The most well-known conventional MLIs are neutral point-clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). Achieving an output level depends on the number of devices and dc sources. However, for increase in levels, increasing device count increases the complexity of the circuit and the devices are highly prone to faults. It has been observed that 21% of the faults occur in devices and 13% in solders, and another survey reports that 38% of device failure is inclined to variable speed drive applications [1]. These results decrease in the reliability of the systems.

Recently, to address the above problem, numerous topologies with lower devices and fault-tolerant have been proposed by various researchers in [2]-[10]. The drawback of these topologies is a reduction in redundant switching states and low fault-tolerant capability with lower output level. To overcome the above drawbacks and increase the fault-tolerant capability, an additional redundant circuit is introduced in MLIs. A comprehensive review of various fault-tolerant MLIs is given [2] with the features of uninterrupted power supply to loads, better efficiency, lower components and lower cost. It is shown that fault tolerance has been done based on solutions of either switch's addition, leg addition, modular replacement or parallel redundant inverter. This paper addresses most of the cases of additional switches and redundant based topologies. It can be noticed that most of the topology's structure is complex and more devices are in operation to produce five-level, seven-level and nine-level output voltage waveforms [3]. In [4], a fault-tolerant MLI for single-phase five-level output voltage with the capability of a single switch and multiple switches is presented. However, it uses two dc sources and 12 switches, which include 4 additional switches for fault-tolerant operation. In [5], FC based single-phase MLI is proposed with a redundant leg which consists of 6 switches and can produce a full output rating with single dc source during single switch and multi-switch fault conditions. In [6] & [7], reduced switch count fault-tolerant MLI is proposed with full output power capability during single and multi-switch faults with two dc sources. The T-type based single-phase MLI with reduced device count and redundant leg is proposed with fault-tolerant capability in [8] & [9]. These topologies have a large number of component count and require two dc sources.

In order overcome the above limitations of more dc sources

This work was supported by the Science and Engineering Research Board under SIRE Fellowship Award SIR/2022/000864.

2024 Third International Conference on Power, Control and Computing Technologies (ICPC2T) | 979-8-3503-4920-7/24/$31.00 ©2024 IEEE | DOI: 10.1109/ICPC2T60072.2024.10474679

and more redundant switches, in this paper, a new single-phase fault-tolerant T-type five-level inverter is presented. The main advantages of the T-type structure are simplicity, modulator and one redundant leg which consists of a half-bridge converter to analyze the output voltage waveforms under one switch or multi-switch open circuit faults. The proposed topology is an added advantage as it can operate at 100% dc utilization with common mid-point neutral. Simple level-shifted pulse width is used to realize the five-level output voltage under healthy, during fault and post-fault conditions. The complete operation of the proposed topology is tested in MATLAB software and the results are presented. Moreover, a comprehensive comparison is made with recent topologies to highlight the merit of the proposed topology. Finally, concluding remarks are presented.

II. Proposed Fault-Tolerant Five-Level Inverter

A. Circuit Description

Fig.1 shows the proposed single-phase fault-tolerant T-type five-level inverter. The main circuit consists of two cascaded T-type inverters, two capacitors and a single dc source. Each T-type network has four switches and is capable of producing three-level output voltages. The cascading of the dual T-type network produces five-level output voltage waveform. The two capacitors are connected in series with self-balanced voltage of $V_{dc}/2$. It can be noticed that there is no requirement of additional passive components for boosting or the full utilization of dc-link voltage at the output voltage. Moreover, it requires 400V dc input compared to 800V in NPC based MLIs which reduces the rating of switching devices and passive components to half and this is an added advantage of the proposed topology. This results in reduced size, cost, higher efficiency, reliability and increased power density [11]. A simple one-leg H-bridge circuit is used in the redundant leg. The complete operation under healthy, during fault and post-fault conditions are as follows;

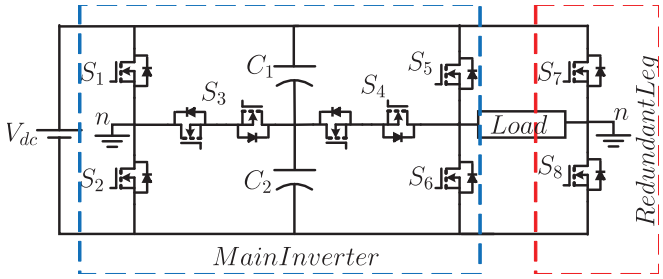

Fig. 1. Single-phase fault-tolerant T-type five-level inverter.

B. Working Principle

In this paper, a simple level-shifted pulse width modulation (LS-PWM) scheme is implemented to realize the five-level operation. Four carriers and one fundamental sine waveform are compared to generate switching states for various levels of operation V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$ & $-V_{dc}$ as shown in Fig. 2. Moreover, Table I highlights the switching sequence for various level generations which is useful for a quick understanding. The state 0 means off and 1 means on. It can be noticed that in most of the states the number device in conduction is less than half of the overall device, which demonstrates that the topology is capable of operating at higher efficiency.

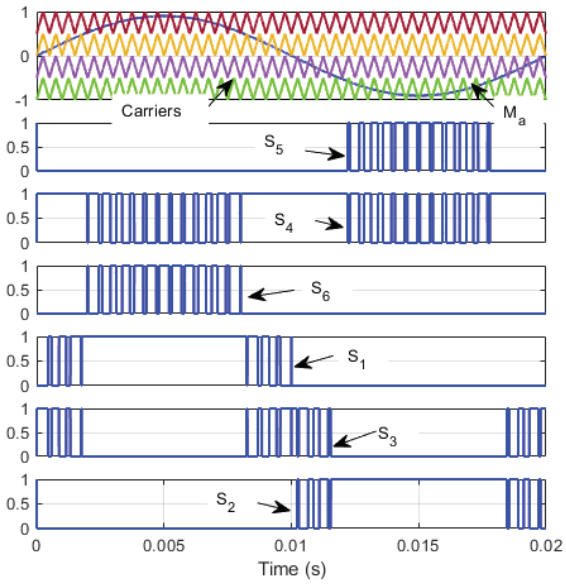

Fig. 2. LS-PWM for firing pulse generation.

TABLE I
Switching Sequence for Five-Level Output Voltage Waveform

Level	S_1	S_2	S_3	S_4	S_5	S_6
$+V_{dc}$	0	1	0	0	1	0
$+V_{dc}/2$	0	0	1	0	1	0
0	0	0	1	1	0	0
$-V_{dc}/2$	0	0	1	0	0	1
$-V_{dc}$	1	0	0	0	0	1

* 0-OFF; 1-ON

In order to evolve the fault-tolerant capability, the proposed topology tests for a single switch open circuit faults of all switches independently. Fig. 3 shows the path for the direction of current and corresponding level generations under single-switch open circuit faults at S_1. It can be noticed from Fig. 3 that five-level output voltage is produced during an open circuit fault at S_1 and the output voltage switching sequence for all the switches under open circuit is given in Table II. It can be noticed that most of the times, five-level output voltage is produced and in some cases three-level output voltages are produced with the use of the redundant leg during single switch open circuit faults. Similarly, Table III gives the switching sequence and the corresponding output voltage level generation for different combinations of two switches under fault conditions. Except the worst of S_4 & S_5 *or* S_4 & S_6, either three-level or five-level output voltage can be generated by the proposed two-switch redundant leg

with full output power. One can observe that during the five-level operation the redundant switches are used for five-level output waveform. For the 3-level waveform, the modulated fundamental waveform is reduced to half to produce the V_{dc}, 0, & -V_{dc} in the proposed topology. Hence, the fault detection algorithm and the corresponding switch sequence selection is important to form the lookup table to operate the topology for the prescribed output voltage level generations.

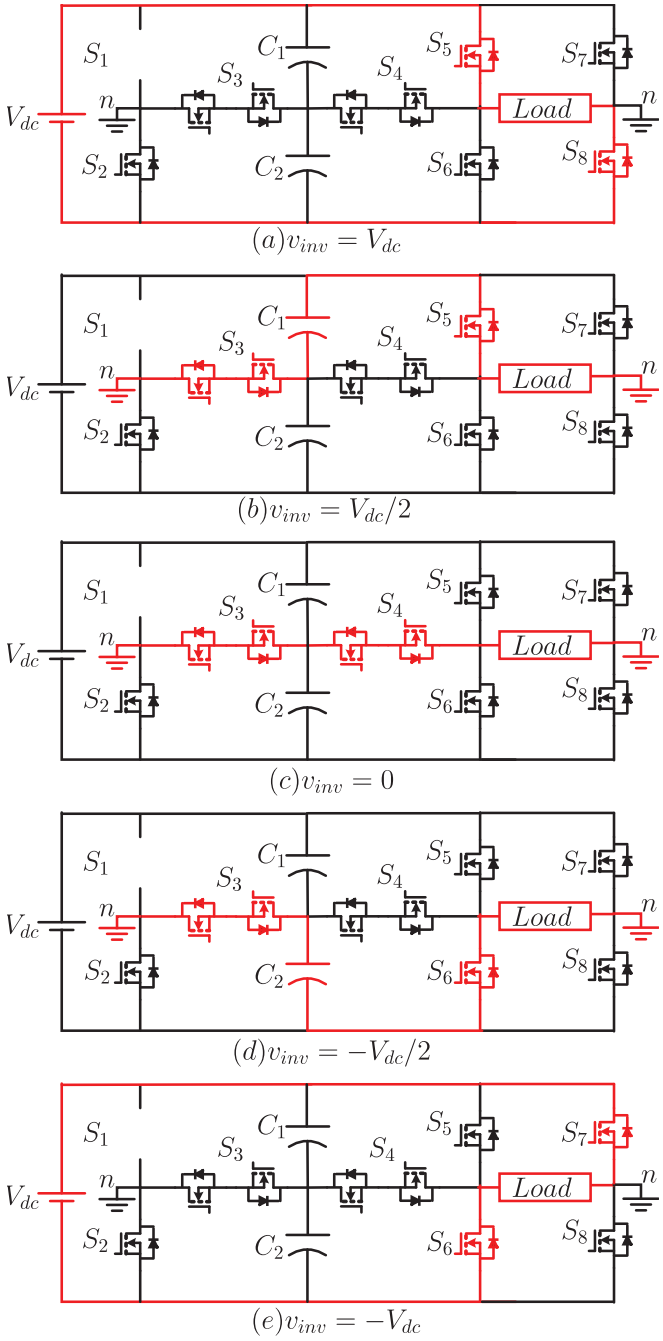

Fig. 3. Five-level output voltage generation under switch S_1 open circuit fault.

TABLE II
SWITCHING SEQUENCE FOR THE AVAILABLE OUTPUT LEVEL AFTER SINGLE SWITCHES FAULT

Faulty Switches	On state switches for specified output levels					Output Level
	$+V_{dc}$	$+V_{dc}/2$	**0**	$-V_{dc}/2$	$-V_{dc}$	
S_1	S_5, S_8	S_3, S_5	S_3, S_4	S_3, S_6	S_6, S_7	5-L
S_2	S_5, S_8	S_3, S_5	S_3, S_4	S_3, S_6	S_6, S_7	5-L
S_3	S_5, S_8	S_2, S_4	S_5, S_7	S_1, S_4	S_6, S_7	5-L
S_4	S_5, S_8	S_3, S_5	S_5, S_7	S_3, S_6	S_6, S_7	5-L
S_5	—	S_1, S_4	S_3, S_4	S_2, S_4	—	3-L
S_6	—	S_1, S_4	S_3, S_4	S_2, S_4	—	3-L

TABLE III
SWITCHING SEQUENCE FOR THE AVAILABLE OUTPUT LEVEL AFTER MULTIPLE SWITCHES FAULT

Multiple Faulty Switches	On state switches for specified output levels					Output Level
	$+V_{dc}$	$+V_{dc}/2$	**0**	$-V_{dc}/2$	$-V_{dc}$	
S_1, S_2	S_5, S_8	S_3, S_5	S_5, S_7	S_3, S_6	S_6, S_7	5-L
S_1, S_3	S_5, S_8	S_4, S_8	S_5, S_7	S_4, S_7	S_6, S_7	5-L
S_1, S_4	S_5, S_8	—	S_5, S_7	—	S_6, S_7	3-L
S_1, S_5	—	S_4, S_8	S_6, S_8	S_4, S_7	—	3-L
S_1, S_6	—	S_4, S_8	S_5, S_8	S_4, S_7	—	3-L
S_2, S_3	S_5, S_8	S_4, S_8	S_5, S_7	S_4, S_7	S_6, S_7	5-L
S_2, S_4	S_5, S_8	—	S_5, S_7	—	S_6, S_7	3-L
S_2, S_5	—	S_4, S_8	S_6, S_8	S_4, S_7	—	3-L
S_3, S_4	S_5, S_8	—	S_5, S_7	—	S_6, S_7	3-L
S_3, S_5	—	S_1, S_4	S_6, S_8	S_2, S_4	—	3-L
S_3, S_6	—	S_4, S_8	S_5, S_7	S_4, S_7	—	3-L
S_5, S_6	—	S_1, S_4	S_3, S_4	S_2, S_4	—	3-L
S_4, S_5	—	—	—	—	—	**
S_4, S_6	—	—	—	—	—	**

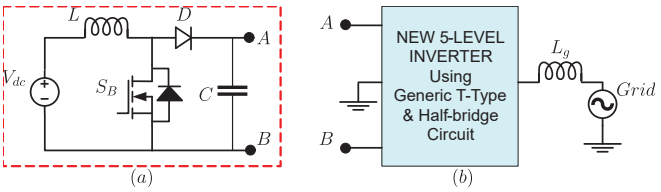

Fig. 4. Proposed topology with frond-end boost converter.

Moreover, from Table II & III, it can be understood that (highlighted in red colour), the three-level output voltage can be boosted to rated 400V during the above periods by regulating the dc input voltage with the use of a front-end DC/DC boost converter as shown in Fig. 4. This results in same output voltage/power can be achieved in all the states of operation during OC faults is an added advantage of the proposed five-Level inverter with generic T-type & Half-bridge circuit.

III. SIMULATION RESULTS

In order to verify the proposed fault-tolerant capability and to realize output voltage waveform, simulation work was carried out in MATLAB/Simulink environment. The study was performed for a switching frequency of 5 kHz and the modulating fundamental sine waveform of 50 Hz. V_{dc} of 400V

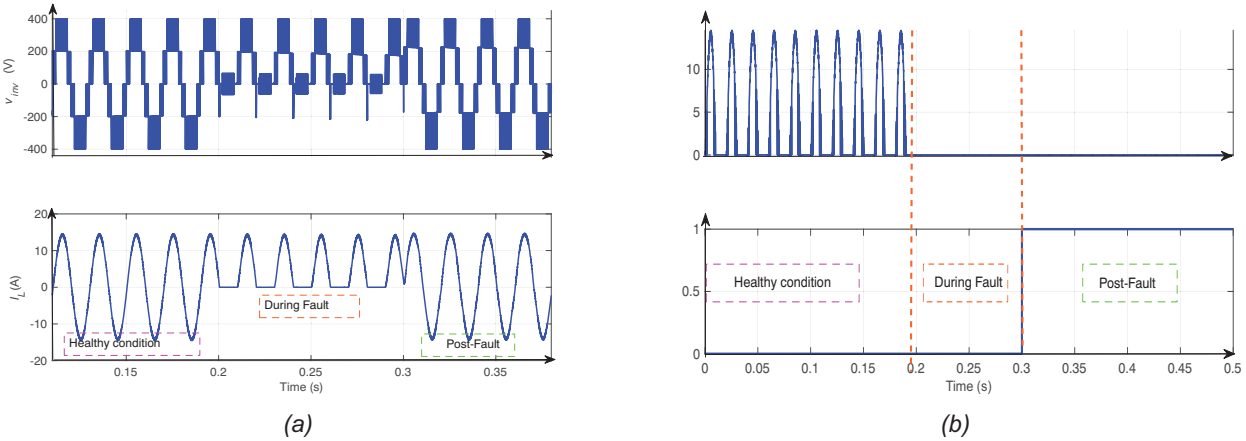

Fig. 5. Simulation results of inverter output voltage and load current during OC fault (a) S_1 (b) Current flowing through switch S_1 and transition period.

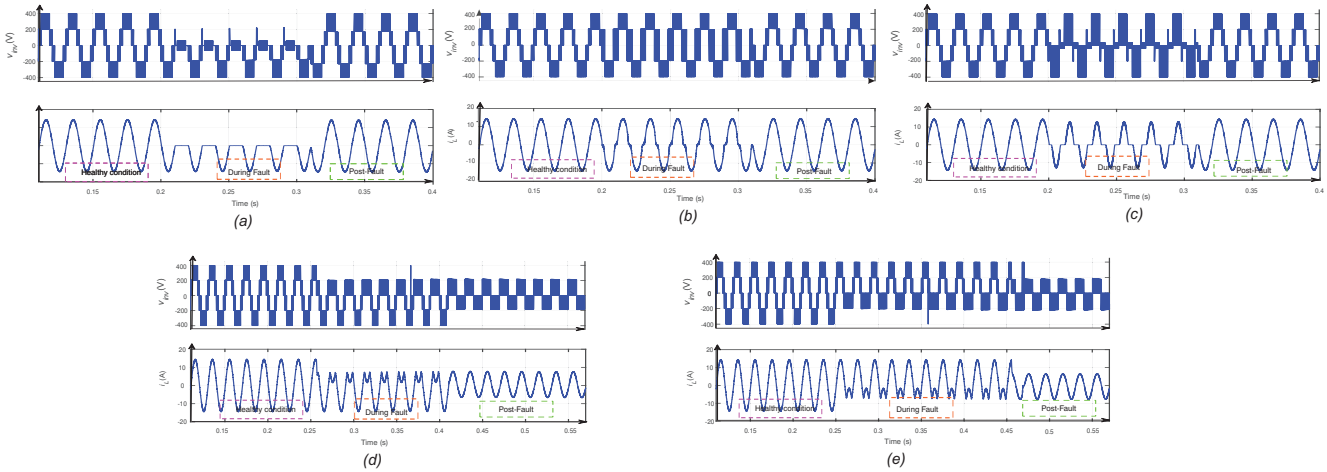

Fig. 6. Simulation results of inverter output voltage and load current during OC fault (Healthy condition, during fault and post-fault), (a) S_2, (b) S_3, (c) S_4, (d) S_5 & (e) S_6.

and a constant load of 25Ω & 10mH were considered. Here, the open circuit (OC) fault is created across various devices by triggering the pulses as per the sequence given in Table II. Fig. 5(a) illustrates the inverter output voltage and the corresponding load current during healthy condition, fault period and post-fault conditions. It can be noticed that the five-level output voltage with equal magnitude of dc voltage is generated that shows that the full output power capability of the inverter under faulty conditions is the same as in healthy conditions. Fig. 5(b) shows that the mode transitions change from zero state to one based on whether the corresponding switching sequences change under faulty situation. The switch current S_1 becomes zero during fault and post-fault conditions i.e., from 0.2 sec to 0.5 sec.

Similarly, the fault is created at various switches and their corresponding output voltage and load current are shown in Figs. 6(a) to (e). Except S_5 and S_6 faults, the five-level output voltage remains same during healthy as well as post-fault conditions. As discussed before, during fault at either S_5 or S_6 the three-level output voltage waveform is generated by regulating the magnitude of the fundamental waveform to generate equal output voltage as shown in Figs. 6(d) & 6(e). The load current becomes sinusoidal and delivers power to the load. Moreover, the proposed topology is tested for grid connected operation with the use of a simple proportional-resonant (PR) controller. Fig. 7 shows the simulation results of inverter output voltage, grid voltage and grid current (scaled up to 10 times) during OC faults across switches S_2 and S_3. It can be noticed that the fault is created at 0.3 sec and the inverter output of five-level voltage waveform is remains unchanged by changing the switching sequence and injects current into the grid. This shows the developed algorithm works well and is most opted for OC faults.

IV. Comparison of various Fault-Tolerant MLI Topologies

In order to evolve the performance of the proposed topology, a comparison of various fault-tolerant five-level topologies

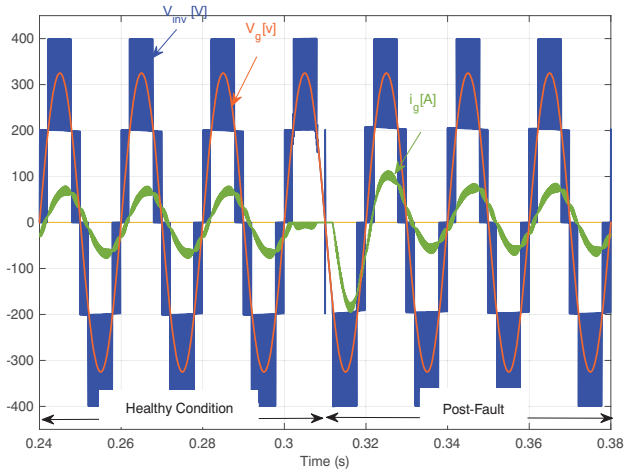

Fig. 7. Simulation results of inverter output voltage, grid voltage and load current during OC fault across S_2 & S_3 (Healthy and post-fault conditions).

is made in this section. Table IV shows the comparison of renowned five-level inverters such as NPC, FC and CHB along with various fault-tolerant MLIs proposed in recent years. It can be noticed that the proposed topology is compact and requires only single dc source compared to CHB and other references [4], [6], & [10]. Most of the recently proposed topologies demand more devices and driver circuits compared to the proposed topology. This shows that more devices were in conduction for other five-level topologies compared to a maximum of three switches in the proposed topology. This implies that the switching and conduction losses will be lower and overall efficiency is expected be significantly higher than that of other fault-tolerant MLIs. Moreover, the proposed MLI is more competitive in terms of single dc source requirement and 100% utilization of input source.

V. Conclusion

This paper presents a new single-phase fault-tolerant T-type five-level inverter. The proposed topology owns the advantages of both modular and reduced count with a maximum of three switches were in operation. The complete operation of single switch OC faults and switching scheme for multi-switch OC is also presented. Level-shifted PWM is implemented to produce the desired output voltage. In order to validate the fault tolerant capability of the proposed MLI, simulation was performed in MATLAB software and the results are presented. Further the full DC bus utilization of the proposed circuit made interesting alternative for the DC bus mid-point clamping circuits. Finally, a detailed comparison is made to highlight the significance of the proposed MLI in terms of devices and efficiency.

References

[1] R. Choupan, S. Golshannavaz, D. nazarpour, and M. Barmala, "A new structure for multilevel inverters with fault-tolerant capability against open circuit faults," *Electric Power Systems Research.*, vol. 168, pp. 105–116, 2019.

[2] H. Rehman, M. Tariq, A. Sarwar, W. Alhosaini, M.A. Hossain, and S.M. Batiyah, "Single-Phase Fault- Tolerant Multilevel Inverter Topologies—Comprehensive Review and Novel Comparative Factors," *Energies*, pp. 1-52, 2022.

[3] H. Rehman, A. Sarwar, M. Tariq, and A. I. Sarwat, "A Fault Tolerant Multilevel Inverter for Off-grid Solar Photovoltaic Application," *2023 International Conference on Power, Instrumentation, Energy and Control (PIECON)*, Aligarh, India, 2023, pp. 1-6.

[4] V. S. P. K, and S. Peddapati, "Single-Phase Five-Level Multiswitch Fault-Tolerant Inverter," *IEEE Trans. on Power Electron.*, vol.38, no.6, pp. 7336-7347, June 2023.

[5] T.J. Nistane, L.K. Sahu, M. Jalhotra, and S.P. Gautam, "Single and multiple switch fault-tolerance capabilities in a hybrid five-level inverter topology," *IET Power Electron.*, vol.13, no.6, pp. 1257-1266, 2020.

[6] B. H. Kumar, V. Bakka, B. Suresh, V. S. Chandrikax, K. Janardhan, and R. S. Kumar, "A New Fault Tolerant Five-Level Multilevel Inverter for Critical Loads," *2023 International Conference on Computer Communication and Informatics (ICCCI)*, Coimbatore, India, 2023, pp. 1-5.

[7] M. Jalhotra, L. Kumar, S.P. Gautam, and S. Gupta, "Development of fault-tolerant MLI topology," *IET Power Electron.*, pp.1-10, 2018.

[8] C. Sadanala, S. Pattnaik, and V.P. Singh, "Fault tolerant architecture of an efficient five-level multilevel inverter with overload capability characteristics," *IET Power Electron.*, vol.13, pp. 368–376, 2020.

[9] M.D. Siddique, M. Rawa, S. Mekhilef, and N.M. Shah, "A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources," *Int. J. Electr. Power Energy Syst.*, vol.128, pp.1-16, 2021.

[10] N.K. Dewangan, T.K. Tailor, R. Agrawal, P. Bhatnagar, and K.K. Gupta, "A multilevel inverter structure with open circuit fault-tolerant capability," *Electrical Engineering*, vol.103, pp. 1613-1628, 2021.

[11] Y. P. Siwakoti, "A new six-switch five-level boost-active neutral point clamped (5L-Boost-ANPC) inverter," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, 2018, pp. 2424-2430.

TABLE IV
Comparison of various Fault-Tolerant Five-Level Inverters

Level	NPC	FC	CHB	[4]	[5]	[6]	[8]	[10]	Proposed
DC Sources	1	1	2	2	1	2	1	2	1
Capacitors	4	10	0	0	1	0	1	0	2
Switches	8	8	8	12	12	4	12	9	6
Bidirectional Switches	0	0	0	0	0	2	1	0	2
Drivers	8	8	8	12	12	6	13	9	8
Diodes	12	0	0	0	0	0	0	0	0
No. of Level	5-L	5-L	5-L	5-L	5-L	5-L	5-L	5-L	5-L
Fault tolerance	N	N	Y	Y	Y	Y	Y	Y	Y