A New Single-Phase Two-Stage Five-Level Photovoltaic Inverter With Low Leakage Current

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***Abstract*-The increased attention towards transformerless inverters (TI) is attributed to their compact size and cost-effectiveness. Various topologies have been proposed to address the issue of leakage current, a significant concern in TI. This paper introduces a single-phase two-stage five-level inverter designed for renewable applications. The topology comprises a DC-DC buck-boost converter and a five-level inverter. The operational principle along with a detailed presentation of a simple Level-shifted Pulse Width Modulation (LS-PWM) technique are outlined. The presented topology is characterized by its voltage-enhancing capability and reduced switch count. Performance evaluation is conducted using MATLAB/Simulink, encompassing an analysis of leakage current and the Common Mode Voltage (CMV) associated with the inverter. The total harmonic distortion (THD) is also analyzed. A method for controlling grid current is employed to generate gating pulses for the switching device and managing both active and reactive powers. This paper provides significant insights into transformerless inverters emphasizing a solution-oriented approach to address leakage current concerns in the context of renewable energy applications.**

Keywords— Transformerless inverters, LS-PWM, leakage current, common mode voltage.

I. INTRODUCTION

The recent trend in electric systems involves in increasing dependence on renewable energy sources, which reduce environmental impact and helped to mitigate the emission of greenhouse gases. These sources offer several key advantages, including a consistent power source, ease of implementation, and their eco-friendly nature. Solar Photovoltaic technology plays a vital role in the global transition towards clean and more sustainable energy sources and efforts to combat climate change. Solar PV technology is also advancing rapidly, with a strong emphasis on improving efficiency, lowering costs, and integrating solar power into the broader energy grid. Solar photovoltaic systems find applications across various sectors, including residential, commercial, and industrial electricity generation.

The upcoming photovoltaic (PV) converters must meet the mentioned criteria, such as a 20-year lifespan, efficiency exceeding 95%, a broad input voltage range, localized maximum power point tracking and safety regulations [1]. Moreover, development of power electronic interfaces play a vital role of PV power generations. In recent years multilevel inverters (MLIs) is getting popular for PV systems. Basically, the traditional MLIs are categorized mainly into three types: 1) Cascaded H-bridge (CHB); 2) Neural-point clamped (NPC); and 3) Flying capacitor converters [2]. There is complexity in control, size and cost due to more number of switches, diodes and capacitors. Cascaded multilevel inverters synthesis a medium-voltage output and attains high-quality output voltages and input currents. A survey of various topologies, modulation techniques and control strategies utilized by these MLI's and also various advanced and regenerative topologies are presented [3].

Consequently, there has been a notable surge in the installation of grid-connected PV systems for electricity generation. Based on type of connection grid connected PV inverters are mainly divided into isolated and non-isolated inverters. The former has a transformer and the latter has no transformer. The transformerless inverter (TI) has becoming more popular due to compact size, low cost and high efficiency [10]. But in TI there is a ground capacitance(C_{PV}) between PV and ground which results in a resonant path formed by C_{PV} of the PV module and the output filter which is located on the grid side[4], [5].This results in a common mode voltage (CMV) and leakage current flows through the resonant path [6].

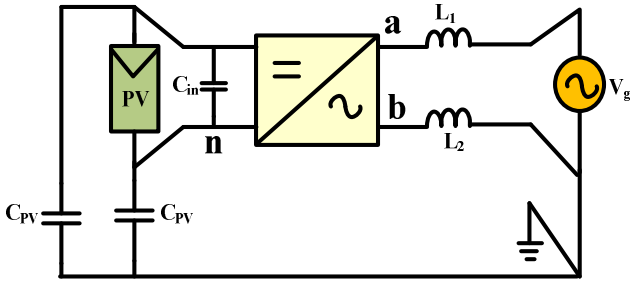

Fig. 1. Common mode schematic of single-phase TI.

Based on the IEEE standard, the leakage current for grid connected TI must be below 100mA [7]. To address this issue, numerous topologies or configurations of MLIs have been presented by the researchers on TI. Leakage current can be minimized by two methods: 1) maintaining constant CMV and 2) Minimizing high-frequency oscillations [8]. With the utilization of unipolar PWM in a full-bridge or half-bridge inverter, it effectively reduces the common mode current to a significant value [12]. The CMV generates resonant circuit resulting in leakage current. It depends mainly on the size of the PV array and environmental conditions [9].

The common mode schematic of a single-phase transformer less inverter is shown in the Fig.1 [10]. The common mode voltage (CMV) expression is obtained from the below equation:

$$V_{cm}(t) = \frac{V_{an}(t)+V_{bn}(t)}{2} \quad (1)$$

Numerous HERIC topologies have been introduced, with superior efficiency but suffering from leakage current

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characteristics that are less favorable than those of the H5 topology [6], [11].

The main aim of this paper is to present a two-stage five-level transformerless inverter with voltage-boosting capability and reduced switch count. The MLI with a front-end DC/DC buck-boost converter is implemented for photovoltaic applications. A simple LS-PWM is utilized to generate gating pulses for power semiconductor devices. The key features of the presented configuration are as follows:

1. Reduced switch count.
2. Improved utilization of the DC-link voltage.
3. Two-stage DC-to-AC conversion with the added capability of voltage boosting and reduced leakage current.
4. Active and reactive power controlling capability.

II. Proposed Topology

Fig. 2. shows the proposed single-phase two-stage five-level inverter for photovoltaic applications. It consists of a DC/DC buck-boost converter cascaded with a reduced switch count five-level DC/AC inverter. Here, the DC/DC converter is built with a single switch (S_b), single inductor (L_a), Single diode (D_a) and Single Capacitor (C_1). The main function of the DC/DC converter is to regulate the voltage across the capacitor irrespective of changes in PV output or load current and balances both the capacitor voltages is an added advantage of the converter. However, this is achieved by using a simple proportional-integral (PI) controller as shown in Fig. 3.

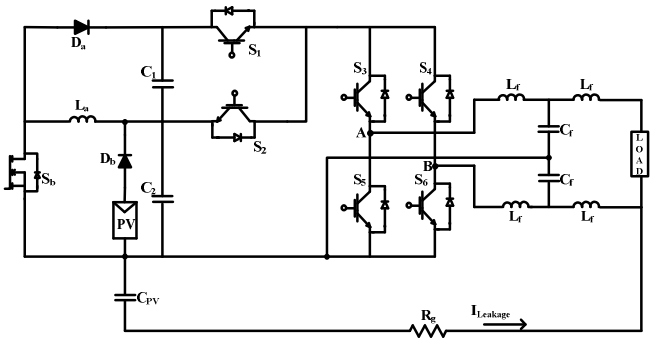

Fig. 2. Proposed single-phase two-stage five-level PV inverter.

The general expression used to calculate the output voltage of the DC-link is as follows:

$$V_{dc} = \frac{D*V_{in}}{(1-D)} \quad (2)$$

Where, V_{in} = dc input voltage, D = duty ratio.

Further, to realize the five-level output voltage waveform, a simple DC/AC inverter consisting of six switches (S_1-S_6) is shown in Fig. 2. The switching states for the each output voltage level generation is described in Table I for easy understanding. Moreover, maximum of only three switches are in conduction for each level generations which will enhance the overall efficiency of the proposed topology is an advantages proposition for photovoltaic applications. In order to realize the five-level output voltage waveform, a simple level-shifted pulse width modulation (LS-PWM) technique is used. LS-PWM is a technique commonly used in power electronic systems, particularly in inverters, to efficiently generate AC voltages from DC sources. In basic PWM techniques, such as carrier-based PWM, the amplitude of the reference signal (often a sine wave) is compared to a triangular carrier wave. The output of this comparison determines the switching of the power devices (transistors or IGBTs) in the inverter. Moreover, the number of levels (n) is determined by the total carriers, which depends on (n-1) carriers. For the five-level operation, four carriers are compared with one fundamental sinusoidal waveform, and the gating signals generated for the switches S_1-S_6 are shown in Fig. 4. For the better understanding of the operation, the different states of the DC/AC inverter are described as follows:

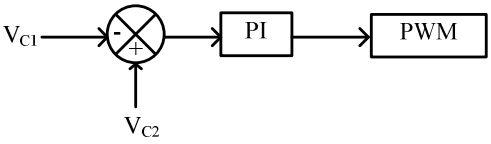

Fig. 3. Control scheme for the DC/DC buck-boost converter.

A. Switching State Description

1. $+2V_{dc}$ level-Positive powering state:

In this operational mode, switches S_1, S_3, and S_6 are ON, the terminal A is connected to the positive side of the DC-link. During this state, the maximum output of the inverter is obtained with the combination of C_1 and C_2, resulting in the synthesis of $V_o = +2V_{dc}$.

Table. I Switching States For Five-Level DC/AC Inverter

Switching state						Output Voltage
S_1	S_2	S_3	S_4	S_5	S_6	(V_{AB})
1	0	1	0	0	1	$+2V_{dc}$
0	1	1	0	0	1	$+V_{dc}$
0	1	1	1	0	0	0
0	1	0	0	1	1	0
0	1	0	1	1	0	$-V_{dc}$
1	0	0	1	1	0	$-2V_{dc}$

1-ON, 0-OFF

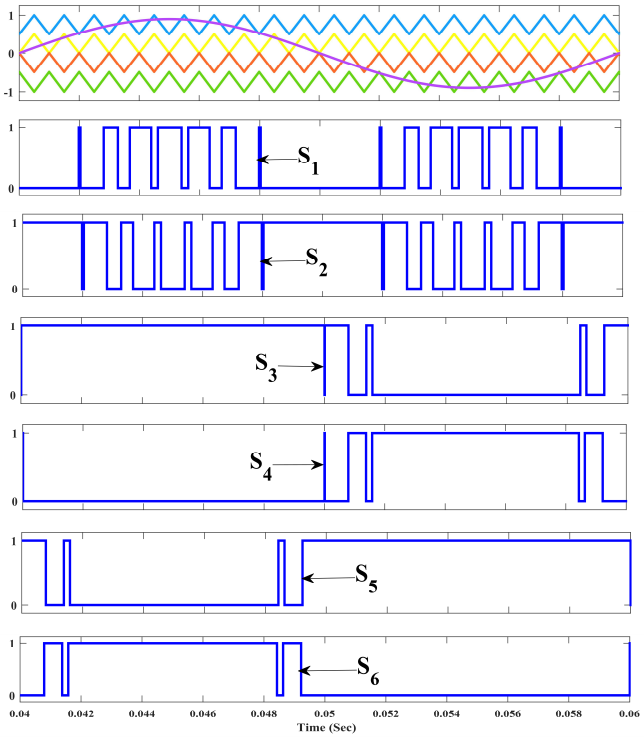

Fig. 4. LS-PWM and gating pulses for switches (S_1-S_6).

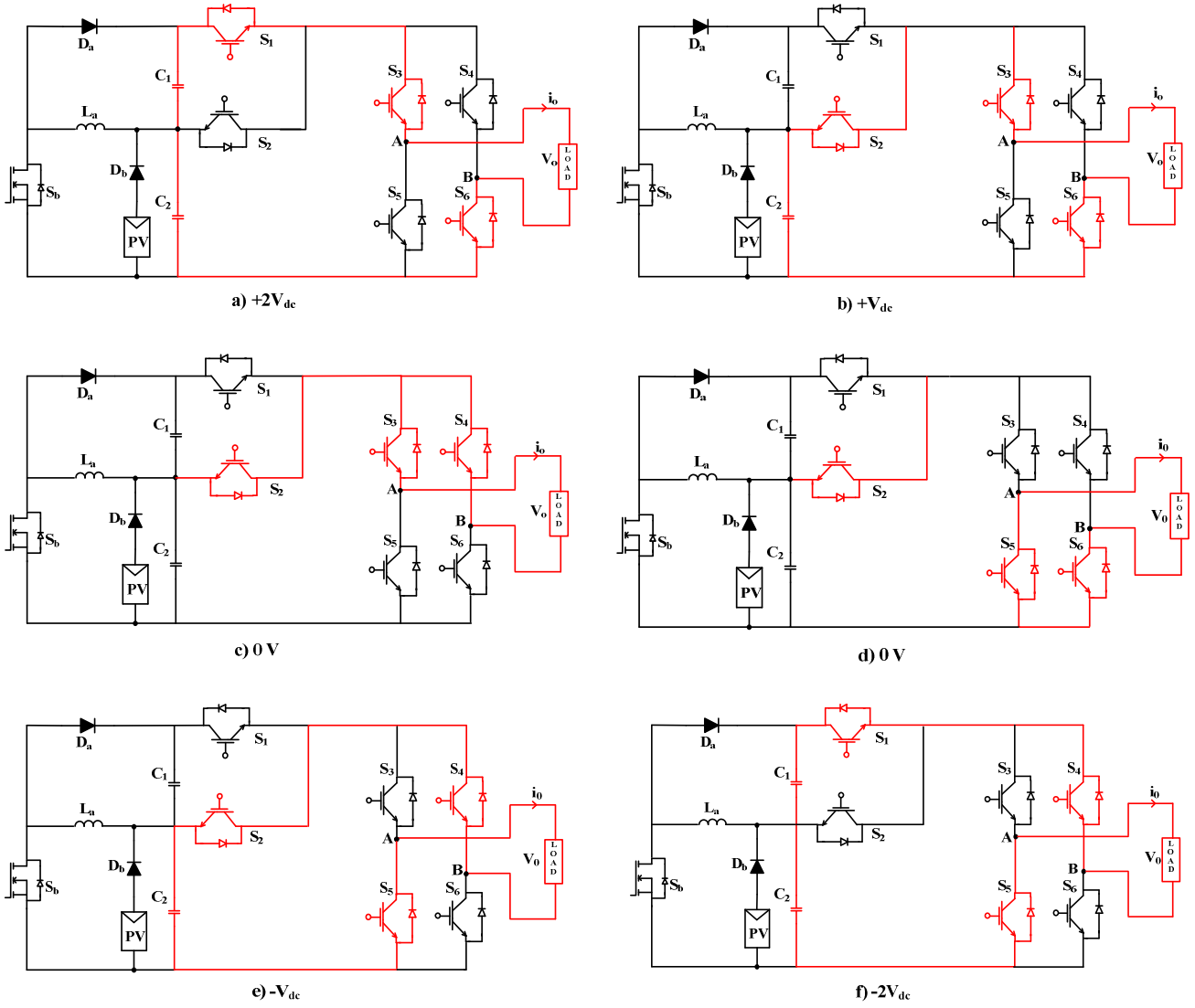

Fig. 5. Switching states and current path for five level voltage generation (a) $+2V_{dc}$ level, (b) $+V_{dc}$ level, (c) & (d) 0 V level, (e) $-V_{dc}$ level, (f) $-2V_{dc}$ level.

2. $+V_{dc}$ level-Positive powering state:
In this operational mode, semiconductor switches S_2, S_3, and S_6 are turned ON, the terminal A is connected to the mid-point of the dc-link. During this state, the output voltage becomes half of maximum voltage and is equal to voltage across capacitor C_2, leading to the synthesis of $V = +V_{dc}$.

3. 0 V level-freewheeling state:
In this operational mode, either semiconductor switches S_2,S_3 and S_4 or S_2,S_5 and S_6 are in the ON state. This configuration generates zero output voltage, resulting in the synthesis of $V_o = 0V$.

4. $-V_{dc}$ level- Negative powering state:
In this operational mode, semiconductor switches S_2, S_4, and S_5 are in the ON state. During this state, the output voltage becomes half of maximum voltage and is equal to voltage across capacitor C_2, leading to the synthesis of $V_o = -V_{dc}$.

5. $-2V_{dc}$ level-Negative Powering state:
In this operational mode, semiconductor switches S_1, S_4, and S_5 are in the ON state. During this state, the configuration generates the negative maximum output voltage with the combination of C_1 and C_2, resulting in the synthesis of $V_o = -2V_{dc}$.

III. Simulation Results

The suggested configuration is formulated using MATLAB/Simulink for an in-depth analysis of the inverter's performance. The topology incorporates specific parameters: a buck-boost inductor with a value of 1mH, two capacitors each with a capacitance of 2000µF, a switching frequency of 10 kHz for S_6, an input voltage of 250V, and a load parameter (RL)=(25Ω + j10mH). The provided input voltage=250V. Notably, the parasitic capacitance (C_{PV}) is established at 20nF, and the ground resistance (R_g) =10Ω during the simulation study.

Fig. 6 shows the measured waveforms of the DC input voltage, and voltage across the capacitors C_1 and C_2. The voltage of 250V is maintained constant in the both the capacitors for the given input by regulating the duty ratio of the DC/DC converter. Fig. 7 shows the five-level inverter output, filtered output voltage and their corresponding load current under steady-state conditions. Fig. 8 shows the %THD of the injected current into the grid which is less than 5% i.e., 3.77% and within the IEEE standards.

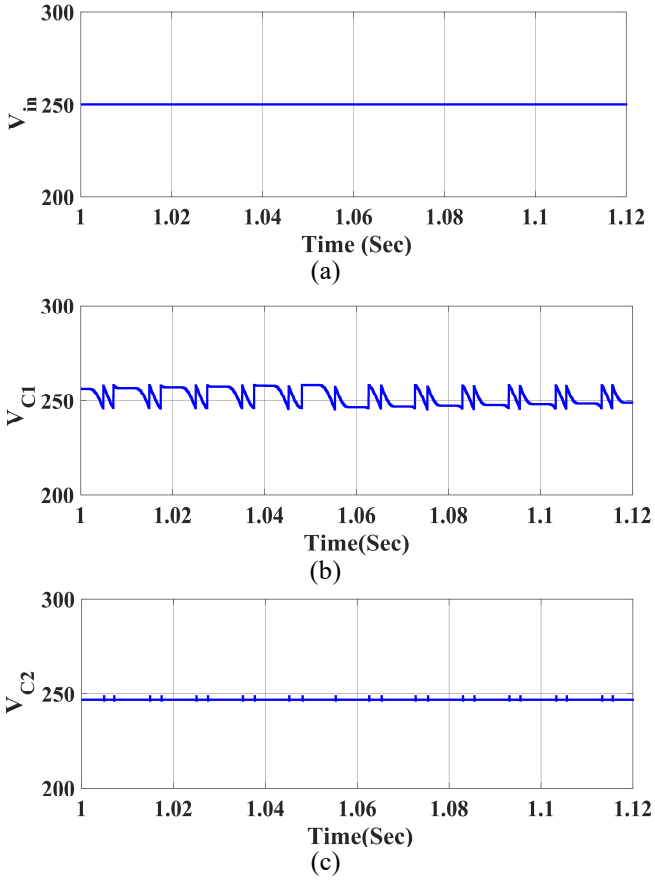

Fig. 6. Response of (a) Input dc voltage, (b) Voltage across capacitor C_1, (c) Voltage across capacitor C_2.

A. Common Mode Voltage Analysis

The proposed configuration incorporates an active filter, as illustrated in Fig. 2, which can be used for mitigating the Common Mode Voltage (CMV) and also filtering the high-frequency oscillations in output voltage. Additionally, this design also monitors high-frequency fluctuations in the voltage across the parasitic capacitor (C_{PV}). The active filter splits the filter capacitor into two equal parts, connecting the midpoint of these split capacitors to the negative of the input (PV). Consequently, this approach significantly reduces leakage current [13]. The magnitude of the leakage current is mainly affected by the circuit topology, pulse width modulation scheme, and the resonant circuit path formed by the ground capacitor (C_{PV}), converter, output AC filter and the grid. The total common-mode voltage is calculated by using equation (1). Fig. 9 shows the results of phase voltages and common mode voltage of the proposed topology. In addition, Fig. 10 shows the voltage across parasitic capacitance and the corresponding leakage current. In simulations, the observed leakage current is under 20mA, a value well below the limits set by IEEE standards.

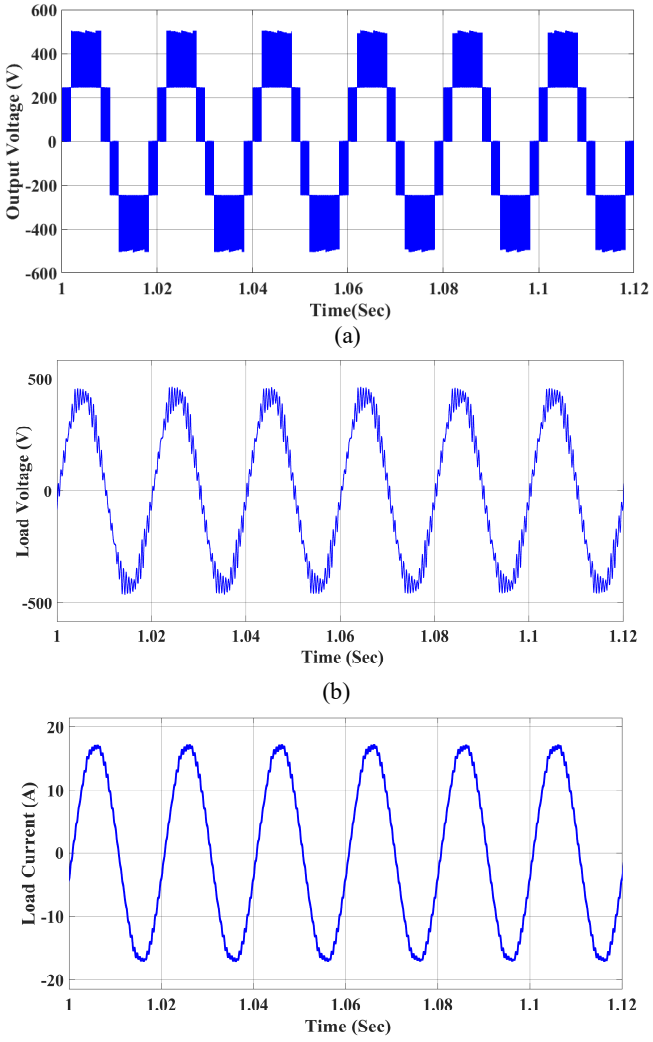

Fig. 7. Response of (a) Five-level output voltage (b) Filtered output voltage and (c) Load current of the inverter.

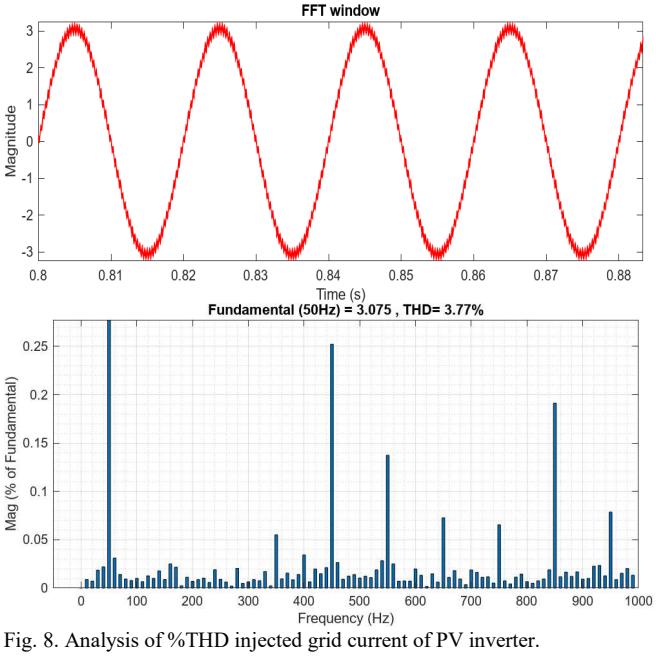

Fig. 8. Analysis of %THD injected grid current of PV inverter.

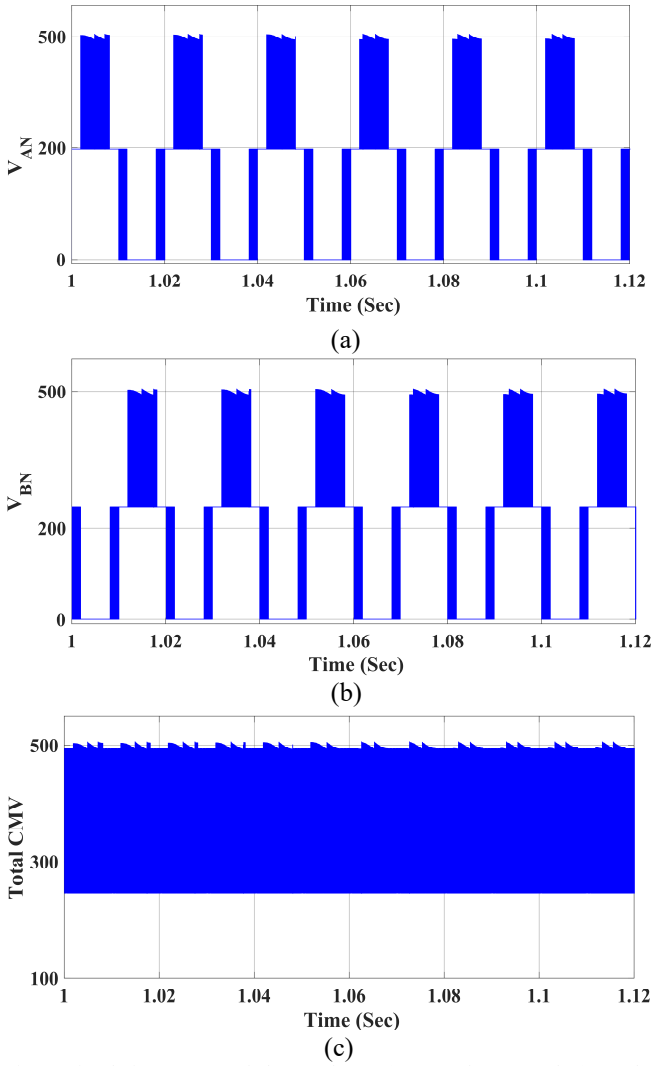

Fig. 9. Simulation outputs of phase voltages (a) V_{AN}, (b) V_{BN} and (c) Total CMV.

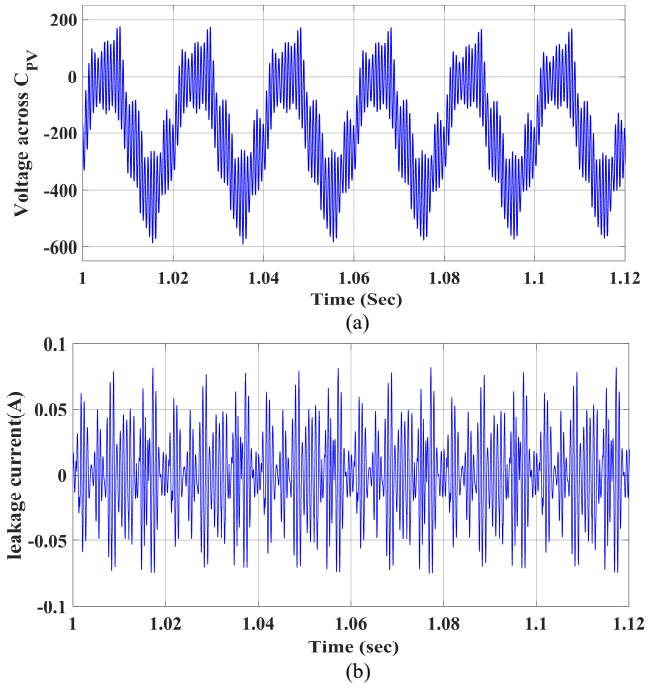

Fig. 10. Waveform of (a) voltage across parasitic capacitance (C_{PV}) and (b) Leakage current.

B. Control Strategy for Grid-tied Inverter

A grid current control method (GCC) is employed to investigate and validate the proposed inverter in real-world scenarios, specifically in conjunction with grid-tied photovoltaic (PV) systems. The inverter employs a GCC approach to determine a switching pattern, effectively managing both active and reactive powers. The control system involves acquiring a reference injected current based on active power and reactive power references, incorporating phase information obtained through a phase-locked loop (PLL). The schematic diagram of the control system for grid-connected usage is illustrated in Fig. 11. In this configuration, the reference current is derived from the specified active power reference (P^*) and reactive power reference (Q^*). Additionally, the magnitude and phase information of the grid values are obtained through the integration of a phase-locked loop (PLL) [14]. Employing a proportional-resonant (PR) controller within the injected grid current loop, an AC reference is derived. This reference is subsequently directed to the level-shifted pulse width modulation stage, where it undergoes comparison with the carriers in each operational mode, leading to the generation of gate pulses. The simple way of tuning the PR controller derived from the Propotional-Integral (PI) controller is addressed for better understanding in [15].

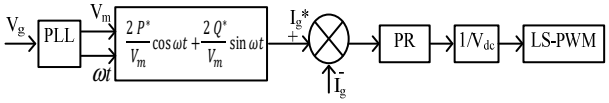

Fig. 11. Control scheme of proposed grid-tied inverter.

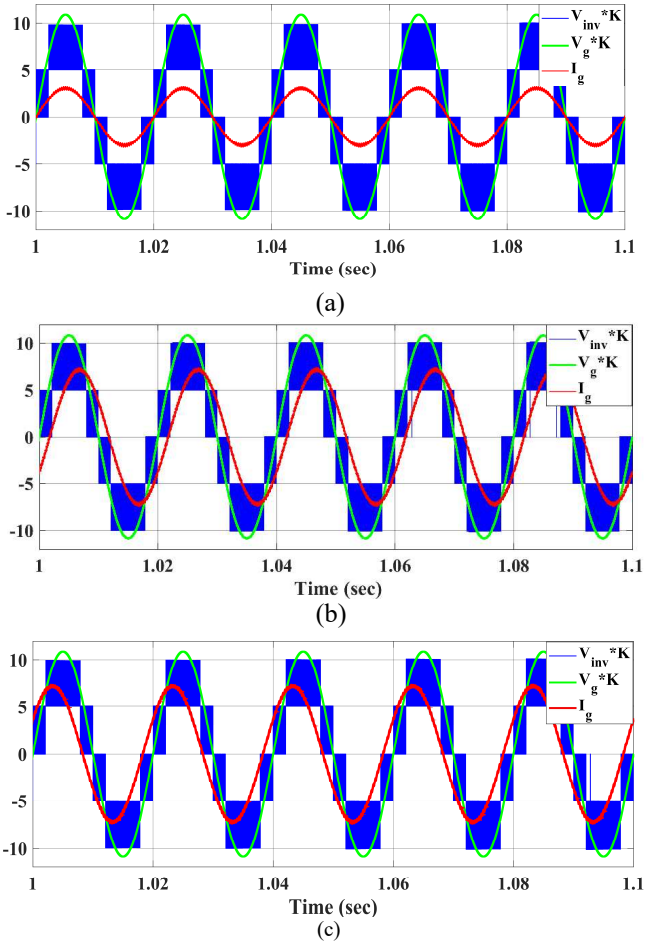

Fig. 12. Simulation results of proposed inverter operating at (a) Unity power factor, (b) Lagging power factor, (c) Leading power factor.

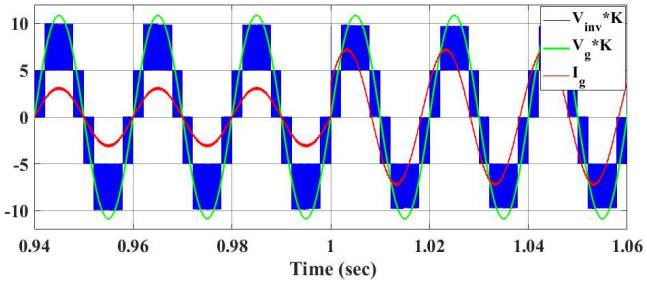

Fig. 13. Waveform of the proposed inverter with step change in active and reactive power at t=1 sec.

Fig. 12 shows the simulation results of the five-level inverter output voltage with grid voltage and grid current under unity, lagging and leading power factors. Similarly, Fig. 13 shows the dynamic response of the injected grid current. It is observed that the PR controllers performs well and regulates the grid current as per the demands. This shows that the proposed topology is most opted for PV system with reduced leakage current.

IV. Conclusion

The proposed configuration can produce a five-level output voltage with voltage-boosting capability. A simple Level-shifted PWM technique is implemented to generate gating pulses and is easy to implement. The performance and viability of the proposed five-level inverter are confirmed by the simulation results done in MATLAB/Simulink environment. Additionally, total harmonic distortion analysis is also presented. By implementing a grid current control method, the active and reactive power control capability is achieved. The paper also includes an analysis of leakage current and common mode voltage, demonstrating that the proposed topology is particularly well-suited for PV applications.

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