DESIGN AND ANALYSIS OF MULTILAYER ON-CHIP INDUCTORS FOR RF APPLICATIONS

Submitted in partial fulfillment of the requirements
for the award of the degree of
DOCTOR OF PHILOSOPHY

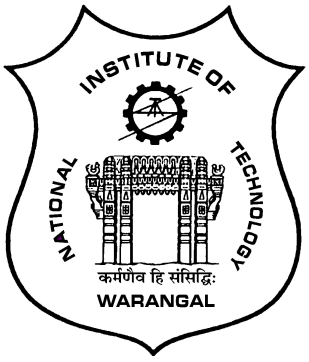
by

B. MURALI

(Roll No: 716031)

Supervisor:

Dr. N. Bheema Rao
Professor



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL
TELANGANA STATE-506004, INDIA

2024

Dedicated to

My family & Teachers

Approval Sheet

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Examiners

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_____

_____

Supervisor

_____

Dr. N. Bheema Rao
Professor
Department of ECE
NIT Warangal

Chairman

_____

Dr. D. Vakula
Professor & HOD
Department of ECE
NIT Warangal

Date: _____

DECLARATION

This is to certify that the work presented in the thesis entitled "**Design and Analysis of Multilayer On-Chip Inductors for RF Applications**" is a bonafide work done by me under the supervision of **Dr. N. Bheema Rao**, Professor, Department of Electronics and Communication Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea / data / fact / source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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(Roll No: 716031)

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CERTIFICATE

This is to certify that the thesis entitled "**Design and Analysis of Multilayer On-Chip Inductors for RF Applications**", which is being submitted by **Mr. B. Murali (Roll No: 716031)**, in partial fulfillment for the award of the degree of Doctor of Philosophy to the Department of Electronics and Communication Engineering of National Institute of Technology Warangal, is a record of bonafide research work carried out by him under my supervision and has not been submitted elsewhere for any degree.

Dr. N. Bheema Rao
(Supervisor)
Professor
Department of E.C.E.
N.I.T. Warangal
Warangal - 506004, India

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ABSTRACT

Recent advances in wireless communication necessitate the development of high-performance, cost-effective, and miniaturized wireless devices with low power consumption. Integrated inductors are among the fundamental passive elements employed in the design of Radio Frequency Integrated Circuits (RFICs) and Monolithic Microwave Integrated Circuits (MMICs). These inductors are crucial for implementing various circuits such as Voltage Controlled Oscillators (VCOs), Low Noise Amplifiers (LNAs), impedance matching networks, filters, and power amplifiers. However, integrating these passive components into wireless devices presents several challenges, including design complexity, achieving a high-quality factor, minimizing on-chip area, and reduction of cost. This thesis addresses some of these challenges by focusing on the design and optimization of integrated on chip inductors. The design of passive components like inductors typically involves the use of electromagnetic (EM) simulators to predict performance metrics. Achieving the optimal performance requires balancing various trade-offs between the cost of the chosen technology and the specific application requirements. One effective approach to enhancing the performance of passive components is the use of spiral geometry. Spiral inductors have been shown to significantly improve the performance characteristics due to their efficient use of space and the ability to achieve high inductance values in a compact form. Here, the spiral geometry is adopted to reduce the footprint of passive components while maintaining or improving their performance metrics.

In this thesis, various inductors including planar inductors, half-turn split inductors, pyramid inductors, coupled pyramid inductors and multilayer inductors, have been proposed and designed to address performance limitations in RF applications. The performance of these inductors, particularly the quality factor, inductance, and self-resonant frequency, is often restricted by parasitic capacitance, current crowding, and proximity effects. To mitigate these issues and to enhance the quality factor, pyramid coupled pyramid and multilayer inductors are proposed. The pyramid inductor design offers improved inductance while optimizing the use of on-chip space. The coupled pyramid inductor achieves an optimal balance between inductance, quality factor, and area efficiency, making it highly suitable for RF applications. To further enhance the performance and improve quality factor within small area multilayer inductor is proposed. In this design each conductor turn is split into two different layers to reduce the overall capacitance, thereby improving the quality factor. Single-layer planar inductors, while straightforward to design, tend to suffer from poor quality factor and inductance. This is primarily due to all the metal tracks being at an equal potential, which exacerbates the capacitance effect. To overcome these drawbacks, a multilayer inductor design is proposed. By

stacking multiple layers, the parasitic capacitance is significantly reduced, and the inductance is increased. The careful selection of the width and spacing of the metal strips across the four layers helps minimize resistive losses, eddy currents, and the current crowding effect.

Mathematical validation of inductors is crucial for theoretically justifying their inductance values. Traditional frequency-independent analytical expressions often exhibit significant deviations when extracting inductance values at frequencies beyond 2 GHz. To address this limitation, this dissertation proposes a frequency-dependent inductance extraction method. This approach incorporates basic Maxwell's equations and magnetic flux expressions to provide more accurate inductance values across a wider frequency range. The Grover concept and Greenhouse method are implemented to evaluate the self-inductance and mutual inductance of spiral inductors. These methods offer a systematic way to account for the complex interactions within the inductor structure. The integral equations derived from these methods are solved using partial integral techniques, which help in precisely calculating the inductance values. For three-dimensional and multilayer inductors, this advanced methodology significantly reduces the error margin. The maximum percentage of error found for these inductors is between 3-4%, demonstrating the effectiveness of this approach. By using frequency-dependent methods, the dissertation ensures that the inductance values are more accurate and reliable, especially at higher frequencies where traditional methods fall short.

Further, a Voltage-Controlled Oscillator (VCO) is designed utilizing the proposed coupled pyramid inductor and multilayer inductor. VCOs are crucial components in telemetry and transponder applications due to their capacity to generate precise and tuneable frequencies, which are essential for maintaining accurate and reliable communication channels. The VCO is constructed using the Clapp configuration, a design particularly well-suited for high-frequency applications due to its ability to provide stable oscillations and excellent frequency tuning capabilities. The performance characteristics of the VCO, such as phase noise, output power, Figure of Merit (FoM), and overall output power, were measured by incorporating both the coupled pyramid inductor and multilayer inductor. Phase noise, a critical parameter in VCO performance, impacts the signal purity and is essential for applications requiring high signal integrity. The FoM, which combines multiple performance metrics into a single value, provides a comprehensive measure of the oscillator's efficiency and effectiveness. Simulation results demonstrate that the multilayer inductor significantly outperforms the coupled pyramid inductor in several key aspects. The multilayer inductor achieves a better FoM, indicating a more efficient and high-performing VCO design. Additionally, it provides superior output power and improved phase noise characteristics compared to the coupled pyramid inductor. These enhancements

are attributed to the multilayer inductor's optimized structure, which minimizes parasitic effects and maximizes inductance and quality factor.

The Low Noise Amplifier (LNA) is a crucial component in wireless receivers, tasked with amplifying incoming signals from the antenna while preserving a high signal-to-noise ratio (SNR). In this, LNAs have been designed using the proposed coupled pyramid and multilayer inductors, each contributing uniquely to the performance of the amplifier. Designing an effective LNA requires balancing several performance metrics, including gain, linearity, noise figure, input matching, and power consumption. These metrics often involve trade-offs; improving one aspect can sometimes lead to compromises in another. The results of indicate that while the gain of the LNA remains almost the same whether using the coupled pyramid inductor or the multilayer inductor, the noise figure is significantly improved when the multilayer inductor is used. Specifically, the noise figure is improved by 64.2% in the LNA incorporating the multilayer inductor compared to the one using the coupled pyramid inductor. This dramatic improvement in the noise figure is particularly advantageous for applications requiring high signal integrity and low noise levels. The multilayer inductor's superior performance in reducing the noise figure highlights its value in the development of advanced communication systems, especially in the high-demand environment of 5G networks. The enhanced noise performance of the LNA with the multilayer inductor makes it an excellent candidate for such applications, ensuring that signals are amplified with minimal added noise, thereby preserving the quality and reliability of communication.

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List of Abbreviations

3D	Three Dimensional
AMS	Analog/mixed signal
BPF	Band Pass Filter
CMOS	Complemtary Metal Oxide Semiconductor
EM	Electro Magnetic
FOM	Figure of merit
IC	Integrated Circuit
IPD	Integrated Passive Devices
LNA	Low Noise Amplifier
MEMS	Micro Electro Mechanical System
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal
Op-Amp	Operational Amplifier
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RF	Radio Frequency
SoC	System On Chip
SEI	Silicon Embedded Inductor
SRF	Self Resonsnce Frequency
VCO	Voltage Controlled Oscillator

Chapter 1

Introduction

1.1 Overview

The evolution of wireless and mobile communication technologies has required the development of low-cost, highly integrated solutions with small on-chip passive components. These components including capacitors, inductors, and resistors play a crucial role in the implementation of receivers and transmitters. The concept of on-chip passive components emerged in the 1990s, initiating significant research efforts [1, 2]. Furthermore, the modern wireless applications often require the integration of multiple functions, such as personal digital assistants, video games, phones, web browsers, emails, and digital cameras, into a single device. This demand has driven researchers to explore the integration of digital, analog, and mixed-signal modules on a single chip to realize Radio Frequency (RF) and mixed-signal system-on-chip (SoC) architectures [3, 4]. One of the primary challenges in achieving this integration is the incorporation of passive components into the SoC design. While Moore's Law has facilitated the scaling down of active components, such as Complementary Metal Oxide Semiconductor (CMOS) transistors, to increase component density and reduce die size, passive components cannot be scaled down at the same pace. This limitation arises from the specific capacitance, resistance, and impedance values required for processing analog signals effectively.

Passive components, particularly inductors, present challenges due to their dependence on physical properties like size and material composition. Shrinking these components to match the scaling of active elements poses significant engineering hurdles. Additionally, the performance requirements of passive components in RF applications, such as high Q-factor

(quality factor) and low parasitic effects, further complicate their integration into SoCs. Researchers have explored various techniques to address these challenges, including innovative design methodologies, material advancements, and novel fabrication processes. For instance, micro-electro-mechanical systems (MEMS) technology has been investigated for on-chip inductor fabrication, offering potential solutions to size and performance limitations. Despite these challenges, the demand for highly integrated RF and mixed-signal SoCs continues to grow, driving ongoing research and development efforts aimed at overcoming obstacles related to on-chip passive component integration. As technology advances and new solutions emerge, the realization of compact, cost-effective wireless communication systems with integrated passive components becomes increasingly achievable. Passive components play a crucial role in electronic circuits by providing impedance, filtering, and tuning functions. The choice of passive components depends on various factors, including the frequency of operation and the circuit's requirements. At lower frequencies, passive devices can often be connected externally without significant issues [5]. However, as the frequency of operation increases, the parasitic effects become more pronounced and can degrade the performance of passive components [6]. In RF (Radio Frequency) and millimeter (mm)-wave applications, where frequencies are typically in the range of MHz to GHz, the characteristics of passive components become particularly critical. For instance, when designing a voltage-controlled oscillator (VCO), which is a fundamental component in RF circuits used for generating oscillating signals, the inductance value plays a crucial role. In practice, achieving small inductance values externally is challenging due to the limitations imposed by the packaging and interconnection technologies. The on-chip passive components are specially designed to offer low parasitic effects and provide the necessary performance characteristics at high frequencies, enabling the realization of VCOs, amplifiers, and filters.

Depending on the design and fabrication techniques, on-chip inductors can be classified into three main types: active, bond wire, and spiral inductors. Active inductors are made using standard CMOS processes, mimicking passive inductors with transistors [7, 8, 9]. Though easy to fabricate, they consume more power and introduce noise. Despite this, they find use in applications less sensitive to power and noise. Bond wire inductors, made by looping bond wires, boast a Q factor of 30 to 40, ensuring efficient energy storage and signal transmission. Nonetheless, they suffer from susceptibility to unwanted coupling with neighboring devices on the chip, leading to interference and compromising RF circuit performance [10, 11]. Hence Spiral inductors are the promising candidate for RF applications due to their compact size and excellent performance characteristics [12, 13, 14]. They are formed by tightly winding a metal trace into a spiral shape on the semiconductor substrate. Spiral inductors offer high Q factors

and can be optimized for specific frequency ranges by adjusting parameters such as the number of turns and spiral dimensions. They also have low parasitic capacitance, which is beneficial for RF circuits. Overall, spiral inductors are well-suited for high-frequency applications where space constraints and performance are critical factors.

1.2 On-chip Components

In high-frequency RF integrated circuits (RFICs), integrating inductors and capacitors directly into CMOS silicon wafers is crucial for achieving higher center frequencies and improved performance. However, integrating these RF passive components onto silicon CMOS wafers presents challenges due to their large sizes, which limits the miniaturization of high-performance 5G RFIC transceivers [15]. To address this challenge, Electronic Design Automation (EDA) tools are essential. These tools allow designers to create passive components directly on the silicon chip, facilitating the integration of circuits onto a single chip and improving interconnections within the packaging. The use of on-chip passive components with high Q factor enhances impedance matching across various stages of the circuit, leading to reduced power consumption.

1.2.1 Active inductor

High-performance RFIC designers struggle with the complicated task of merging digital, analog, and RF circuitry on a single chip. A pivotal challenge lies in integrating passive components, such as capacitors, inductors, and resistors, directly onto the RFIC. These components are crucial for filtering, matching, and tuning RF signals but traditionally take up a considerable amount of space, complicating the integration process and degrade the performance due to parasitic effects. Fortunately, recent advancements in design methodologies and fabrication technologies have paved the way for overcoming these challenges. Innovations like embedded passive components, 3D integration, and advanced material technologies offer promising solutions for achieving higher levels of integration without compromising on performance. These approaches not only reduce the footprint of passive components but also enhance the RFIC's overall efficiency, reliability, and functionality. As a result, the integration of digital, analog, and RF circuitry on a single chip has become increasingly feasible, leading in a new era of compact, high-performance RF systems. Active inductors play a crucial role in enhancing the performance and conserving space in CMOS RFICs [16]. The main criteria for evaluating active

inductors are the Q, self-resonance frequency, inductance (L), and the required on-chip area. Various factors influence the electrical performance of Inductors, including their geometrical design, process settings, and manufacturing methods [17]. As RFIC operating frequencies rise, the required L value decreases, making it challenging to achieve with off-chip inductors [18]. With the progress in CMOS technologies, we can now create on-chip passive inductors for fully integrated mixed-signal SOC systems. These Silicon Embedded Inductors (SEIs) are made by inserting metal conductors into silicon insulating substrates and linking them using through-Silicon-Via connections. Active inductors employ operational amplifiers (Op-Amp) and the

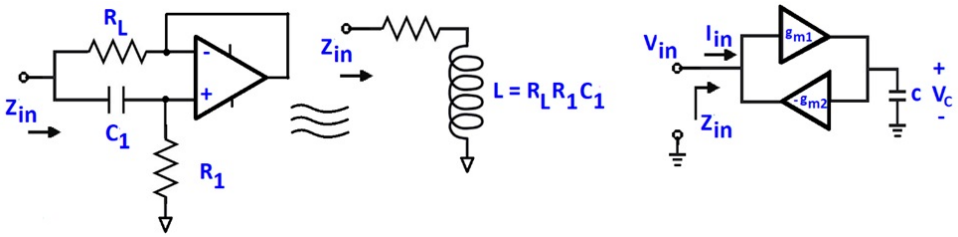


Figure 1.1: Op-Amp and a Gyrator based active inductor

gyrator-C methods. These devices have the ability to allow multi-band operation by adjusting the inductance. Fig. 1.1 depicts instances of active and gyrator inductors. An inductor may be

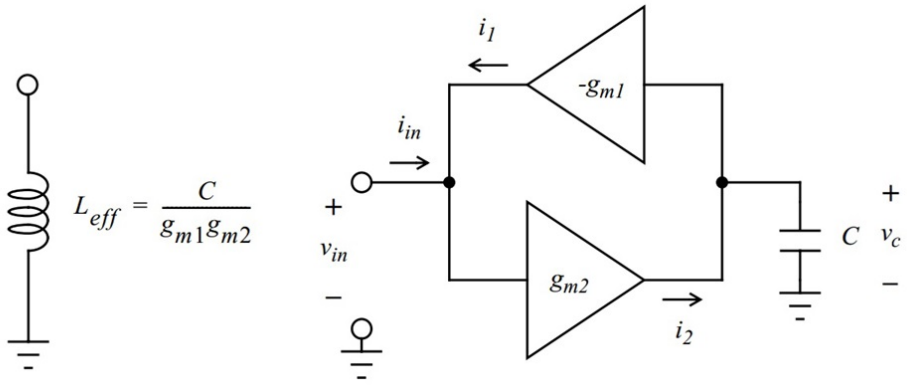


Figure 1.2: Gyrator-based active inductors in single-ended configurations

constructed by utilizing a series of resistors, an Op-Amp, and a capacitor. The Op-Amp functions as a high impedance element, replicating the characteristics of an inductor. Nevertheless, the Q-factor of these inductors based on Op-Amps is reduced due to the presence of a series resistor, R_L [19]. This architecture necessitates a greater amount of on-chip area and creates nonlinearity [20]. Further, the Gyrator based active inductor that connects two transconductors in a feedback loop to simulate an inductive impedance. This is accomplished by transforming its characteristic capacitance. With advancements in IC technologies, high-quality capacitors are readily available, enabling the creation of L using on-chip gyrators combined with capacitors [21]. Fig. 1.2 and Fig. 1.3 depict the typical structure of gyrator-based inductors in single-ended

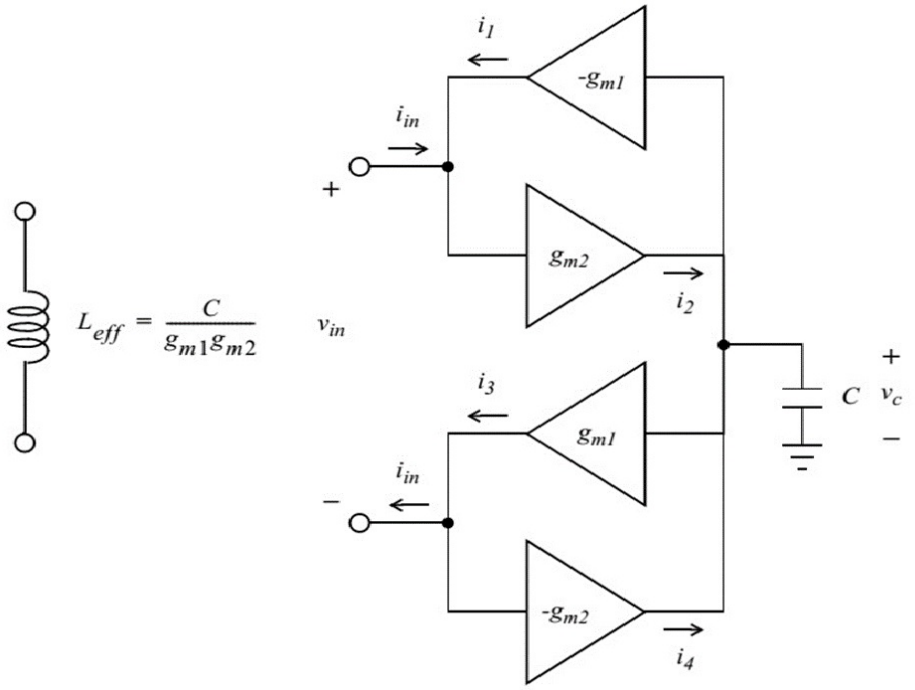


Figure 1.3: Gyrator-based active inductors in floating configurations

and floating configurations, respectively. This inductor works at frequencies below 1 GHz. The formula to calculate the effective impedance of the gyrator inductor is represented by Eq. 1.1.

$$L_{eff} = \frac{c}{g_{m1}g_{m2}} \tag{1.1}$$

where g_m represents the transconductance of two gain op-amps and C denotes parallel capacitance. On the other hand, active inductors tend to have drawbacks such as lower Q, poorer noise performance, and increased power consumption, mainly because of parasitic capacitances [22].

1.2.2 Bondwire inductor

Craninckx and Steyaert's work in 1995 marked a significant step forward in the field of RFICs by introducing the concept of on-chip bond wire inductors [23]. These inductors are an essential component in RF circuits, contributing to the circuit's performance and functionality. Bond wires are thin wires used to establish electrical connections between a semiconductor chip and its package, as illustrated in Fig.1.4. These wires are typically made of gold due to its good electrical conductivity and resistance to corrosion. The diameter of these bond wires usually ranges from 25 to 250 μm, and their length typically varies from 2 to 5 mm.

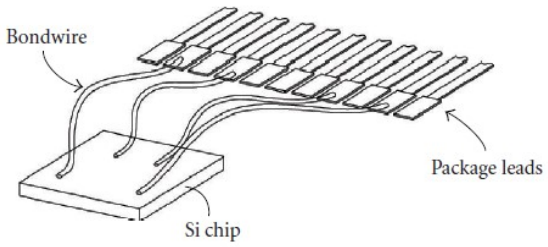


Figure 1.4: Interconnection of metal leads and packaged IC chip through bondwires

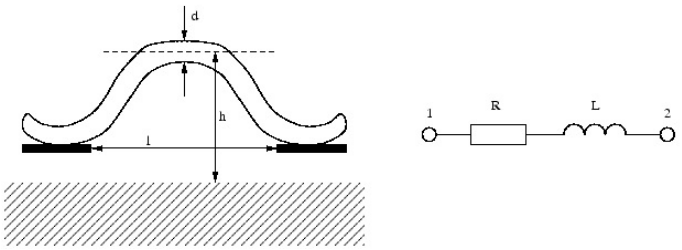


Figure 1.5: Bond wire and its equivalent circuit

Bond wire inductors primarily provide L to the circuit and they offer a value in the range of several nH. Besides inductance, bond wires also exhibit resistance (R), which can vary from several mΩ to tens of mΩ. One of the key advantages of bond wire inductors is their high Q-factor, typically ranging from 30 to 60. A higher Q-factor implies lower energy losses and better performance. The performance of a bond wire inductor is influenced by several factors:

- Length of the Wire (l): The inductance of the wire increases with its length.
- Diameter of the Wire (d): A larger diameter typically results in higher inductance and lower resistance.
- Height of the Substrate (h): This refers to the distance between the wire and the underlying substrate. It can influence the inductance and parasitic capacitance.
- Frequency of Operation: The inductor's behavior can change with the frequency at which it operates due to skin effect, proximity effect, and other high-frequency phenomena.

Fig.1.5 illustrates the physical dimensions and the equivalent circuit representation of a bond wire inductor. The physical dimensions include the wire's length, diameter, and height above the substrate. The equivalent circuit model would typically include the L, R, and possibly parasitic capacitance (C) to represent the inductor's behavior in the circuit. The bond wire usually has dimensions of around 100 μm x 100 μm, leading to significant parasitic capacitance and resistance because of the oxide layer and silicon beneath it [24]. These parasitic effects can

lead to reduced L, lower Q-factor, and limitations on the usable frequency range, affecting the overall performance and efficiency of circuits using bond wire inductors [25]. To mitigate these issues, designers often employ various techniques such as using thinner bond wires, optimizing the layout, or using different materials to minimize parasitic effects and improve performance.

1.2.3 Spiral inductor

Planar spiral inductors are commonly used on-chip inductor models, illustrated in Fig. 1.6. These inductors are typically fabricated in Si technologies using at least two metal layers. The upper layer creates the inductor's structure, while the lower layer connects the inner port to an external connector through via. A square spiral inductor is a widely adopted design for

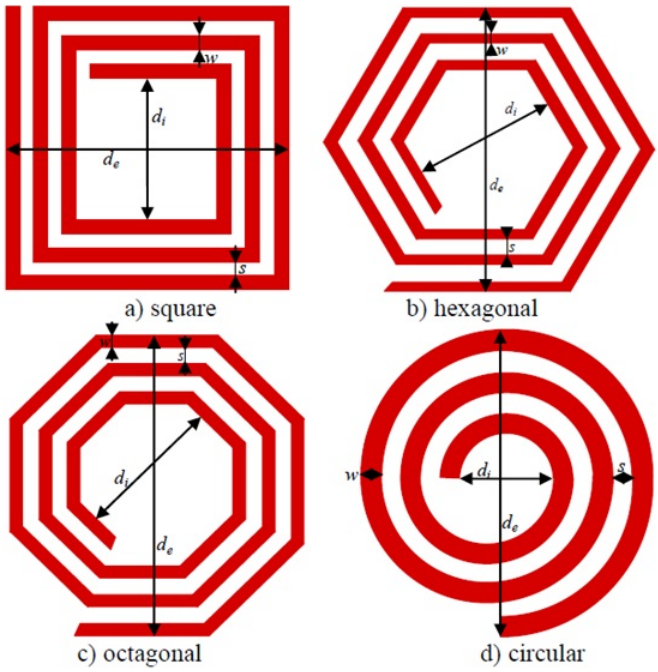


Figure 1.6: Bond wire and its equivalent circuit

monolithic inductors, initially developed mainly for RF applications. The key figure of merit (FoM) parameters for these on-chip spiral inductors include: (i) Q, (ii) Optimal frequency (f_{max}) at which the Q factor reaches its peak value (Qmax), and (iii) Self-resonant frequency (f_{SRF}). The design of a spiral inductor ensures that the turns carrying current in the same direction are placed closely together, while turns with current flowing in opposite directions are spaced farther apart. This configuration enhances the positive mutual inductance and increases the overall inductance value. In Fig. 1.7, region I represents the inductive region. The f_{SRF} is the frequency at which the Q factor drops to zero; beyond this frequency, the inductor starts behaving like a capacitor. The values of Q, L, and f_{SRF} can be significantly influenced by various parameters.

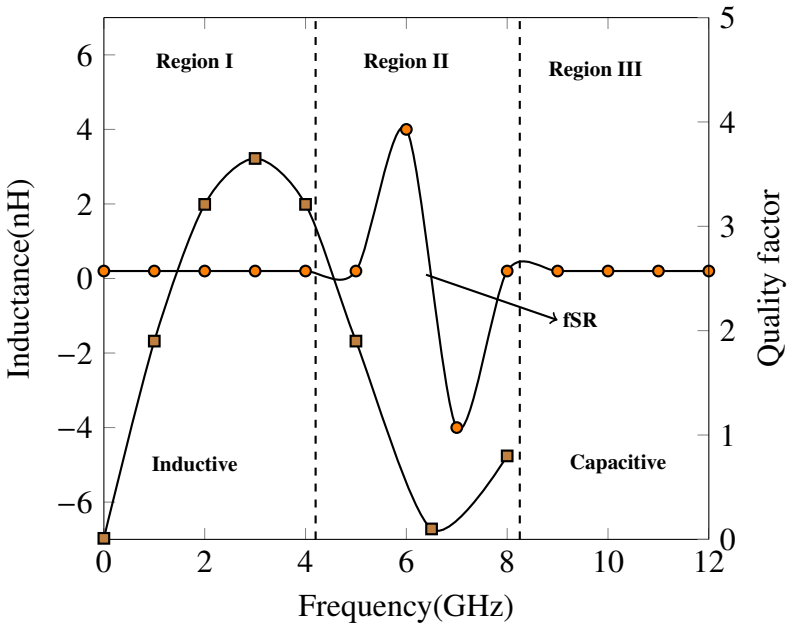
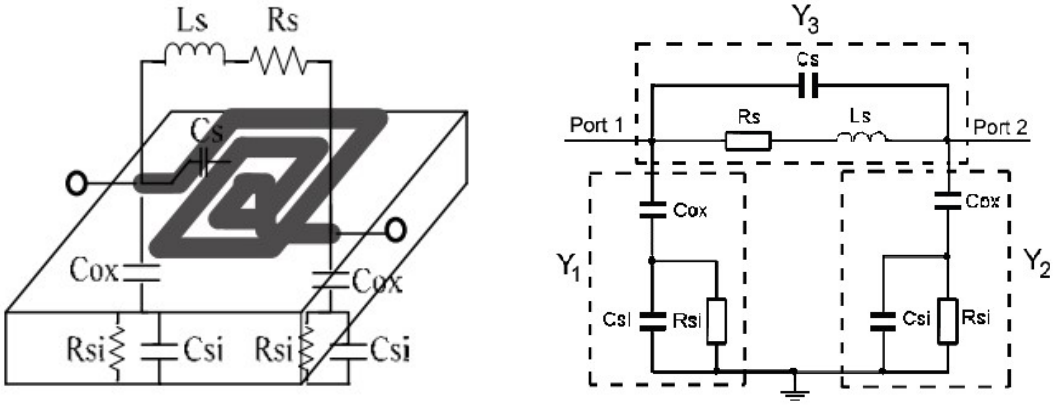


Figure 1.7: Performance metrics of on-chip inductor

These parameters can be categorized into design and process-controlled parameters. For a spiral inductor, the design-controlled parameters, also referred to as lateral parameters, include inner diameter (d_{in}), outer diameter (d_{out}), conductor width (w), spacing between adjacent conductors (s), and the number of turns (n). Process-controlled parameters, also referred to as vertical



(a) 3D view (b) Physical model of spiral inductor on Silicon

Figure 1.8: Typical π–equivalent model of spiral inductor

parameters, include metal resistivity, substrate resistivity, oxide thickness, metal thickness, and the number of metal layers. These factors determine the L, C, Q, and other parasitic elements of an inductor, such as series resistance (R_s), oxide capacitance (C_{ox}), substrate capacitance (C_{si}), substrate resistance (R_{si}), and spiral capacitance (C_s). The physical model or π-model of a spiral inductor [26] is derived based on these parameters, as illustrated in Fig. 1.8.

1.2.4 Impact of parasitics on the performance of on-chip inductor

The inductor is primarily meant to store magnetic energy, but it also has unwanted properties like resistance and capacitance, known as parasitic resistance and capacitance. The physical model depicted in Fig. 1.8 shows these parasitic elements in an on-chip inductor. This model helps analyze the inductor's performance both at low frequencies, around a few MHz, and at high frequencies, up to several GHz. The Q of an inductor is a measure of the ratio between the energy stored and the energy wasted during one cycle of excitation as given in Eq. 1.2.

$$Q = 2\pi\left(\frac{\text{Peak Magnetic Energy - Peak Electrical Energy}}{\text{Energy loss in one oscillation cycle}}\right) \tag{1.2}$$

The Q of the on-chip inductor, which is installed on a silicon substrate, is determined by the physical model and may be found in Eq. 1.3.

$$Q = \underbrace{\frac{\omega L}{R_s}}_{\text{ohmic loss}} \cdot \underbrace{\frac{R_p}{\left(R_p + \left[(\omega L/R_s)^2 + 1\right]R_s\right)}}_{\text{substrate loss}} \cdot \underbrace{\left[1 - \frac{R_s^2\left(C_s + C_p\right)}{L} - \omega^2 L\left(C_s + C_p\right)\right]}_{\text{self-resonance factor}} \tag{1.3}$$

where,

$$R_p = \frac{1}{\omega^2 C_{ox} R_{Si}} + \frac{R_{Si}(C_{ox} + C_{Si})^2}{C_{ox}^2} \tag{1.4}$$

$$C_p = C_{ox}.\frac{1 + \omega^2(C_{ox} + C_{Si})C_{Si}R_{Si}^2}{1 + \omega^2(C_{ox} + C_{Si})^2 R_{Si}^2} \tag{1.5}$$

The inductor's self-resonance frequency (f_{SR}) is represented in Eq.1.6.

$$f_{SR} = \frac{1}{2\pi\sqrt{LC_{eq}}}. \tag{1.6}$$

where, ω represents the angular frequency of the stored energy, R_p and C_p are the combined parasitic resistance, capacitance values and C_{eq} represents the total parasitic capacitance [27]. The term $\frac{\omega L}{R_s}$ presents both the stored magnetic energy and the ohmic loss due to series resistance. As we move into higher frequencies, particularly in the GHz range, the Q factor

tends to decrease. This decrease is primarily attributed to a combination of substrate loss and self-resonance effects. The substrate loss essentially arises from the penetration of electrically induced displacement current between the metal and the substrate. This can be accurately modeled using a substrate RC network that includes components like C_{ox}, R_{Si}, and C_{Si}, as depicted in Fig. 1.8. For on-chip inductors commonly used, this substrate loss factor typically results in a reduction of Q by 10 to 40% [26].

At high frequencies, the L value of an inductor is influenced not only by its Q factor but also by substrate losses caused by the magnetic field. This substrate loss can be understood as the mutual inductance between the metal components and the substrate [28]. When magnetically induced eddy currents occur, they flow in the opposite direction to the current in the coil. This leads to an increase in negative mutual inductance, reducing the total inductance and consequently lowering the Q factor [26]. In the GHz range, current crowding in the conductor decreases the skin depth, which in turn increases resistance. This rise in series resistance further reduces the Q factor. The behavior of multilayer inductors and multipath inductors at high frequencies can be effectively explained using a multilayer physical model [29, 30, 31], which is an extension of the single-layer physical model. Beyond the peak Q frequency (f_{Qmax}), the inductor's performance worsens due to increased substrate losses and the effects of current crowding.

The Y-parameters for inductors in the π-model can be calculated directly from the series and shunt impedances of the network [27]. The inductance, Q factor, and series resistance can be obtained from these Y-parameters using Eq. 1.7, Eq. 1.8, and Eq. 1.9 [32], respectively.

$$L = Im(\frac{-1}{2\pi f Y_{11}}) \tag{1.7}$$

$$Q = \frac{Im(Y_{11})}{Re(Y_{11})} \tag{1.8}$$

$$R_s = \frac{1}{Re(Y_{12})}. \tag{1.9}$$

1.2.5 Losses in spiral inductor

The performance of the spiral inductor deteriorates at high frequencies due to substrate losses and ohmic losses [33]. Substrate losses occur because electric and magnetic fields penetrate into the substrate, as illustrated in Fig. 1.9. Ohmic losses, also known as metal losses, result from uneven current distribution in the metal caused by skin effect and proximity effect [34].

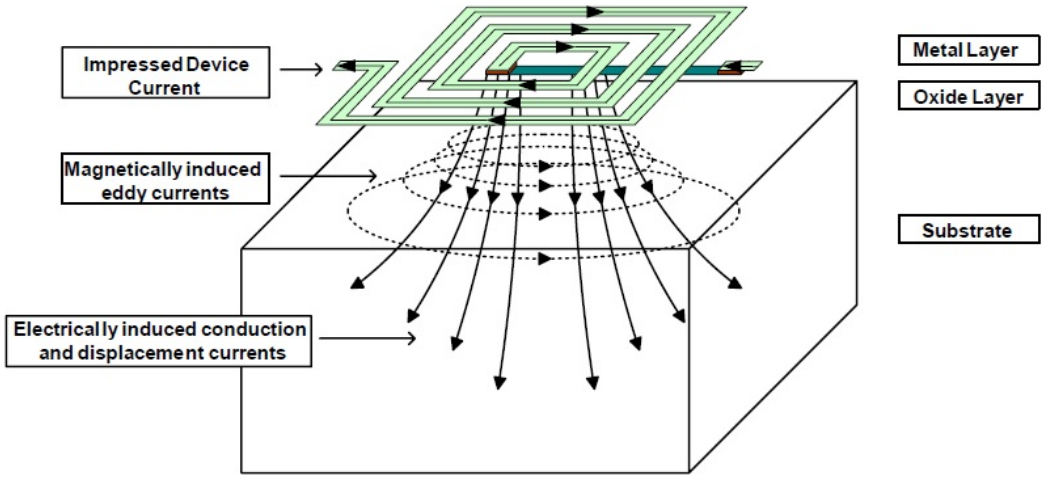


Figure 1.9: Substrate losses in spiral

The skin effect describes how high-frequency magnetic fields preferentially flow along the surface of a metal conductor, causing uneven current distribution. This is closely related to the proximity effect, where magnetic fields from adjacent metal lines further influence the current distribution. Both effects together increase the apparent resistance of the metal trace. As a result, at elevated frequencies, these phenomena elevate the inductor's series resistance and lower its Q-factor, as shown in Figure 1.10.

To improve the performance of spiral inductors, various techniques have been proposed to enhance key metrics such as Q factor and inductance. Methods like substrate etching [35], incorporating a patterned ground shield [36] beneath the inductor, and using high-resistivity substrates [37] have been effective in reducing substrate losses and improving the Q factor. However, these approaches often come with complex and costly fabrication processes and are not easily compatible with other active MOS devices. The performance of spiral inductors can be significantly improved by using them in multilayer configurations. In these setups, spiral inductors can be organized either in series or parallel across different metal layers. When arranged

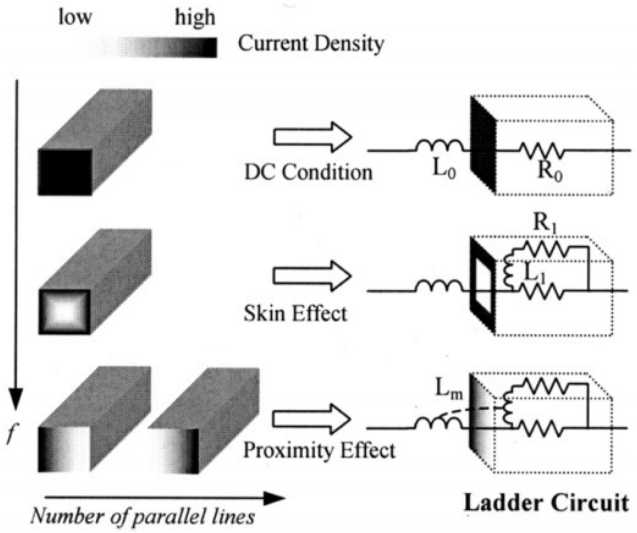


Figure 1.10: Variation of skin and proximity effects with frequency

in series, they increase the overall inductance without needing extra on-chip space compared to a single-layer inductor [38]. Conversely, connecting the metal layers in parallel [39] increases the effective metal thickness, which lowers the series resistance and improves the Q factor.

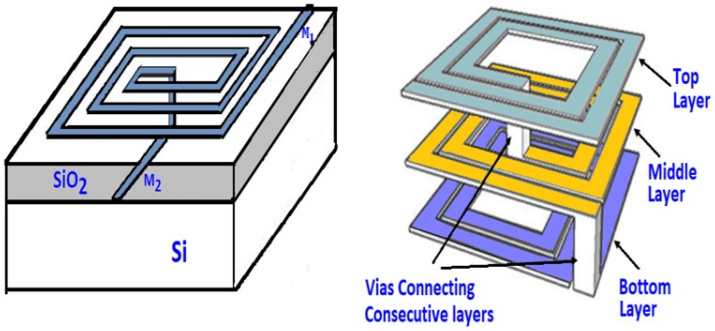


Figure 1.11: Multilayer (3 layer) Inductor and a 3D Inductor

Advanced CMOS RFIC fabrication techniques now support the stacking and linking of multiple metal layers in a sequential arrangement, referred to as series stacking. This advancement facilitates the development of multilayer inductors with significantly enhanced inductance compared to conventional planar inductors [40]. Even though they occupy the same chip area as planar inductors, multilayer inductors offer superior L and Q factor. This makes them well-suited for compact designs within the limited space of a chip, especially for 5G RFIC applications. Fig. 1.11 presents a typical configuration of a multilayer inductor.

1.2.6 Differential inductor

Spiral inductors can be divided into two main categories based on their port arrangement: symmetrical and asymmetrical. In an asymmetrical spiral inductor, also called a conventional spiral inductor, the ports are placed on opposite sides of the structure, as shown in Fig. 1.12. Conversely, symmetrical spiral inductors have their ports on a single side of the structure. The

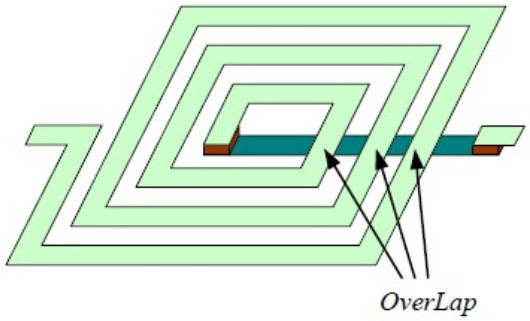


Figure 1.12: Asymmetrical spiral inductor

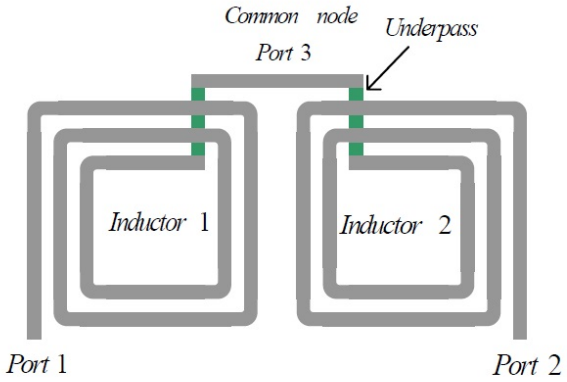


Figure 1.13: Symmetric spiral inductor using two asymmetrical spiral inductors

conventional asymmetrical inductor, illustrated in Fig. 1.13, requires a pair of these inductors, leading to a larger footprint on the chip. In contrast, a fully symmetrical inductor, as seen in Fig. 1.14, is formed by connecting two separate spirals with a single spiral that spans across an axis of symmetry. This connection involves multiple cross-over and cross-under links, enabling it to occupy a smaller area on the chip [41]. Rabjohn [42] first introduced this winding technique for connecting both the primary and secondary coils in monolithic transformers. Lately, there have been notable strides in multilayer differential inductor technology, achieving superior performance while also reducing the required space. Fractal inductors have also entered the

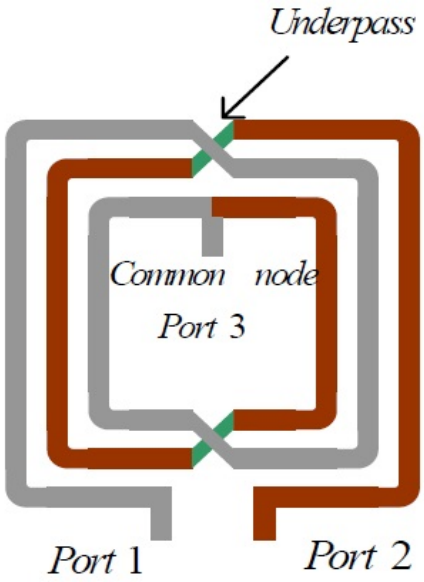


Figure 1.14: Symmetric spiral inductor

field, providing higher inductance values without needing a larger area. These fractal designs are rooted in mathematical space-filling curves that fill an area through iterative patterns. They come in various forms, offering a flexible geometric basis for crafting inductor and capacitor designs. RFIC designers have adeptly incorporated fractal geometry into wireless technology, tapping into its potential to shrink IPD passive components in RFIC and MMIC applications. Additionally, fractal capacitors deliver increased capacitance within a single layer [43]. However, it's important to highlight that designing these fractal inductors can be intricate and might lead to higher production costs.

1.3 On-chip capacitors

On-chip capacitors are specialized components found within ICs that serve to shield RFICs from interference caused by noise. These capacitors can be positioned either on the package substrates or directly embedded within the semiconductor die. Their capacitance is determined by both the capacitor's physical dimensions and the dielectric constant of the semiconductor material. On-chip capacitors are integral to various functions such as impedance matching networks, Voltage-Controlled Oscillators (VCOs), tuned resonators, and Band Pass Filter (BPF) circuits [44]. Important performance measures for RF capacitors include capacitance density, breakdown voltage, Q factor, and linearity. To evaluate capacitance and Q factor at high frequencies, engineers often rely on obtaining S-parameters through either electromagnetic (EM)

simulation tools or a vector network analyzer (VNA). MOS capacitors feature a structure simi-

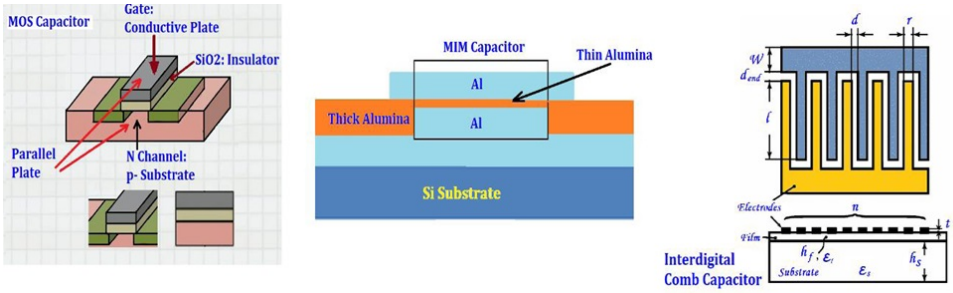


Figure 1.15: Generic structure of MOS, MIM and interdigital capacitors

lar to MOS transistors, incorporating a thin oxide layer as the gate insulator. These capacitors function as varactors, meaning their capacitance changes in response to applied DC voltage. However, variations in capacitance can result from depletion effects or charge build-up at the oxide layer boundary. To address these issues, Metal-insulator-metal (MIM) capacitors have become more popular [45]. They consist of a high-k dielectric layer between two metal layers. MIM capacitors rely solely on the electric field between the metal layers, reducing susceptibility to substrate effects. However, they tend to require more on-chip space and don't scale as efficiently with technological advancements. On the other hand, interdigital capacitors, also known as metal fringe capacitors, employ an interdigital design to harness fringing fields, achieving enhanced capacitance [46]. While they offer advantages in capacitance, interdigital capacitors are susceptible to parasitic effects. Fig. 1.15 provides an overview of these capacitor structures. Spiral capacitors can be efficiently designed and simulated in SONNET by

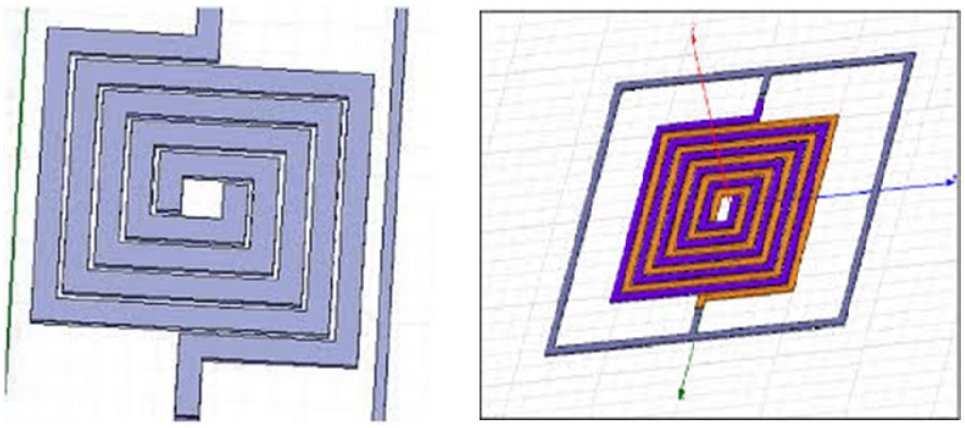


Figure 1.16: Generic structure of the spiral and fractal capacitors

adjusting the parameters of the metal, dielectric, and substrate layers to align with CMOS technology [47]. Research has indicated that using spiral geometry can boost capacitance by more than 10%, enhance the Q value by 50%, and elevate the SRF by 20% compared to traditional fractal capacitors [48]. Further, the design and fabrication of fractal capacitors can be intricate

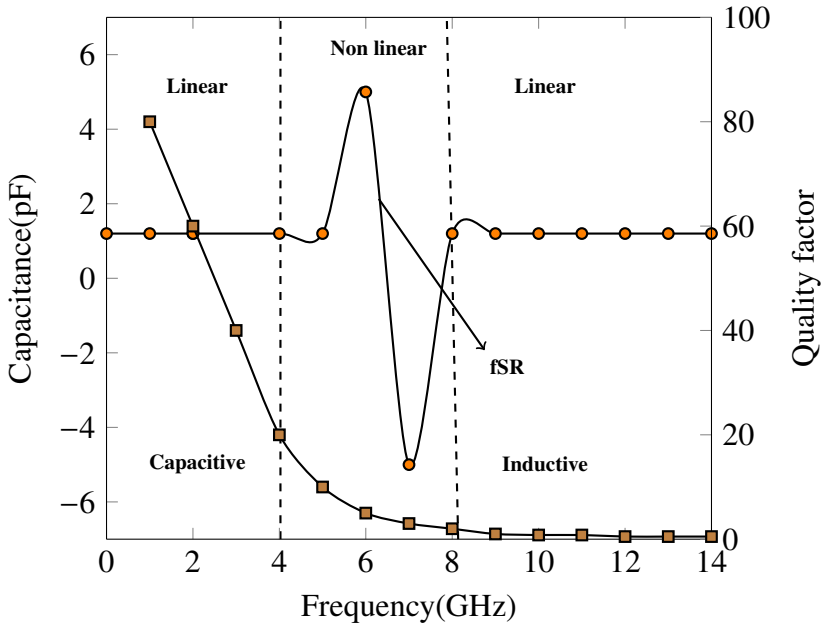


Figure 1.17: Performance metrics of on-chip capacitor

and expensive. Fig. 1.16 showcases the configurations of these on-chip capacitors, which are particularly suitable for RFIC applications. The on-chip capacitor's performance is evaluated based on its capacitance per area, Q factor, and self-resonance frequency, as illustrated in Fig. 1.17. The capacitance and Q factor values can be calculated using Eq. 1.10 and Eq. 1.11

$$Capacitance = \frac{-Im[Y_{21}]}{2\pi f} \tag{1.10}$$

$$Q\ factor = \frac{Im[Y_{11}]}{Re[Y_{11}]} \tag{1.11}$$

1.4 Low Noise Amplifier

Low noise amplifiers (LNAs) play a crucial role in wireless communication systems by amplifying weak input signals. They are vital for receivers as they enhance the signal to minimize subsequent noise without adding much noise themselves. Important factors to consider when evaluating LNAs are their amplification level, noise figure (NF), input impedance matching, energy consumption, linearity, and reliability.

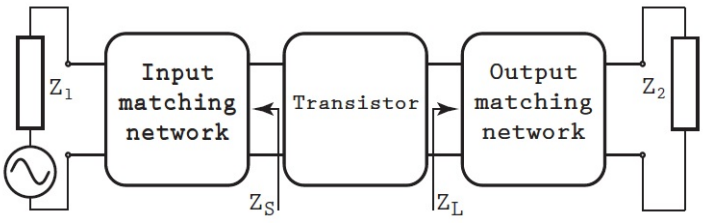


Figure 1.18: Block diagram of LNA

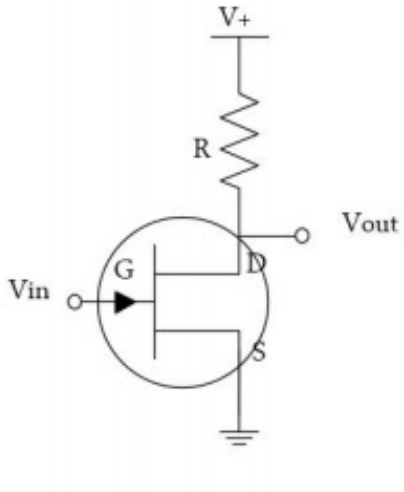


Figure 1.19: Common source

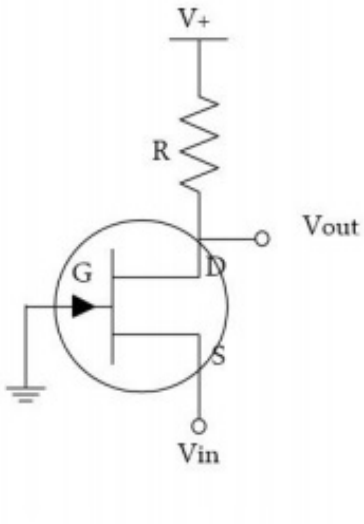


Figure 1.20: Common gate

LNA circuits commonly feature a universal topology comprising three primary stages: the input matching network, the transistor amplifier, and the output matching network, as depicted in Fig. 1.18. There's a variety of LNA designs described in the literature, each with its pros and cons. In CMOS LNA designs, the common source (CS) and common gate (CG) configurations are the most prevalent as illustrated in Fig. 1.19 and Fig. 1.20, respectively. The CS LNA is known for delivering high gain and impressive noise performance [49]. However, its bandwidth can be constrained due to the miller effect. To overcome this limitation, an inductor can be added to the source of the CS stage, resulting in the inductive source degeneration topology. This modification boosts both the gain and noise performance, making the CS LNA with inductive degeneration ideal for narrowband LNA designs [50]. Conversely, the CG LNA offers advantages like superior input matching, reverse isolation, linearity, and broader bandwidth. Nonetheless, it often falls short in noise performance. To improve this, techniques such as capacitive cross-coupling has been developed to enhance the noise characteristics of the CG stage [51, 52, 53]. The CG setup excels in wideband input matching, which has made it a preferred option for broadband LNA designs [54, 55, 56]. The cascode LNA illustrated

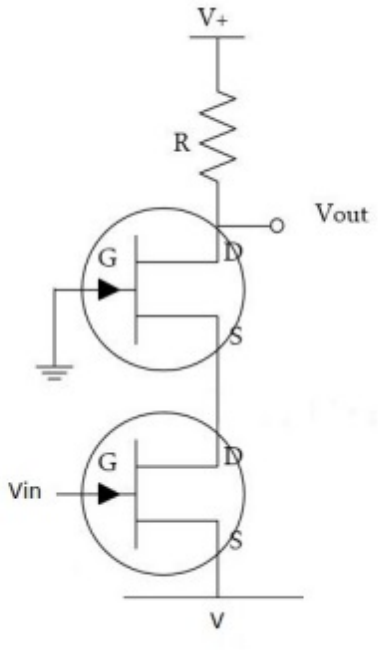


Figure 1.21: Cascode LNA

in Fig. 1.21 offers outstanding noise performance, high power gain, low power consumption, and improved reverse isolation [57, 58, 59]. However, its noise and gain characteristics tend to deteriorate at extremely high microwave frequencies. This degradation is primarily attributed to the rising substrate parasitic admittance at the drain-source common node with increasing frequency [60, 61]. While the cascode stage is well-suited for narrowband applications similar to the CS stage, incorporating feedback techniques can extend its use to multi-band and wide-band applications [62, 63]. Additionally, the cascode configuration can be adapted for wideband applications by employing complex LC matching networks at the input [64].

Distributed amplifiers (DA) [65] and multistage LNAs [66] are known for their ability to achieve broadband input matching, high gain, and wide operation. However, these designs often face challenges in reducing power consumption and on-chip area due to their multiple cascading stages. On the other hand, current-reuse LNAs are recognized for delivering high performance while consuming less power, maintaining flat gain, low NF, excellent linearity, and good input matching [67, 68].

1.5 Voltage Controlled Oscillator

Voltage-Controlled Oscillators (VCOs) stand as pivotal components in electronic circuits, where the oscillation frequency of the signal generated upon the voltage applied to them. Their versatility lies in the ability to generate AC signals, with frequencies directly tied to the input voltage, enabling adaptability across various applications. Fundamentally, VCOs operate on the principle of energy transfer between different forms within a circuit. This is often achieved through an LC circuit [69]. In this setup, energy oscillates between the L and C. Initially, the capacitor stores energy as an electric field between its plates, which then discharges through the inductor, storing it as a magnetic field. The inductor subsequently releases this stored energy, charging the capacitor, thus initiating a repeating cycle. The frequency of this oscillation is determined by the resonant frequency of the LC circuit, which is proportional to the square root of the product of the inductance and capacitance. The utility of VCOs extends broadly across electronic systems, notably in Phase-Locked Loops (PLLs). A PLL is a control system that generates an output signal with a fixed phase relationship to a reference signal. VCOs within PLLs are instrumental in aligning the output frequency with that of the reference signal, facilitating tasks such as frequency synthesis and synchronization. Beyond PLLs, VCOs serve diverse applications in frequency and phase modulation, function generators, synthesizers, telecommunications, radio, and computing systems.

In VCOs, on-chip inductors play a crucial role in determining the oscillation frequency and overall performance of the circuit. These inductors are typically integrated directly onto the semiconductor substrate, alongside other active and passive components, to minimize parasitic effects and optimize performance. The primary function of on-chip inductors in VCOs is to provide the necessary energy storage for the oscillation process. When a voltage is applied to the VCO, it generates an oscillating signal whose frequency is determined by the resonant frequency of the LC tank circuit formed by the on-chip inductor and a capacitor. The inductor stores energy in the form of a magnetic field, while the capacitor stores energy in an electric field. Together, they create a resonant circuit that oscillates at a frequency determined by their combined values. The Q-factor of the on-chip inductor is a critical parameter that significantly influences the performance of the VCO. A higher Q-factor indicates lower energy losses in the inductor, resulting in a more stable and efficient oscillation. Achieving a high Q-factor requires careful design and fabrication techniques to minimize resistive and parasitic losses within the inductor structure. Another important consideration is the inductance value of the on-chip inductor, which directly impacts the oscillation frequency range and tuning sensitivity of the VCO. By adjusting the voltage applied to the VCO, the effective capacitance and

inductance can be varied, allowing for frequency modulation or tuning. Therefore, the design of the on-chip inductor must strike a balance between achieving the desired inductance value and minimizing parasitic effects to ensure accurate frequency control and stability. Additionally, on-chip inductors can be susceptible to external interference and noise, which can degrade the performance of the VCO. Proper shielding and isolation techniques may be employed to mitigate these effects and improve the overall reliability of the oscillator circuit.

1.6 Design tool and Measurement setup

Passive components on ICs are commonly designed and analyzed using EM simulation software like HFSS, SONNET, and ADS. SONNET uses the Finite Element Method (FEM) for its simulations, breaking down the component into small sections or mesh elements. Through applying appropriate boundary conditions and solving Maxwell's equations, SONNET produces a scattering matrix that accurately evaluates the component's behavior. Here is a simplified breakdown of the SONNET simulation process:

- Meshing: Divide the component structure into mesh elements.
- Field Computation: Calculate the electromagnetic fields within the structure at the specific frequency.
- Error Calculation: Determine the discrepancy between the simulation and desired results.
- Adjustment: If the error is too high, refine the mesh and re-evaluate.
- Iteration: Continue the simulation and adjustment process until the error reaches an acceptable level. One of the advantages is, ability to simulate across a wide frequency range without the need to change the mesh.

1.7 Motivation

The evolution of communication devices relies heavily on ICs, especially in analog subsystems like LNAs, VCOs, and filters. On-chip inductors are crucial components within these subsystems. However, losses in on-chip inductors often require the use of external ones for narrow band subsystems, complicating design and introduces parasitics. There is a need for

compact, high-inductance, high-quality factor on-chip inductors to simplify design and improve performance. While researchers have proposed various designs, there is still room for improvement in both quality factor and size. Multilayer inductors offer promise in addressing these challenges.

1.8 Problem statement

Developing a compact, high-performance multilayer on-chip inductor tailored for RF applications to optimize system functionality by maximizing Q-factor while minimizing the area.

1.9 Objectives

The objective of this research is to enhance system performance in high-frequency RF applications through the development of advanced on-chip inductors.

- Designing a high-Q split inductor with half-turns for RF use.
- Introducing a pyramid-shaped inductor and multilayer inductor.
- Creating a pyramid and high-Q multilayer inductor based VCO for telemetry transponder applications.
- Creating a low-noise figure LNA by employing an coupled pyramid and multilayer inductor.

1.10 Organization of Work

In this thesis the design and simulation of multilayer on-chip inductors is carried out in the standard CMOS process. To address the challenge posed by the unavailability of inductor fabrication on silicon, the designed models are downscaled to lower frequencies and fabricated on FR-4 substrate. This approach enables the assessment of inductor performance under practical conditions, facilitating a comprehensive evaluation of their effectiveness at high frequencies. This section gives a brief summary of all chapters.

Chapter 1 This chapter presents the introduction of on-chip inductor designs in integrated circuits. It provides an overview of various inductor configurations with their advantages and disadvantages followed by problem statement of the research work.

Chapter 2 This chapter provides a thorough examination of inductors, covering their conceptual framework and advancements. It presents various inductor configurations and their practical applications. The review starts from the design of the on-chip inductor to the state-of-the-art inductors designed by various researchers.

Chapter 3 In this chapter, the design of planar, half-turn split inductor, coupled pyramid and high Q Multi-Layer Inductors are proposed and analyzed.

Chapter 4 This chapter elaborates on the theoretical foundations and mathematical analysis behind the configurations of the spiral on-chip inductors. It also illustrates the equivalent circuits proposed by the researchers. The mechanisms used to enhance the inductance and quality factor are also discussed. The causes for the reduction in quality factors are elaborated on in this chapter for the comprehensibility of the readers.

Chapter 5 This chapter presents a Coupled Pyramid and multilayer inductor based VCO design with high figure of merit (FoM) for Telemetry Transponder Applications.

Chapter 6 In this, the design and analysis of a Low Noise Amplifier (LNA) with a Coupled Pyramid and multi layer Inductor Structure is presented.

Chapter 7 The overall conclusions drawn from each contribution are detailed in this chapter, along with the future scope of the work.

Chapter 2

Literature Survey

2.1 Introduction

The rapid expansion of both wireless and wired communication has incited a significant interest in the development of low-cost radio frequency integrated circuits (RFICs). These circuits offer notable advantages, such as reduced size and power consumption, which have greatly contributed to the advancement of personal communication services. The integration of radio frequency circuits brings several benefits, primarily in terms of size reduction and energy efficiency. This integration has been made possible through the research conducted over the past four decades in the field of micro devices. By incorporating elements like resistors, capacitors, diodes, and transistors onto a single chip, RFICs can achieve higher levels of compactness and energy efficiency. One noteworthy trend in this field is the growing use of on-chip inductors in radio frequency circuits. Traditionally, on-chip components included resistors, capacitors, diodes, and transistors, but recent advancements have led to the integration of inductors as well. This development is particularly evident in crucial circuits within RF front-end systems, such as low noise amplifiers, oscillators, phase-locked loops, and mixers.

2.2 Conventional On-Chip spiral inductor

In [70] E. Frlan et al., introduced a novel lumped equivalent model to elucidate the behavior of a square spiral inductor with 0.065 mm² area. This inductor was crafted on an alumina substrate, improving an inner diameter of 160 μm. At lower frequencies, the inductor demon-

strated an impressive inductance of 2 nH. However, as the frequency increased to 20 GHz, its inductance value slightly decreased to 1.75 nH.

In [71], N.M. Nguyen, et al., explored the design and fabrication of two square spiral inductors on a standard silicon substrate. These inductors, featuring outer diameters of 230 μm and 115 μm respectively, showcased the inductance values of 9.3 nH and 1.3 nH, with corresponding self-resonance frequencies of 9.7 GHz and 2.47 GHz. Both inductors exhibited quality factor (Q) values ranging from 3 to 8, indicating their effectiveness in various frequency ranges. Leveraging these inductors, the authors successfully implemented a low pass LC filter, demonstrating superior performance in terms of input matching, linearity, and power gain. Furthermore, they developed an RF bandpass amplifier tailored for the L band (1-2 GHz) utilizing a monolithic inductor with an inductance of 4 nH in silicon bipolar technique. This amplifier achieved notable results, including a peak gain of 8 dB, a Noise Figure (NF) of 6.4 dB, and a well-matched input impedance.

In [72, 73], Yue C. Patrick, et al., contributed significantly to the advancement of on-chip inductor technology on silicon substrates. They developed a comprehensive physical model that takes into account various factors affecting inductor performance, including copper losses, substrate losses, and parasitic losses. This model provides a deep understanding of the behavior of on-chip inductors and offers insights into ways to optimize their design for improved efficiency and performance. Moreover, their research has spurred the development of innovative inductor structures in subsequent years, further expanding the possibilities for on-chip integration and enhancing the capabilities of integrated circuits in various applications.

In [74], Chang, et al., introduced an innovative approach to enhance the performance of a UHF range spiral inductor. Their method involved etching the substrate beneath the inductor, resulting in significant improvements. Specifically, they designed a 100nH inductor with an outer diameter of 440 μm. Upon experimentation, the removal of the substrate led to remarkable enhancements in the self-resonant frequency (f_{SRF}), increasing it from 800 MHz to 3GHz. Additionally, the inductor exhibited a peak Q of 4 at 400 MHz.

In [75], Min P. Park et al., conducted experiments to evaluate standard CMOS inductors fabricated on three substrates with varying resistivities. Their research aimed to assess how different substrate properties affect inductor performance. Interestingly, using a high-resistive substrate resulted in reduced substrate losses and improved Q of the inductors. Through detailed analysis, the team explored the impact of various layout parameters, such as metal thickness,

metal width, spacing, inner diameter, and number of turns, on both the Q value and inductance across all three substrates.

In [76], C. Patrick Yue and SS. Wang presented a detailed analysis of a GPS receiver circuit model featuring an integrated silicon spiral inductor, strategically shielded by a ground shield. Their study aimed to investigate the impact of high-frequency skin effects and substrate losses on the inductor's performance. They optimized the inductor at 2 GHz by adjusting parameters such as oxide capacitance and series resistance. Additionally, they examined the influence of multi-level interconnect scaling and low k on the Q of the inductor. Utilizing a 0.5 μm CMOS process with five metal layers, they observed closely matched measurement and model values for the L and Q factor, averaging around 10 nH and 6.3, respectively.

In [77] and [78], the impact of substrate resistivity on inductors is thoroughly examined. Strategies such as removing the substrate or employing high-resistivity substrates are proposed to mitigate substrate losses. Although this process improves the inductance but it suffers with poor reliability, long-lasting stability, and expensive fabrication cost.

In [79], the authors delve into the optimization of spiral inductors fabricated on silicon, accompanied by thorough layout optimization and circuit simulation. They address crucial issues such as the skin effect and substrate losses inherent in inductor modeling, emphasizing the significance of mitigating these effects for enhanced performance. The study highlights the efficacy of ground shielding techniques in reducing substrate loss and noise, offering practical insights into improving inductor design. Moreover, the authors propose a practical approach centered on balancing series resistance and oxide capacitance to optimize inductor performance. By utilizing copper and low-k dielectrics, the system overall performance, particularly in terms of Q, is significantly enhanced. Notably, the inductor characterized by an outer diameter of 470 μm exhibits an inductance of 10 nH and a quality factor of 5, underscoring the effectiveness of the proposed methodologies in achieving desirable performance metrics.

In [80], Chia-Hsin Wu et al., introduced a novel approach to inductor design, involving the shunting of selective metal layers. Their innovative structure aimed to address key challenges such as reducing series resistance and enhancing the Q. By increasing the thickness of the metal layers, series resistance was effectively reduced, leading to improvements in the Q factor of the inductor. However, a trade-off emerged as the proximity of lower metal layers to the substrate resulted in increased parasitic capacitance, thereby lowering the self-resonant frequency (f_{SRF}).

2.2.1 Multilayer on-chip spiral inductor

Planar inductors typically occupy a larger on-chip area due to their design requirements, which often necessitate a minimum of two metal layers. These layers are strategically positioned, with one located in the top metal layer and the other placed underneath, known as an underpass. However, as technology progresses, there has been a notable advancement in the realization of inductors by leveraging multiple metal layers. This evolution allows for more efficient use of space on the chip and enables the implementation of more complex and higher-performance inductor designs. By utilizing multiple metal layers, designers can optimize the layout and configuration of planar inductors, leading to improved performance and functionality in integrated circuit applications.

In [81, 82], Merrill, Burghartz et al., proposed a novel approach to inductor design using series stacked inductors within multilevel technology. This innovative technique aimed to maximize the inductance value per unit area, thereby reducing overall system costs. By stacking multiple inductors in series, designers could achieve higher inductance levels within a given space, offering greater efficiency and cost-effectiveness. However, a trade-off arises as the parasitic capacitance between consecutive metal layers increases, leading to a reduction in the f_{SRF}.

In [83], Y. Koutsoyannopoulos et al., presented a novel approach utilizing multilayer series stacked inductors, implemented in configurations of two and three layers. By connecting metal layers in series, the overall length of the metal is extended, resulting in increased inductance values. Furthermore, aligning the current direction in the top and bottom layers enhances positive mutual inductance, further amplifying the inductance. Compared to conventional planar spiral inductors occupying the same on-chip area, these multilayer series stacked inductors demonstrated a remarkable increase in inductance, up to 600%. This advancement allows for the attainment of large inductance values within minimal on-chip space, offering significant benefits in terms of efficiency and cost-effectiveness. However, it's crucial to note that the heightened parasitic capacitance between consecutive metal layers poses challenges, leading to a decrease in both the quality factor and the f_{SRF}.

In [84], Zolfaghari et al., introduced a novel two-layer series stacked multilayer inductor utilizing 0.25 μm technology, incorporating five metal layers. Notably, the placement of spirals at a greater distance from each other effectively reduces parasitic capacitance, resulting in a notably higher SRF. The inductor implemented across the top and bottom layers (M5 and M2) exhibited a significant 2-fold improvement in SRF, reaching 1.79 GHz compared to the inductor spanning the top two consecutive layers (M5 and M4) with a SRF of 0.96 GHz. Interestingly,

despite the difference in SRF, both inductors maintained consistent inductance values, each registering at 266 nH within an on-chip area of 240 μm $\times$ 240 μm. Additionally, the study explored stacked transformers, achieving a notable voltage gain of 3 (9.5 dB) at 1.5 GHz.

In [85], J.N. Burghartz et al., proposed a standard 0.8 μm BiCMOS multilayer spiral inductor comprising four metal layers, each with a width of 16 μm and a spacing of 10 μm between them. Notably, these metal layers were interconnected in parallel using via arrays, effectively increasing the effective metal thickness. This augmented thickness played a crucial role in reducing the series resistance of the inductor, consequently enhancing its Q. The inductor design featured a single metal layer (MM3) with three shunted metal layers (M2/M3/M4), resulting in Q factor values of 6.5 and 8.6, respectively, within an on-chip area of 0.051 mm².

In [86], P. Findley et al., introduced a novel approach using a differential structure to enhance the SRF of inductors. This innovative design focuses on mitigating high voltage swings and reducing the effective shunt capacitance by 50% for each port. By employing this differential configuration, the inductor achieved a remarkable 60% improvement in f_{SRF} compared to a standard differential inductor occupying the same on-chip area.

In [87], Chih-Chun Tang et al., introduced a compact 3D inductor designed within the confines of a 0.35 μm one poly four metal (1P4M) CMOS process. This innovative inductor utilized non-sequential metal layers, a departure from traditional approaches, to mitigate interlayer capacitance and enhance the SRF. Their 3D inductor design offered significant advantages, having 80% reduction in area compared to planar counterparts. Additionally, it exhibited a notable 34% improvement in SRF, although there was a slight 8% decrease in the Q to stacked inductors with equivalent on-chip area and inductance. The integration of this miniature 3D inductor enabled the realization of a 2.4 GHz CMOS LNA, effectively reducing the footprint and cost of the RFIC.

In [88], I. Iramnaaz et al., proposed a novel approach to creating high-quality RF inductors utilizing a multilayer structure comprising alternate layers of ferromagnetic films and copper materials. The key innovation lies in the suppression of the skin effect, primarily achieved through the zero-effective permeability at the ferromagnetic anti-resonant frequency. This suppression resulted in a notable increase in the Q of the inductor. Specifically, the reported inductor exhibited an inductance of 0.5 nH and a Q value of 21, with an outer diameter of 200 μm. Remarkably, this represented an 86% increase in Q value compared to inductors based on conventional copper spiral designs.

In [89], VNR Vanukuru et al., presented a novel multipath series stacking octagonal spiral inductor, with the unique feature of equal path lengths. This design innovation aimed to minimize interlayer capacitance, leading to a notable increase in the f_{SRF}. By implementing a multi-path technique, the inductor effectively mitigated both the skin effect and proximity effects, resulting in reduced AC resistance and capacitance, as well as higher inductance values. Fabricated on 180 nm Silicon on Insulator (SOI) with dual thick metal stacks, the inductor exhibited significant improvements compared to standard multipath series stacked inductors. Specifically, it demonstrated a 10% enhancement in Qmax value, a 50% improvement in Qmax frequency, and a remarkable 100% increase in f_{SRF}.

In [90], G. Haobijam et al., investigated a novel Multilayer Pyramidal inductor, implemented across six layers using 0.18 μm technology. This innovative design consists of two up and down inductors connected in series, forming the MPS (Multilayer Pyramidal Spiral) inductor structure. With a differential excitation approach, the MPS inductor achieves a significant inductance value of 23nH. Moreover, compared to conventional planar inductors, it exhibits notable improvements, including a nearly 20% enhancement in the Q factor and a remarkable 30.6% improvement in the f_{SRF}.

In [91], Tang et al., proposed a novel miniature 3D inductor design. This structure involves connecting two or more stacked inductors in series, with each stacked inductor featuring only one metal turn in every metal layer. One of the key advantages of this design is the reduction in metal-to-metal capacitance, resulting in a higher SRF. Compared to traditional stacked inductors, the miniature 3D inductor showcased a notable 34% improvement in SRF. However, there was a slight trade-off, as the Q factor experienced an 8% degradation relative to stacked inductors with the same inductance value.

In [92], Xiangming Xu et al., introduced a novel multipath crossover interconnection octagon stacked spiral inductor fabricated using the 0.13 μm SiGe BiCMOS process. This innovative design incorporates a technique where the metal wire of the spiral inductor is segmented into multiple paths based on the process rules and the depth of skin effects at the response frequency. Each individual path's width is carefully controlled to be equal to or less than the skin depth, effectively mitigating proximity and skin effects, thus enhancing the inductor's Q-factor and reducing its footprint. Additionally, a crossover-interconnection method is employed to equalize the total path lengths, minimizing the current-crowding effect and further enhancing the Q-factor. Compared to conventional stacked and planar inductors, the proposed design achieved remarkable improvements, with a 63.8% enhancement in peak Q-factor (2.3 GHz) relative to stacked inductors (1.5 GHz) and a 44% improvement compared to planar inductors.

The proposed inductor demonstrated a Q value of 9.78 at 2.3 GHz, improving an inductance of 8.2 nH while occupying a compact on-chip area of 0.0289 mm².

2.2.2 On-chip VCO design

In [93], J. Burghartz et al., fabricated a square spiral inductor with specific dimensions: 10 μm width, 3.5 μm spacing, and occupying an on-chip area of 160 x 160 μm. This inductor exhibited an inductance of 2.45 nH, a Qmax value of 9.7, and a self-resonance frequency (SRF) of 5.3 GHz. Leveraging this high-Q square spiral inductor, the researchers implemented various RF circuits, including a LNA, Voltage-Controlled Oscillator (VCO), and Bandpass Filter (BPF). Through these implementations, notable improvements were observed across different performance metrics. The BPF demonstrated a significant enhancement in insertion loss by more than 5 dB, while the LNA exhibited higher gain, reduced power consumption, and lower Noise Figure (NF). Additionally, the VCO achieved power savings and a remarkable 7 dB improvement in phase noise.

In [94], Joonchul Kim et al., proposed a miniature Symmetric Trace Differential Stacked Spiral Inductor (SDSSI) using standard 0.18 μm CMOS technology. Despite employing a stacking technique, the SDSSI achieved a high SRF and Q by strategically reducing parasitic capacitance between layers. This was achieved by alternating the placement of traces at different positions in each layer. Subsequently, a VCO was implemented using the SDSSI, exhibiting impressive performance metrics. The VCO yielded an output power spectrum of 0.79 dBm and a phase noise of 114 dBc/Hz at a 1-MHz offset frequency. Notably, the oscillation frequencies of the VCO spanned from 1.84 GHz to 2.38 GHz, with a tuning range of 26%. The on-chip area occupied by the SDSSI and VCO was compact, measuring 80 μm² and 350 μm², respectively. The SDSSI boasted an inductance of 5 nH and a self-resonance frequency of 11 GHz.

In [95], a low noise and low power 5.8 GHz VCO utilizing an on-chip MEMS inductor is introduced. Fabricated within a one-poly six-metal CMOS process using 0.18 μm technology, this oscillator incorporates the chip implementation centering technique and micromachining post-process. Through micromachining, the oxide between metals and silicon is eliminated, resulting in improved Q and L values of the inductor. Specifically designed for use in a 5.8 GHz VCO, the inductor achieves a maximum L value of 1.88nH and a Q of 15. Notably, the CMOS MEMS inductor demonstrates an impressive 88% enhancement in Q compared to a standard CMOS inductor.

In [96], a 3-D integrated coil inductor is developed on silicon for a 10 GHz LC type VCO, specifically tailored for low jitter VCO applications in high data rate communication systems. The primary objective is to enhance the Q factor of the inductor, crucial for achieving optimal performance in high-frequency circuits. Through the adoption of compliant interconnect processing methods, the inductor achieves a remarkable inductance value of 1nH at a frequency of 10 GHz, coupled with a Q factor exceeding 50. To attain these performance metrics, an outer diameter of 140 μm to 200 μm is considered, ensuring the compatibility of the inductor with the desired application requirements.

In [97], Deepak Balodi et al., introduced a pioneering approach to designing an on-chip inductor LC- VCO for S-band applications, prioritizing low power consumption and minimal phase noise. By employing a low bias voltage of 1.2 V in a cross-coupled differential structure, they effectively compensated for losses within the LC resonator, resulting in remarkably low power dissipation of 8.56 mW, VCO's high gain and low noise requirements. They opted for a moderate L value of 8 nH for the tank inductor while ensuring a very high Q, maintaining optimal performance for the VCO frequencies outlined in their local oscillator (LO) plan. Their design achieved an exceptional phase noise level of -140 dBc/Hz at a 1MHz offset, surpassing contemporary designs and demonstrating the efficacy of their approach in minimizing phase noise while maximizing efficiency in S-band applications.

In [98], Sang-woong et al., presented a novel 0.35 μm CMOS VCO with a high-Q inductor held in a wafer-level package (WLP), for a significant advancement in integrated circuit design. The WLP inductor was ingeniously implemented using the redistribution metal layer of the WLP, showcasing a better Q-factor of 8 at 2 GHz. This high-Q inductor design enhances the performance of the LC-resonator within the VCO. Notably, the VCO demonstrated exceptional power efficiency, consuming only 1.87 mW, while achieving a minimum phase noise of –120.2 dBc/Hz at a 600 KHz offset. Furthermore, the VCO featured a wide tuning range of 385 MHz, catering to various frequency modulation requirements.

In [99], Heesauk Jhon et al., showcased a VCO constructed using a 1 poly and 6 metal mixed signal standard CMOS process, representing a notable advancement in integrated circuitry. A key innovation was the incorporation of patterned-ground shields (PGS) beneath the spiral to enhance the Q of the inductor within the LC resonator, despite thin metal thickness. This adoption effectively mitigated the effects of the low resistive Si substrates AC current, optimizing performance. The resultant LC VCO exhibited better characteristics, with a 2.1 mW of DC power consumption and a phase noise of -123.7 dBc/Hz at a 1-MHz offset, operating at a frequency of 2.62 GHz. Moreover, the integration of a vertical shunt inductor with PGS

addressed critical challenges associated with thin metal thickness and the low resistivity of the logic CMOS process, ensuring robust compensation.

In [100], Miyoung Lee et al., introduced a high-performance symmetrical differential inductor tailored for small chip area and high Q-factor VCO (QVCO). Utilizing a 0.13-μm TSMC process, they designed the proposed inductor with a two-turn octagonal structure, a design choice that effectively minimized chip area while enhancing phase noise characteristics. They further implemented this innovative inductor design in a QVCO, offering a wide operating range spanning 20% from 4.5 to 5.5 GHz. The QVCO exhibited better phase noise performance, measuring 119.7 dBc/Hz at a 1 MHz offset from 5.15 GHz. Notably, the proposed QVCO resulted a negligible output phase error of less than 0.5° and consumed a total power of 5.4 mW at a supply of 1.2 V. Additionally, the adoption of the symmetrical differential inductor in the QVCO significantly improved output voltage swing and phase noise by 75% and 10 dB, respectively, for a given power consumption.

2.2.3 On-chip LNA design

The first stage in amplifying the signal in any receiver is the LNA, and it holds significant affect over the overall noise performance. Designing an effective LNA is quite challenging due to the array of objectives it must meet: achieving a low Noise Figure (NF), high gain, minimal power consumption, excellent input matching, and strong linearity.

In [101], Pourmand et al. introduced a fully integrated 0.18μm CMOS cascode LNA featuring an on-chip spiral inductor matching network, tailored specifically for IEEE 802.11a applications. The LNA showcased notable achievements, importantly in power efficiency and performance metrics. Efforts were made to curtail LNA power consumption, resulting in an impressive reduction to just 16 mW. Despite this reduction, the LNA managed to maintain a gain of 17.82 dB and a reverse isolation of -58.37 dB at 5.5 GHz. The values of S_{11} and S_{22}, indicating input and output reflection coefficients respectively, stood at -16.1 dB and -32 dB, attesting to the amplifier's strong matching characteristics. Moreover, the LNA exhibited an IIP3 (third-order input intercept point) of +3 dBm, signifying its ability to handle nonlinear distortion, and improved a NF of less than 2.9 dB, affirming its capability to maintain signal fidelity even in the presence of noise.

In [102], Masumesh Shams et al. presented a comprehensive study on a three-stage, 3-10.6 GHz wideband Ultra-Wideband (UWB) LNA implemented in 130 nm CMOS technology. The

LNA architecture incorporated several innovative techniques to achieve broad frequency coverage and maintain desirable performance characteristics. The design elements were strategically chosen to enhance performance metrics across the frequency spectrum. The LNA demonstrated a better power gain of 17 dB, indicating its ability to amplify weak signals effectively. Despite its broad frequency range, the LNA managed to maintain a NF of 5.5 dB, ensuring minimal degradation of signal quality due to internal noise. Additionally, the LNA exhibited an IIP3 of -7.7 dBm, which is indicative of its robustness against nonlinear distortion effects. Furthermore, the LNA achieved a power consumption of 15 mW from a 1 V power supply, highlighting its efficiency in power usage. The S_{11} and S_{22} is measured at -10 dB and -25 dB, respectively underscoring the LNA's capability to match with input and output impedances effectively.

In [103], Zhengmin Ke et al. introduced an advancement in LNA technology with a compact, LNA operating at 5 GHz. This LNA, designed using the SISL (Substrate Integrated Suspended Line) platform and employing a pHEMT (pseudomorphic High Electron Mobility Transistor) transistor, showcased remarkable performance attributes. One notable feature of this LNA is its compact and self-packaged structure, incorporating an air cavity. This design choice not only simplifies fabrication, especially when implemented on a PCB, but also offers distinct advantages such as reduced size and lower dielectric losses.

In [104], T Sunil Kumar et al., introduced an innovative approach to designing a high-performance LNA tailored for the 5G band, operating at 28 GHz. They utilized the orthogonal series stacked inductor in a 90nm CMOS technology. A significant aspect of their contribution was the use of a multilayer PCB fabricated fractal inductor, which demonstrated notable improvements over a standard fractal inductor in terms of inductance, Q factor, and series resistance. The measured results indicated that the multilayer PCB fractal inductor doubled the inductance, increased the Q factor by 56%, and reduced series resistance by 33%, all achieved within an equivalent on-chip area. By incorporating this enhanced inductor into their LNA design, the researchers were able to achieve impressive performance metrics. The LNA improved an enhanced gain of 30.668 dB, and NF of just 0.7 dB, indicating minimal degradation of signal quality due to internal noise. Furthermore, the LNA demonstrated efficient power usage, consuming only 5 mW from a 2.2 V power supply, within the desired frequency range of 27-30 GHz.

In [105], Fanucci L et al., presented a fully integrated LNA tailored for 3V operation. The design featured a bootstrapped inductor along with a preselecting input filter, aiming to optimize performance in terms of gain, bandwidth, and NF. One notable achievement of this LNA was its gain of 36 dB, indicating its ability to amplify weak signals effectively. The use

of a bootstrapped inductor contributed to this high gain by enhancing the LNA's impedance matching and overall efficiency. The LNA exhibited a Q value of 13 and a wide bandwidth of 140 MHz, ensuring compatibility with a variety of communication standards and applications. Furthermore, the LNA maintained a low NF of just 2 dB at 1.8 GHz, highlighting its capability to preserve signal fidelity even in the presence of noise. However, it's worth noting that despite these impressive performance metrics, the manufactured LNA IC exhibited a relatively small dynamic range, with a 1 dB compression point measured at -46 dBm.

In [106], D Linten et al. introduced a groundbreaking design: a low-power, fully integrated LNA operating at 5.5 GHz, utilizing 90 nm RF CMOS technology with built-in electrostatic discharge (ESD) protection. One of the key achievements of this LNA was its power gain of 13.3 dB, which signifies its ability to amplify signals effectively at the desired frequency. Additionally, the return loss of -14 dB indicates good impedance matching at the input, ensuring minimal signal reflection. The LNA exhibited a wide bandwidth of 1.35 GHz, enabling it to accommodate a range of signal frequencies within the 5.5 GHz band. Despite its high performance, the power consumption of the LNA remained low, measured at 9.7 mW, which is crucial for energy-efficient operation in battery-powered devices. Furthermore, the LNA demonstrated a low NF of 2.9 dB, indicating minimal degradation of signal quality due to internal noise.

In [107], P. P. Moghadam et al. introduced an innovative inductorless wideband LNA, addressing challenges of wide bandwidth, impedance matching, and low power. They employed a Cascode Common-Gate stage with current-steering and reuse techniques for efficiency. Simulated in 0.13 μm CMOS, it showed a low noise figure (2.8-3.4 dB) and high-power gain (19.2 dB) across 0.04-4.6 GHz. Input impedance matching was superior (-10.5 dB). Remarkably, it consumed only 8.5 mW from a 1.2 V supply, making it highly suitable for power-efficient applications.

In [108], Abdelhamid Helali et al., proposed a HEMT Gallium Nitride (GaN) based LNA tailored for wireless and Internet of Things (IoT) applications. This amplifier, designed for operation in the X-band frequency range (8–12 GHz), showcased impressive performance metrics. The LNA demonstrated a substantial gain of 38 dB, indicating its ability to amplify signals effectively within the specified frequency range. Additionally, the noise factor remained below 2.4 dB, ensuring minimal degradation of signal quality due to internal noise. Moreover, the LNA exhibited excellent input and output reflection coefficients (S_{11} and S_{22}) measured at -14 dB and -8 dB respectively. Their findings indicated that the proposed LNA outperformed other LNAs in terms of simulated performance metrics.

2.3 Summary

This chapter delves into the evolution and optimization of various on-chip passive components. Through literature it is identified that the significant silicon footprint occupied by the essential passive components such as inductors and capacitors, with a noticeable trade-off between inductance and quality factor. Notably, there's a lack of focus on analyzing inductors concerning design and process-controlled parameter variations. This thesis embarks on designing on-chip spiral inductors with the aim of achieving not just high inductance and quality factor but also improved self-resonant frequency for the efficient operation of RF devices in millimeter-wave circuits. Moreover, it's observed that as on-chip area diminishes, the operating frequency of components tends to rise. Therefore, there's a persistent need to minimize the on-chip footprint of components in the design phase. To address this challenge, the dissertation proposes multi-layer spiral inductors with minimized footprints to improve figure-of-merit properties. Through comprehensive analysis, the performance of RF circuits is evaluated by integrating the proposed inductor alongside existing ones.

Chapter 3

On-chip Spiral Inductors

3.1 Introduction

The on-chip inductors play an important role in the design of RF circuits such as VCOs, LNAs, Bandpass filters, and other tuning circuits. The half-turn split inductor is a crucial on-chip component in RFICs, playing a pivotal role in various RF applications. Its significance stems from its ability to provide compact, efficient, and high-performance solutions for RF circuits while overcoming the limitations of traditional inductors. The half-turn split inductor offers a compact footprint, which is essential for modern RFIC designs characterized by stringent space constraints. By utilizing only half of a turn in its design, it achieves a significant reduction in size compared to conventional inductors, making it particularly well-suited for integration within the limited area of modern semiconductor chips. The multilayer design enables a higher number of turns in a confined space, resulting in increased inductance without sacrificing efficiency. Moreover, the stacked configuration allows for precise control over the inductance value, enabling customization to meet specific circuit requirements. Furthermore, the compactness enables the integration of complex RF systems onto a single chip, facilitating the development of miniaturized and highly integrated RF devices such as wireless communication systems, radar systems, and IoT devices. This chapter deals with the implementation of half-turn and multipath inductors using variable splitting and stacking techniques to enhance the performance of the inductor. The design and simulation of the half-turn split inductor, coupled pyramid inductors and multilayer stack inductors are discussed in section 3.2, section 3.3 and section 3.4 respectively.

3.2 Planar and Half-turn Split Inductor

The journey of RF on-chip inductors commenced with the development of a single-layer structure known as the planar inductor, which seamlessly integrates into RFIC interconnects. This planar inductor configuration can consist of one or multiple conductors turns, tailored to meet specific performance demands. The popularity of the planar spiral inductor stems from its compact size, robust mutual inductance, impressive Q-factor, and straightforward design process. In on-chip implementations on silicon substrates, these inductors typically utilize a minimum of two metal layers. The top layer hosts the inductor structure, while the bottom layer facilitates port connections through underpass contacts. A constant-width spiral inductor emerges as a preferred choice, prized for its simplicity and compatibility with standard layout tools, offering ease of generation. This design not only ensures efficient utilization of on-chip real estate but also delivers optimal performance characteristics essential for RF applications. The proposed planar inductor is shown in Fig. 3.1.

The geometry parameters of the inductor structure, including metal width (w), metal spacing (s), outer diameter (d_{out}), and the number of metal turns (N), play pivotal roles in shaping its performance characteristics. In this configuration, conductors carrying current in the same direction are positioned closely together, while those carrying current in opposite directions are spaced further apart. This strategic arrangement serves to amplify the net positive mutual inductance and consequently enhances the overall inductance value. Among these parameters, the Q-factor emerges as the most critical design consideration for a spiral inductor. Q-factor, influenced by both frequency and geometry, directly impacts the inductor's efficiency and effectiveness. However, modeling a spiral inductor poses a significant challenge due to the complex electromagnetic coupling between metal lines. Achieving an accurate representation necessitates careful consideration of these factors, underscoring the intricate nature of spiral inductor design.

The main drawback of planar inductor is poor Q factor because of parasitic capacitance and skin effect. The proposed half-turn split inductor is implemented with same area to obtain high Q factor and inductance as shown in Fig. 3.2 (a) and 3.2 (b). Moreover, the half-turn split inductor exhibits excellent performance characteristics, particularly in terms of Q-factor and f_{SRF}. The unique geometry of the half-turn split inductor minimizes parasitic capacitance and resistance, leading to enhanced Q-factor compared to traditional inductors. This high Q-factor is crucial for maintaining signal integrity, improving the efficiency of RF circuits, and enabling long-range communication with minimal signal loss. Additionally, the self-resonant frequency

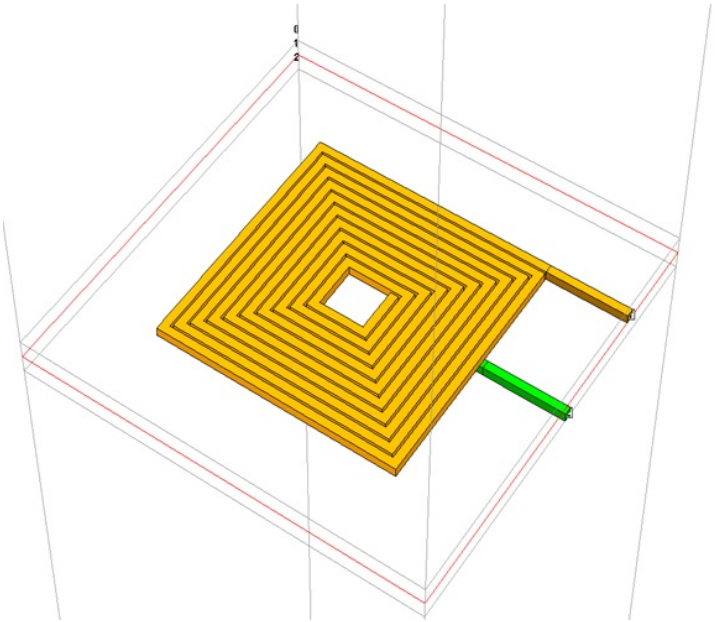


Figure 3.1: Planar Inductor (3-D view)

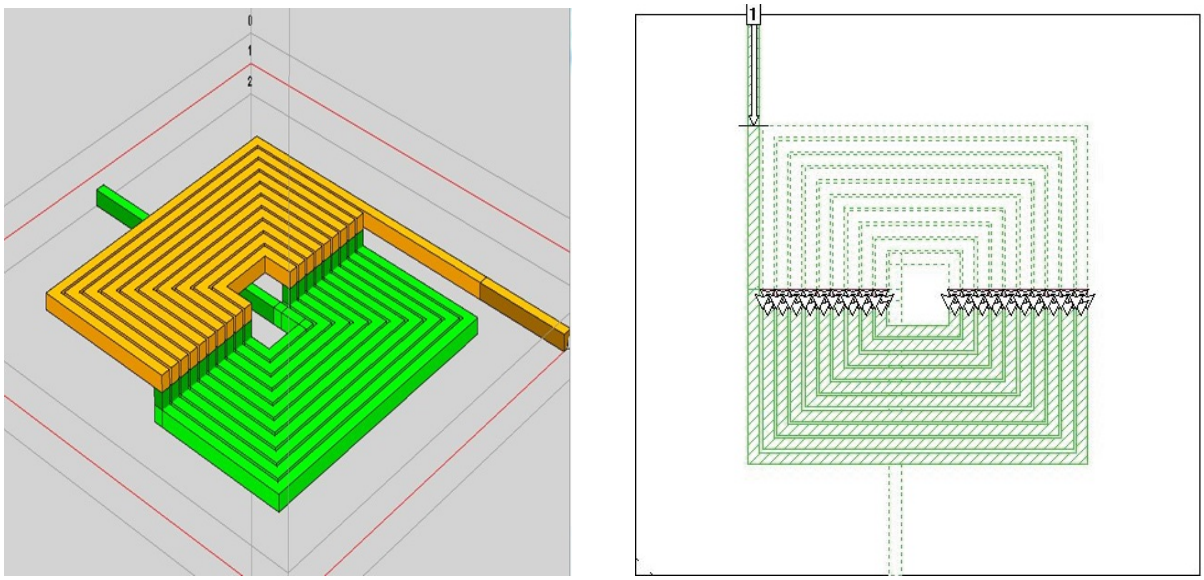
of the half-turn split inductor is typically higher than that of conventional inductors, allowing for operation at higher frequencies without sacrificing performance. The inductor is designed such a way that each turn is split in two half and placed in to two different layers. By placing each turn of the conductor in two different layers the parasitic capacitance is reduces drastically and increases the Q factor. The value of inductance also improved compared to the planar inductor.

Furthermore, the half-turn split inductor offers improved manufacturability and reliability compared to conventional inductors. Its symmetrical structure simplifies the fabrication process, reducing manufacturing costs and increasing production yield. Additionally, the absence of metal bridges in the core of the inductor enhances its reliability by minimizing the risk of electromigration and metal fatigue, thereby ensuring long-term stability and durability of RFICs in demanding operational environments. To design the single layer spiral inductor the following equations (Eq. 3.1 - 3.3) are utilized [109].

$$R_s = \frac{\rho l}{w\delta\left(1 - e^{\frac{t}{\delta}}\right)}, c_s = \frac{nw^2\varepsilon_{ox}}{t_{ox}} \tag{3.1}$$

$$c_{subs} = c_{ox}\frac{\left[1 + w^2\left(c_{ox} + c_{si}\right)c_{si}R_{si}^2\right]}{1 + w^2\left(c_{ox} + c_{si}\right)^2 R_{si}^2} \tag{3.2}$$

$$R_{subs} = \frac{1}{\left(w^2 c_{ox}^2 R_{si}\right)} + \frac{\left[R_{si}\left(c_{ox} + c_{si}\right)^2\right]}{c_{ox}^2} \tag{3.3}$$



(a) (b)

Figure 3.2: Half turn split inductor (a) 3-D view (b) 2-D view.

where, l is total spiral length, n is number of turns, W is metal width, t is metal thickness, tox is oxide thickness, ρ is resistivity and δ is skin depth. The design and simulation of on-chip planar and half-turn split inductors are shown in Table 3.1. The following equations are

Table 3.1: Design specifications for the half-turn split inductor

Parameter	**Specification**
Number of turns	10
Material	copper
width of the metal turn (μm)	2
Thickness (μm)	2
Substrate	Silicon (Si)
Oxide	Silicon Dioxide(SiO_2)
Spacing between turns (μm)	0.5
On-Chip area	60 μm $\times$ 60 μm

used to calculate the important metrics of the planar and proposed half-turn split inductor. The inductance represents capability of magnetic energy stored in the device. Many algorithms are used to calculate the inductance but greenhouse method gives the best approximation. The greenhouse algorithm calculates total inductance by computing the sum of self-inductances (L_{self}) of individual segments and mutual inductance between two segments is given in Eq. 3.4 [110].

$$L_{self} = \frac{\Psi}{I} \tag{3.4}$$

Where Ψ is the magnetic flux, and I is the Current flowing along the conductor. The total inductance expression is given in Eq. 3.5 as,

$$L_T = L_s + M^+ - M^- \tag{3.5}$$

Where L_T = Total Inductance L_s= Series Inductance of all segments (M^+ positive and M^- negative mutual inductances). The Q-factor is the important figure of merit of the inductor and calculated as shown in Eq. 3.6,

$$Q = 2\pi \frac{peak\ magnetic\ energy - peak\ electric\ energy}{Energy\ loss\ in\ one\ cycle} \tag{3.6}$$

3.2.1 Results and Discussions

The design of the half-turn split inductor has been successfully implemented and evaluated using SONNET (EM) simulation software. The simulation results, depicted in Fig. 3.3, reveal a remarkable 31.6% improvement in the Q factor compared to the traditional planar inductor configuration. This enhancement is attributed to a strategic placement of each turn across two different layers, effectively mitigating inter-wire capacitance and reducing series resistance. Additionally, as illustrated in Fig. 3.4, the inductance values of both planar and split inductors remain comparable from 1.0 GHz to 10.0 GHz.

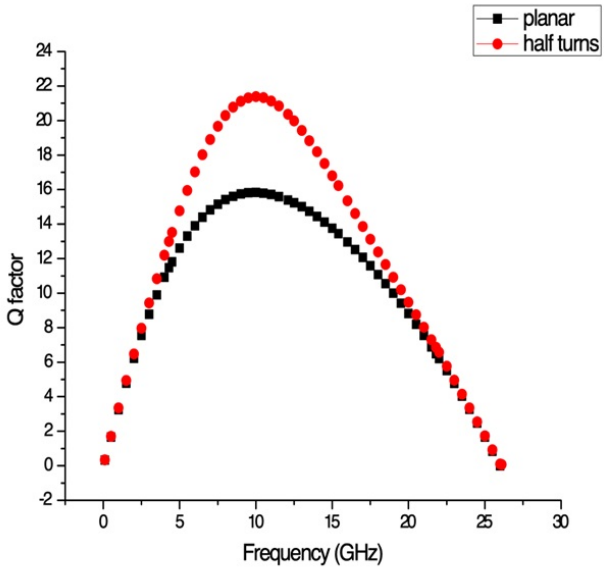


Figure 3.3: Quality factor

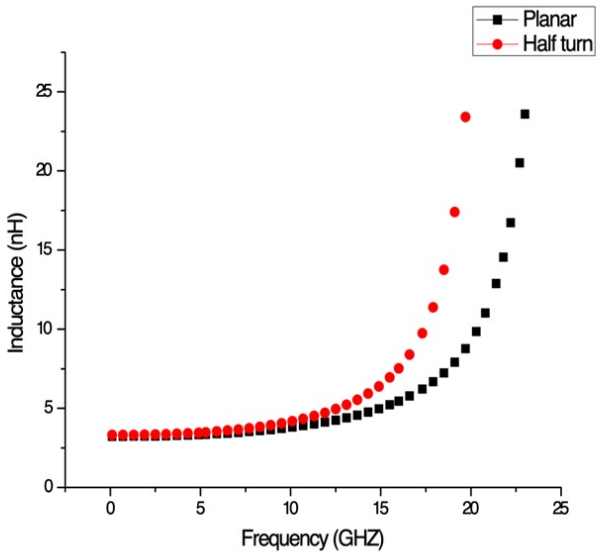


Figure 3.4: Inductance

Table 3.2: Comparison of Planar and Proposed Inductor

S.No	Name of the Inductor	L (nH)		Q	
		Practical	**Theoretical**	**Practical**	**Theoretical**
1	Planar Inductor	5.7	5.9	15.8	16.2
2	Half-turn Split Inductor (Proposed)	6.56	6.7	20.8	21

However, beyond 10.0 GHz (i.e at 14 GHz), a notable 15% improvement is observed in the proposed split inductor design compared to the standard planar counterpart. The comparison of inductance and Q-factor is depicted in Table 3.2. This observation underscores the efficacy of the split inductor structure in achieving superior performance characteristics, particularly at higher frequencies where traditional planar configurations may exhibit limitations. Overall, the utilization of the half-turn split inductor represents a promising advancement in RF circuit design, offering enhanced Q factor and frequency-dependent performance improvements.

3.3 Proposed pyramid and coupled pyramid inductor structure

In the design of on-chip inductors, the calculation of inductance holds paramount importance, particularly in efforts to enhance both inductance and Q factor. The total inductance of an inductor can be computed as the sum of series inductances of individual conductors and mutual

inductance. When currents flow in the same direction within two metal tracks, positive coupling occurs, leading to an increase in inductance. Conversely, when currents flow in opposite directions and are placed close to each other, the overall inductance decreases. The interplay between self and mutual inductance significantly influences the overall DC inductance of the inductor, as discussed in literature [111]. To address these considerations, a pyramid inductor design is introduced, featuring varying inner diameters from top to bottom layers. With each successive layer, the inner diameter decreases by 2 μm. To further optimize inductance, two turns are

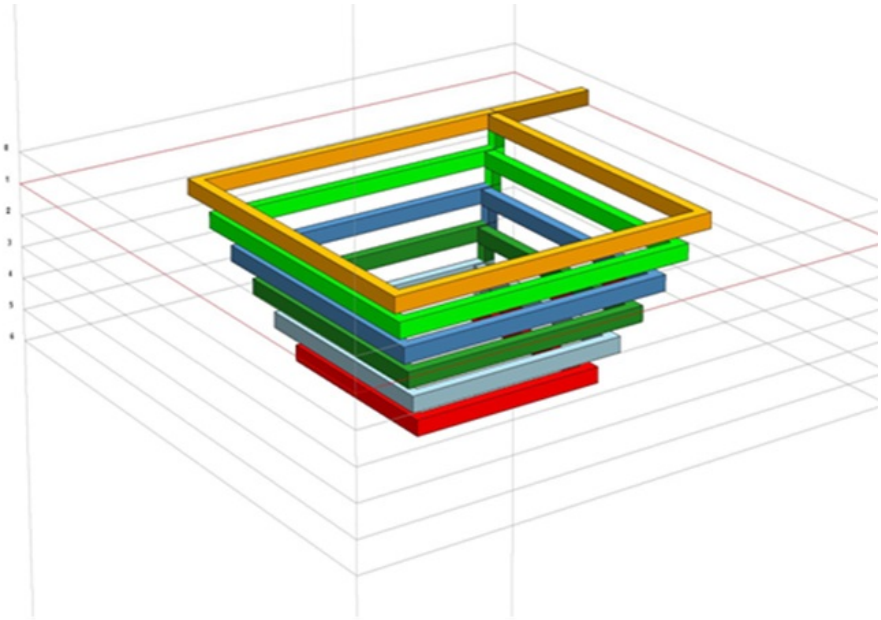


Figure 3.5: Pyramid inductor

incorporated at each layer, with variable width and dimensions employed in every layer to improve the Q factor of the proposed inductor, as depicted in Fig. 3.5. The pyramid inductor is crafted with a conductor width of 2 μm, a spacing of 0.5 μm between conductors, and a conductor thickness of 2 μm. Notably, the outer diameter of the inductor diminishes as it descends to lower metal layers. This deliberate reduction serves to mitigate field coupling between adjacent layers and enhance substrate losses attributable to field coupling and displacement current.

The design of the coupled pyramidal inductor closely resembles that of the pyramid inductor, as depicted in Fig. 3.6. However, in this variation, the outer diameter undergoes a strategic alteration: it decreases until the bottom three layers and then symmetrically increases for the subsequent three layers. This stacked structure serves to further diminish substrate loss and field coupling, thereby amplifying both inductance and Q factor. The conductor width remains consistent at 2 μm, with a 0.5 μm gap between conductors and a thickness of 2 μm. The symmetrical stacking of metal strips contributes to a reduction in eddy current loss and crowding effect by minimizing the ingress of magnetic fields into the substrate. This meticulous design

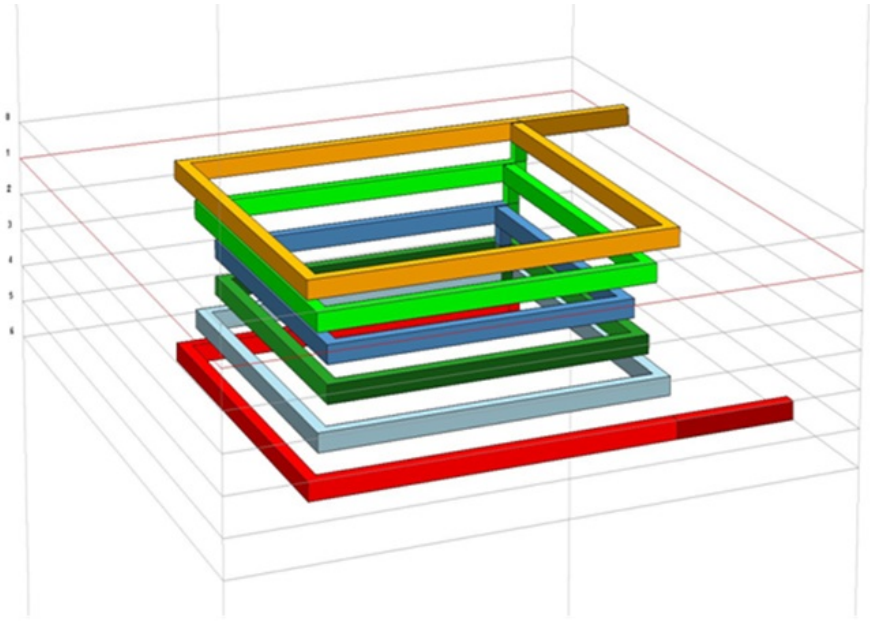


Figure 3.6: Coupled pyramid inductor

approach underscores a commitment to optimizing inductance and Q factor while concurrently mitigating potential sources of loss and interference.

3.3.1 Results and Discussions

The pyramid and coupled pyramid inductors are specifically designed for Silicon substrates with a thickness of 100 μm. Through meticulous calculation, the inductance, Q factor, and resistance of these inductors are determined from the Y parameters, which are derived from the S parameters as illustrated in Fig. 3.7 and Fig. 3.8. Simulation results notably showcase a significant enhancement in the inductance value of the coupled pyramid inductor compared to its pyramid counterpart. While the improvement in Q factor is marginal, the improved inductance value proves advantageous for designing inductors operating at lower frequencies. This finding underscores the utility of the coupled pyramid inductor in compact designs aimed at achieving higher inductance values. The simulation values attained for both the pyramid and coupled pyramid inductors are meticulously tabulated in Table 3.3, providing a comprehensive comparison of their respective performances. This insight not only highlights the potential of the coupled pyramid inductor in enhancing inductance but also underscores its relevance in optimizing the performance of on-chip inductors for diverse frequency applications.

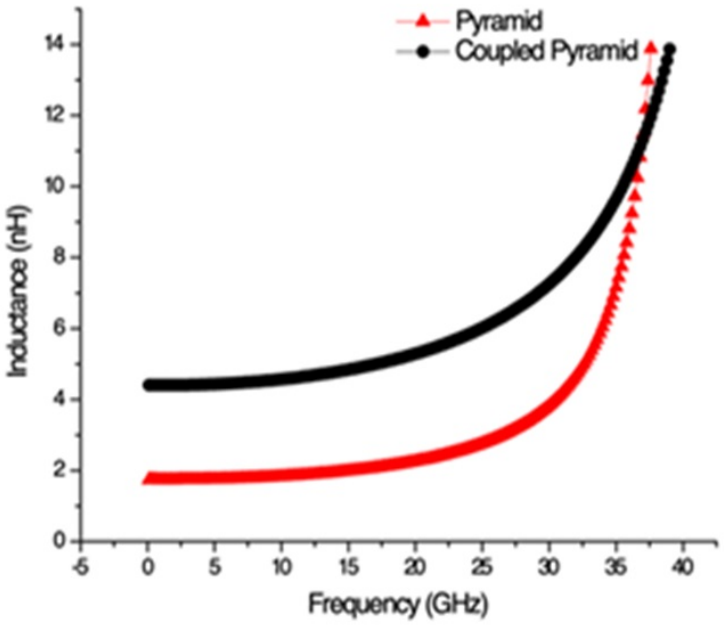


Figure 3.7: Comparison of Inductance

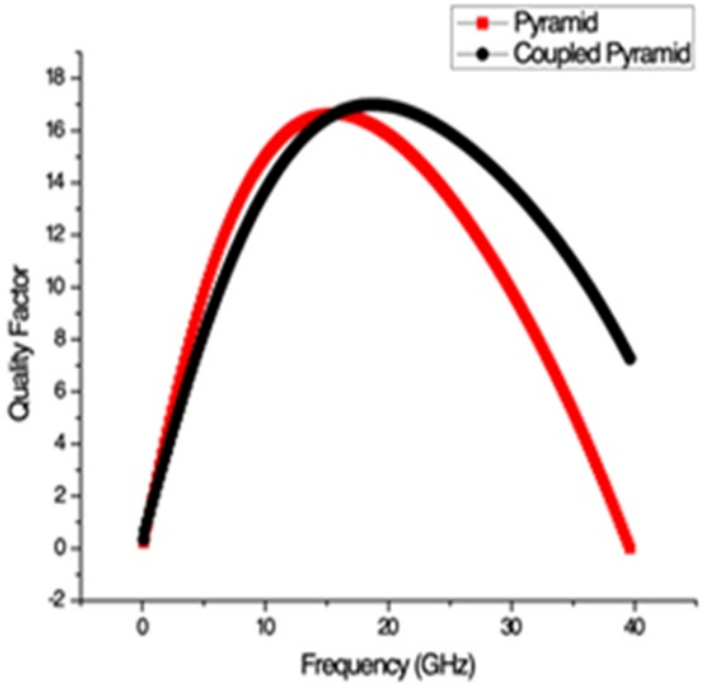


Figure 3.8: Comparison of Q factor

Table 3.3: comparison of planar and Multilayer inductor

S.No	Name of the Inductor	L (nH)		Q	
		Practical	**Theoretical**	**Practical**	**Theoretical**
1	Pyramid Inductor	1.92	2.1	16.8	17.1
2	Coupled Pyramid	4.85	4.9	17.15	18.2

3.4 Proposed Multilayer Inductor

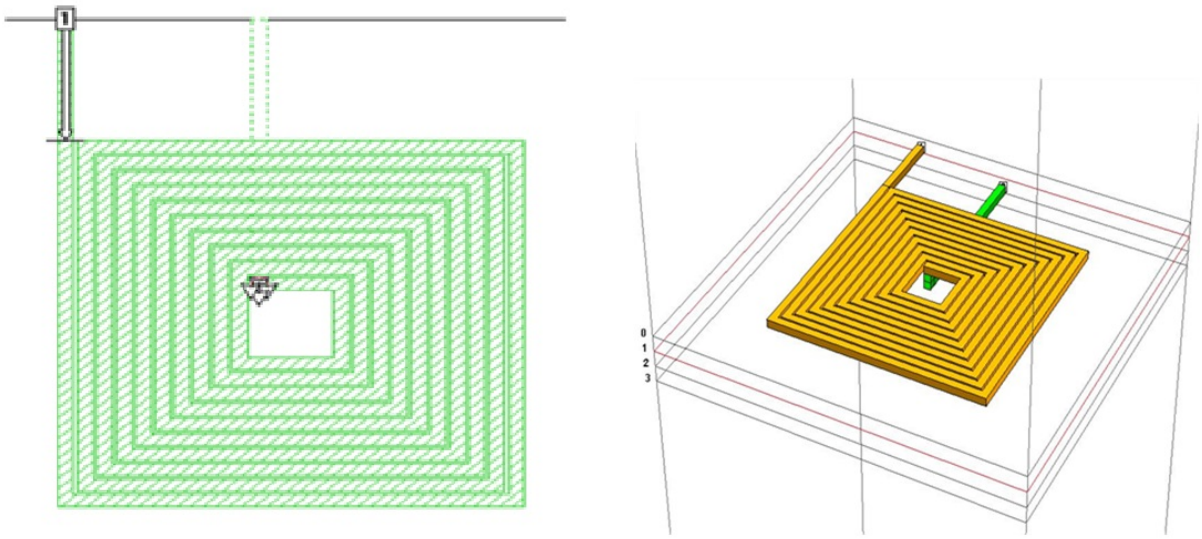
Initially, a single layer planar inductor is designed, as depicted in Fig. 3.9. However, single layer configuration suffers from a poor Q factor due to the equi-potential nature of all metal tracks, leading to increased capacitance effects. Additionally, the limited number of turns restricts the inductance. To address these shortcomings and enhance the performance of the inductor in terms of inductance (L), Q factor, and SRF, various alternative configurations such as hexagonal, octagonal, and circular shapes are proposed [112]. Among these, the hexagon inductor demonstrates superior electrical performance compared to the planar inductor but requires a larger area footprint.

In pursuit of further improvements in inductance and quality factor, a multilayer inductor design is introduced, as illustrated in Fig. 3.10. This multilayer inductor is designed across four layers, leveraging layers stacking to mitigate parasitic capacitance and enhance inductance. The width and spacing of the metal strips in each layer are meticulously chosen to minimize resistive losses, eddy losses, and crowding effects. Through careful stacking of the metal strips, the entry of magnetic field loops into the substrate is reduced, resulting in improved performance with respect to eddy current and crowding current. Moreover, by adjusting the width and thickness of the metal strips, the impact of skin depth is mitigated. Fig. 3.10 (a) provides a top view, depicting the orientation of the strips and the spacing between metallic strips. In Fig. 3.10 (b), a perspective view is presented, showcasing how the dimensions of the metal strips decrease as they transition to lower metallic layers. This comprehensive approach to design optimization underscores the commitment to achieving superior performance characteristics while simultaneously addressing various technical challenges associated with inductor design.

The parameters used for evaluating the inductor's performance are Q factor, resistances, capacitances, SRF, and area. The above parameters are combined into a single parameter called FoM of the inductor and is given in Eq.3.7.

$$FoM = \frac{LQ_{max}f_{SRF}}{\sqrt{a}} \tag{3.7}$$

Where L is the inductance, Qmax is the maximum value of the Q factor, f_{SRF} is the self resonant frequency and A is the area. The Q factor describes the amount of magnetic energy stored in



(a) (b)

Figure 3.9: Planar Inductor (a) Top view (b) Prospective view.

the inductor [113] given by Eq. 3.8

$$Q = \frac{\omega L_T}{R_s} \frac{R_p}{\left[\left(\frac{\omega L_T}{R_s}\right) 2 + 1\right] R_s} \left[1 - \frac{R_s^2 \left(c_s + c_p\right)}{L_T} - \omega^2 L_T \left(c_s + c_p\right)\right] \tag{3.8}$$

Where ω is the angular frequency, R_p is the substrate parasitic resistance, R_s is the series resistance, C_P is the substrate parasitic capacitance, C_s is the interlayer capacitance and L_T is the total inductance

$$R_p = \frac{1}{\omega^2 C_{ox} R_s} + \frac{R_{si} \left(C_{ox} + C_{si}\right)^2}{C_{ox}} \tag{3.9}$$

Where C_{ox} is the oxide parasitic capacitance and C_{si} is the substrate capacitance

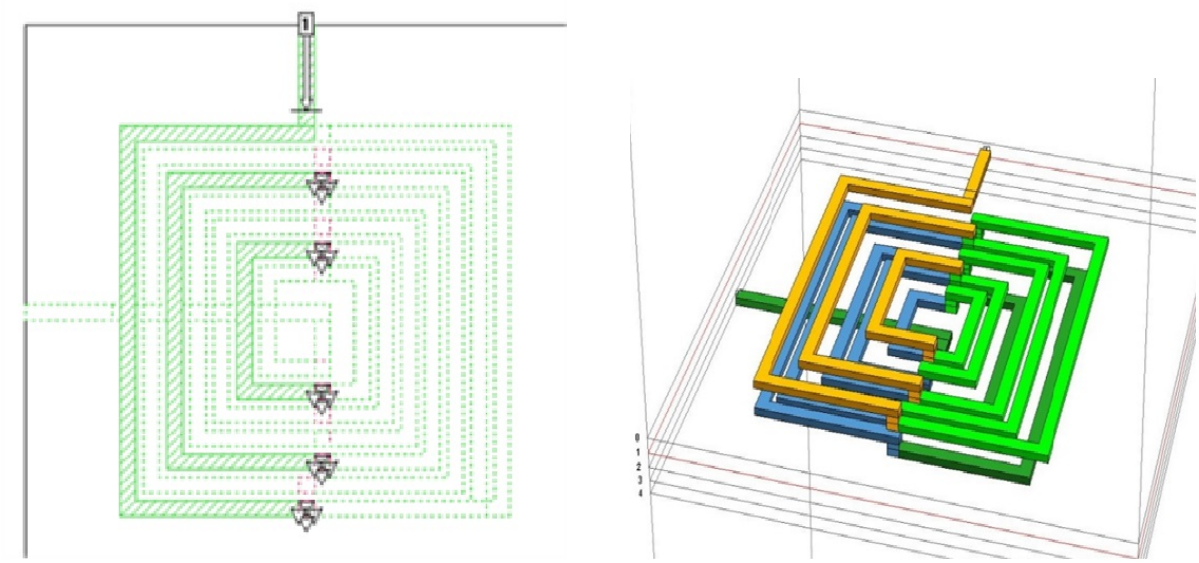
$$C_p = C_{ox} \frac{1 + \omega^2 \left(C_{ox} + C_{si}\right) C_{si} R_{si}^2}{1 + \omega^2 \left(C_{ox} + C_{si}\right)^2 R_{si}^2} \tag{3.10}$$

$$f_{SRF} = \frac{1}{2\pi \sqrt{L_T C_{eq}}} \tag{3.11}$$

Where C_{eq} is the equivalent parasitic capacitance.

3.4.1 Simulation Results and Discussions

The proposed multi-path and multi-layer inductor design, implemented within a compact area of 60 μm X 60 μm across four layers, represents a significant advancement in RF circuitry.



(a) (b)

Figure 3.10: Multilayer Inductor (a) Top view (b) Prospective view.

Utilizing SONNET (EM) simulation software, the inductor's performance is thoroughly evaluated based on specific design parameters: outer diameter (OD) of 50 μm, spacing of 2 μm, and conductor thickness of 4 μm. The substrate's dielectric constant is 12.9, with a thickness of 100 μm, while each layer boasts a thickness of 4 μm. Through simulation, the inductance, Q factor, and series resistance values are extracted from the S-parameters, which are then converted to Y parameters using Eqs. 3.12 - 3.14.

$$L = \frac{1}{2\pi f} Im\left[\frac{1}{Y_{11}}\right] \tag{3.12}$$

$$Q = \frac{-Im\left[\frac{1}{Y_{11}}\right]}{Re\left[Y_{11}\right]} \tag{3.13}$$

$$R_s = \frac{1}{Re\left[Y_{12}\right]} \tag{3.14}$$

The comparison between the multi-layer inductor and the standard planar inductor is depicted

Table 3.4: comparison of planar and Multilayer inductor

S.No	**Name of the Inductor**	**L (nH)**		**Q**	
		Practical	**Theoretical**	**Practical**	**Theoretical**
1	Planar Inductor	3.12	3.25	15.8	16.2
2	Multilayer (Proposed)	3.25	3.3	18.51	18.7

in Figures 3.11, 3.12, and 3.13, showcasing the respective performances in terms of inductance, Q factor, and series resistance. The simulation results highlight a marginal improvement in

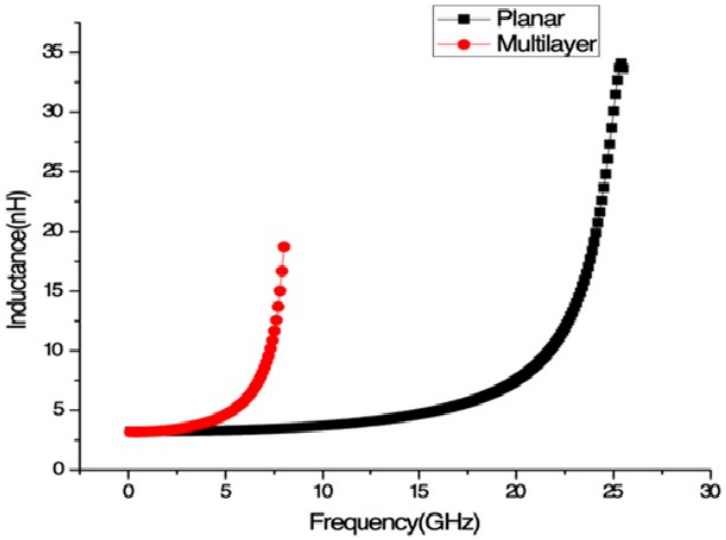


Figure 3.11: Simulation result of inductance for the planar and multilayer inductor

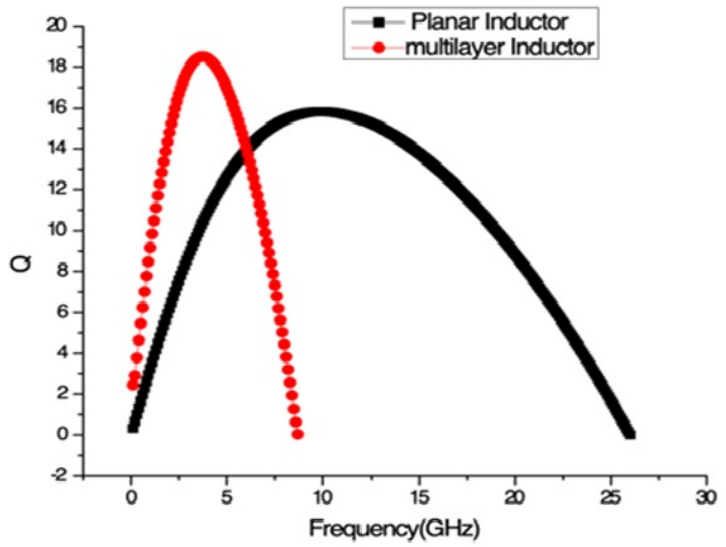


Figure 3.12: Simulation result of Q factor for the planar and multilayer inductor

inductance for the planar inductor, attributed to the absence of mutual positive coupling between layers. In contrast, the proposed multi-layer inductor exhibits a notable 17% enhancement in Q factor compared to its planar counterpart. This improvement is primarily attributed to the reduction in parasitic capacitance and current crowding effects enabled by the multi-layer configuration.

Numerical values achieved for both the planar and multi-layer inductors are tabulated in Table 3.4, providing a comprehensive comparison of their respective performances. Overall, the simulation outcomes underscore the significant benefits offered by the multi-layer inductor design, demonstrating its potential to elevate the performance and efficiency of RF circuits.

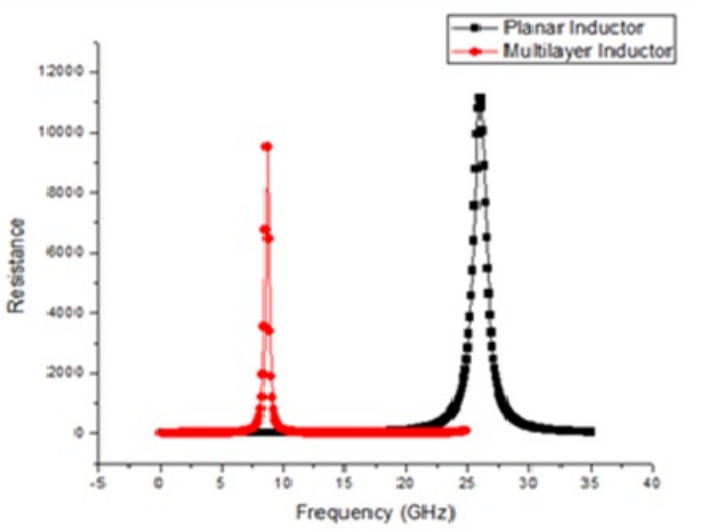


Figure 3.13: Simulation result of series resistance for the planar and multilayer inductor

3.5 Summary

This chapter provides a comprehensive analysis of the design and implementation processes for four distinct types of on-chip inductors: the standard planar inductor, the half-turn split spiral inductor, the coupled pyramid inductor, and the multilayer inductor. Through meticulous optimization of both device layout parameters and process control parameters, an optimal combination was established to facilitate the design and simulation of various on-chip passive components utilizing spiral structures. Notably, the proposed half-turn split inductor demonstrates a significant 31.6% improvement in Q factor at frequencies above 10 GHz. To further enhance inductance and Q factor, the pyramid and coupled pyramid inductors were introduced, showing a 35% improvement in Q factor compared to the standard pyramid inductor. However, at a frequency of 5 GHz, these inductors exhibited a relatively low Q factor. Consequently, a multilayer inductor was proposed, achieving a 17% enhancement in Q factor over the coupled pyramid inductor. These improvements are attributed to the reduction in interwiring capacitance and series resistance. The multilayer inductor demonstrated the best overall performance in terms of both inductance and Q factor. Simulation results indicate that the proposed inductors are particularly advantageous for high-frequency RF applications, ranging from 1 GHz to 10 GHz. This collective insight underscores the efficacy of the proposed designs in enhancing the performance and applicability of on-chip inductors, especially in demanding high-frequency RF environments.

Chapter 4

Mathematical Verification

4.1 Introduction

Inductance extraction is a pivotal stage in verifying various on-chip passive inductor designs. Over time, researchers have derived several analytical expressions to calculate inductance for on-chip spiral inductors with different geometries. Methods such as Greenhouse formulations, modified Wheeler formula, Current sheet approximation, Integral field solution, partial equivalent electrical circuit (PEEC) [114], and data fitting algorithms have been developed for this purpose. Grover's basic analytical expression offers a foundational framework for extracting inductance from metal lines and parallel conductors [115]. While the conventional Greenhouse model provides accurate results, it involves large summation steps dependent on the number of interacting parallel conductor segments, making it computationally intensive. However, these analytical expressions are generally frequency-independent and yield satisfactory results for frequencies up to 2 GHz. Beyond this range, discrepancies between theoretical and experimental values arise due to variations in on-chip spiral losses at higher frequencies, especially relevant in modern high frequency and millimeter-wave circuits utilized in wireless and mobile communications, operating from 3 to 300 GHz. Therefore, there is a pressing need for frequency-dependent accurate expressions to extract inductance values at 5G frequency bands. The Greenhouse method computes inductance as the sum of self-inductance and mutual inductances of conductor segments, which are influenced by conductor spacing and segment dimensions. Mutual inductance, whether positive or negative, depends on the direction of current flow in conductor turns, affecting overall inductance and consequently, the Q of the inductor.

Grover's work contributes numerical expressions for self and mutual inductance across various conductor structures, enhancing understanding and facilitating precise inductance calculations.

4.2 Inductance Calculation

Initially, Grover laid the groundwork by providing expressions for self and mutual inductance across various configurations of thin films and conductors. Building upon Grover's foundational work, Greenhouse further refined inductance extraction techniques, particularly for rectangular cross-sections. Greenhouse's approach encompasses considerations of self-inductance, positive mutual inductance, and negative mutual inductance. Consider a 3-turn spiral inductor with a rectangular cross-section, comprising 12 conductor segments as depicted in Fig. 4.1 [116]. The self-inductance expression is given in Eq. 4.1,

$$L_i = 0.2l_i\left[ln\left(\frac{2l_i}{w+t}\right) + 0.5 + \left(\frac{w+t}{3l_i}\right)\right]\mu H \tag{4.1}$$

Where 'l_i' represents the length of the i^{th} segment of the conductor, while 'w' and 't' denote the width and thickness of the conductor respectively, measured in meters. Additionally, μ stands for metal permeability. The self-inductance of the spiral can be expressed as shown in Eq. 4.2

$$L_0 = \sum_{i=1}^{12} L_i \tag{4.2}$$

The total self-inductance of a spiral can be expressed as the sum of positive and negative mutual inductance. Positive mutual inductance occurs when the currents through the conductors are in the same direction, while negative mutual inductance occurs when the currents through the conductors are in opposite directions. The mutual inductance between two segments is symmetrical, denoted in Eq. 4.3

$$M_{i,j} = M_{j,i} \tag{4.3}$$

For a 3-turn spiral, its positive and negative mutual inductance can be represented as (Eq. 4.4):

$$M_+ = 2\left(M_{1,5} + M_{1,9} + M_{2,6} + M_{2,10} + M_{3,7} + M_{3,11} + M_{4,8} + M_{4,12} + M_{5,9} + M_{6,10} + M_{7,11} + M_{8,12}\right) \tag{4.4}$$

$$\begin{aligned} M_- = 2\Big(&M_{1,3} + M_{1,7} + M_{1,11} + M_{5,3} + M_{5,7} + M_{5,11} + M_{9,3} + M_{9,7} + M_{9,11} \\ &+ M_{2,4} + M_{2,8} + M_{2,12} + M_{6,4} + M_{6,8} + M_{6,12} + M_{10,4} + M_{10,8} + M_{10,12}\Big) \end{aligned} \tag{4.5}$$

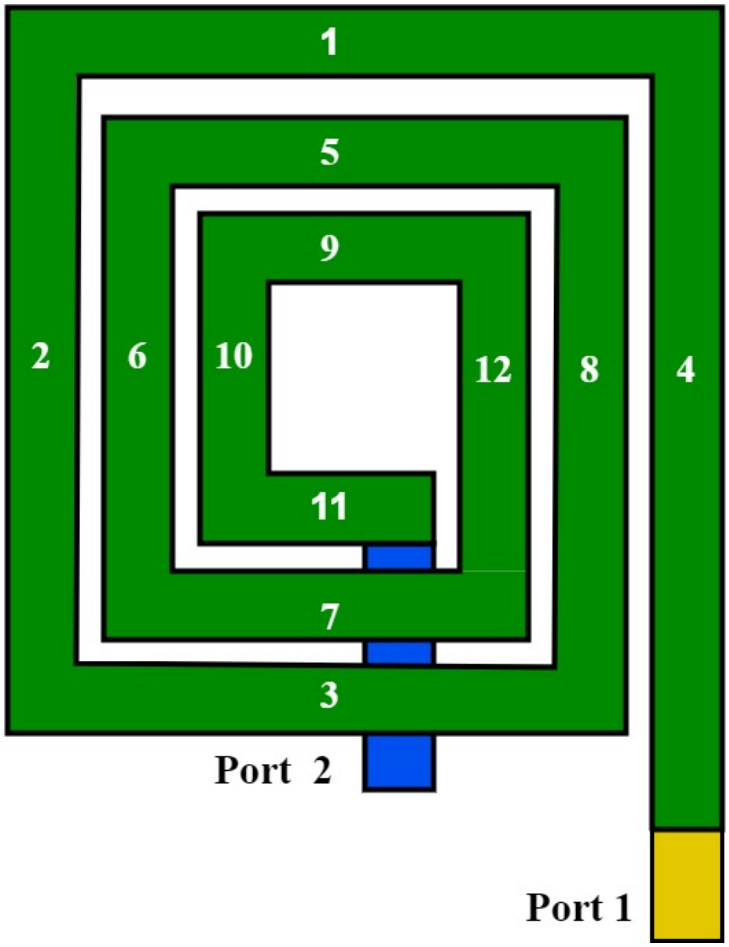


Figure 4.1: Square spiral with 3 turns (12 segments)

The total inductance of the spiral is expressed as below Eq. 4.6 and Eq. 4.7.

$$L_T = L_0 + M_+ - M_- \tag{4.6}$$

$$\begin{aligned} L_T = \sum_{i=0}^{12} L_i + 2\Big(&M_{1,5} + M_{1,9} + M_{2,6} + M_{2,10} + M_{3,7} + M_{3,11} + M_{4,8} + M_{4,12} \\ &+ M_{5,9} + M_{6,10} + M_{7,11} + M_{8,12}\Big) - 2\Big(M_{1,3} + M_{1,7} + M_{1,11} + M_{5,3} + M_{5,7} \\ &+ M_{5,11} + M_{9,3} + M_{9,7} + M_{9,11} + M_{2,4} + M_{2,8} + M_{2,12} + M_{6,4} + M_{6,8} + M_{6,12} \\ &+ M_{10,4} + M_{10,8} + M_{10,12}\Big) \end{aligned} \tag{4.7}$$

The shunt and substrate capacitances of the planar inductor in the hybrid lumped model can be represented as given in Eq. 4.8 and Eq. 4.9, respectively.

$$C_{shunt} = \frac{wlc_0}{2} \tag{4.8}$$

$$C_{subs} = C_{ox}\frac{\left[1 + w^2\left(C_{ox} + C_{si}\right)C_{si}R_{si}^2\right]}{1 + w^2\left(C_{ox} + C_{si}\right)^2 R_{si}^2} \tag{4.9}$$

where, C_0 represents the substrate capacitance density, typically ranging from 0.01 to 0.001 fF/μm^2. l stands for the total length of the spiral, w represents the width of the metal, C_{ox} is the oxide capacitance. The main goal of the above spiral is to attain the target inductance value within the smallest footprint feasible, while simultaneously minimizing parasitic capacitance to ensure that the self-resonant frequency (f_{SRF}) remains beyond the desired frequency band.

4.3 Frequency Independent Analytical Method

The Greenhouse and Grover methods have yielded numerous frequency-independent analytical formulas for extracting inductance in planar and multilayer inductors.

4.3.1 Greenhouse method

In the analysis of planar rectangular spiral inductors, the presence of negative mutual inductance impacts both the calculation of mutual inductance and the overall inductance. Total inductance is influenced by three main factors: the self-inductance of each segment, the positive and negative mutual inductance between line segments. Specifically, for an inductor with n turns and J segments, the number of positive mutual inductance terms (M_+) can be expressed as 4[n(n-1) + 2n(J-4n)].

The self-inductance of a straight conductor can be expressed as given in Eq. 4.10.

$$L = 0.002l\left\{ln\left(\frac{2l}{GMD}\right) + \frac{AMD}{l} + \left(\frac{\mu}{4}\right)T - 1.25\right\} \tag{4.10}$$

The Geometric Mean Distance GMD = 0.22352(w+t) and Arithmetic Mean Distance AMD = w/3. Total inductance of inductor is $L_{Total} = L_{Self} + M_+ - M_-$. The Q value of inductor is

$$Q = ln\left[\frac{l}{GMD} + \frac{GMD}{l} + \left\{1 + \left(\frac{l}{GMD}\right)^2\right\}^{\frac{1}{2}} - \left[1 + \left(\frac{GMD}{l}\right)^2\right]^{\frac{1}{2}}\right] \tag{4.11}$$

4.3.2 Modified Wheeler Formula

The self-inductance can be estimated based on the number of turns, using a simplified version of the Wheeler formula as given in Eq. 4.12 [117].

$$L_{Mod.wh.} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{4.12}$$

Where μ_0 (permeability of vacuum), n (number of turns), d_{avg} (average diameter), ρ (filling ratio of the spiral), K_1 and K_2 coefficients for different layouts are shown in Table 4.1. When a

Table 4.1: Coefficients for MW expression

Layout	$\mathbf{K_1}$	$\mathbf{K_2}$
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

spiral inductor has more turns in a single layer, its inductance decreases because the innermost turns are closer to the center of the spiral, reducing positive mutual inductance and increasing negative mutual inductance. Increasing the central hollow space, on the other hand, increases total inductance, but it also enlarges the size of the inductor.

4.3.3 Current Sheet Approximation

To find the inductance of a planar inductor, we analyze it by treating its spiral segments as current sheets with equivalent current densities. Each pair of parallel sheets contributes to mutual inductance, which can be either positive or negative, while each sheet also has its own self-inductance. In the case of a square spiral inductor, there are four identical current sheets. The adjacent sheets are oriented orthogonally, while the opposite ones are parallel. We calculate both self and mutual inductances using three different methods: geometric mean distance (GMD), arithmetic mean distance (AMD), and arithmetic mean square distance (AMSD). The self-inductance is determined by Eq. 4.13.

$$L_{CSA} = \frac{\mu n^2 d_{avg} C_1}{2} \left(ln\left(\frac{C_2}{\rho}\right) + C_3 \rho + C_4 \rho^2 \right) \tag{4.13}$$

Where layout coefficients C_1, C_2, C_3, and C_4, are different for various layouts which are shown in Table 4.2, ρ represents the fill ratio, and n represents the number of conductors. It's noted that

the accuracy of a specific formula decreases notably when w/s ratio is high. This discrepancy becomes significant when the spacing s<3w resulting in a maximum error of 8%.

Table 4.2: Coefficients for CSA expression

Layout	$\mathbf{C}_1$	$\mathbf{C}_2$	$\mathbf{C}_3$	$\mathbf{C}_4$
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.0	0.17
Octagonal	1.07	2.92	0.0	0.19

4.3.4 Inductance Extraction using Meander Inductors

The inductance of multilayer inductors can be calculated using the principles of meander inductors, following the Greenhouse and Grover methods. By considering parameters like conductor length, width, and thickness, we can derive straight forward formulas for both self and mutual inductance. A simplified analytical expression is provided to calculate the self-inductance of each segment (or turn) of a conductor is given in Eq. 4.14.

$$L = 0.021\left[ln\left(\frac{2l}{w+t}\right) + \frac{w+t}{3l} + 0.50049\right] \tag{4.14}$$

where the layout parameters l, w and t are the w is the length, width and thickness respectively. The total self-inductance of an inductor is determined by considering the combined effects of each individual segment of the conductor. This includes factors such as the length of the conductor, the spacing between segments, and their respective positions. The calculation of mutual inductance using meander inductance extraction can be divided into five distinct cases, each of which is based on the analytical expression for the meander inductor mentioned earlier [118].

Case-1: (Parallel filaments of equal length) This assumes equal length for conductors, which are positioned at distance 'r' in parallel as shown in Fig. 4.2. Mutual inductance when length of conductors is same and are placed at distance 'r' opposite to each other can be expressed as shown in Eq. 4.15.

$$M_{c1}(l,r) = \frac{\mu_0 l}{2\pi}\left[ln\left(\frac{l}{r}\right) + \sqrt{1+\frac{l^2}{r}} - \sqrt{1+\frac{r^2}{l}} + \frac{r}{l}\right] \tag{4.15}$$

Case-2: (Parallel filaments of unequal length with spacing)

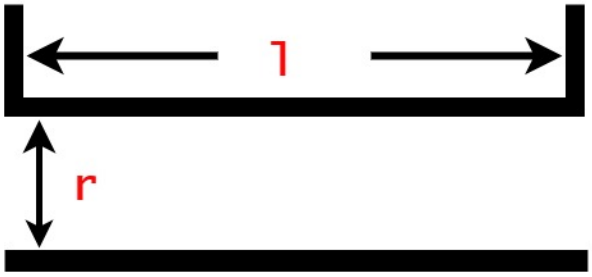


Figure 4.2: Parallel filaments of equal length

This setup involves conductors of varying lengths, with a distance of s between them and a separation of r between layers, as depicted in Fig. 4.3. The calculation of mutual inductance

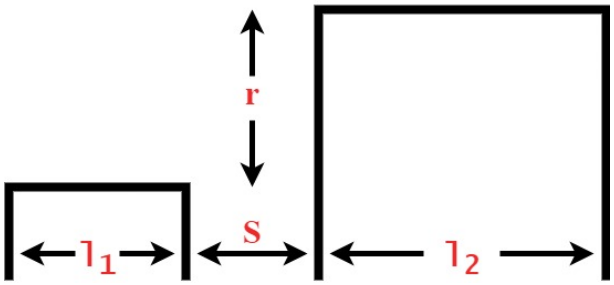


Figure 4.3: Parallel filaments of unequal length spaced apart by s

for parallel filaments is given by the Eq. 4.16.

$$M_{c2}(l_1, l_2, r, s) = 0.5\,\{M_c\,(l_1 + l_2 + s, r) + M_c\,(s, r) - M_c\,(l_1 + s, r) - M_c\,(l_2 + s, r)\} \tag{4.16}$$

Case-3: (Common end line perpendicular filaments)

This assumes that the conductors, which are separated and terminate in a common perpendicular configuration as depicted in Fig. 4.4, have unequal lengths. The formula for determin-

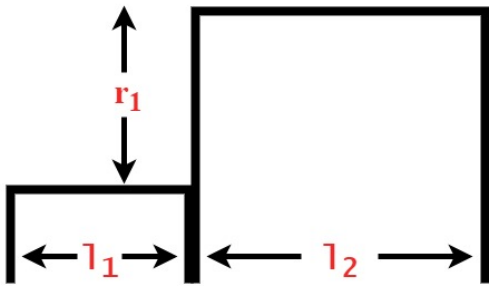


Figure 4.4: Conductor filaments of unequal length ending in common perpendicular

ing mutual inductance between two perpendicular filaments with common ends is expressed as

given in Eq. 4.17.

$$M_{c3}(l_1, l_2, r_1) = 0.5\{M_c(l_1, r_1) + M_c(l_2, r_1) - M_c(l_1 - l_2, r_1)\} \tag{4.17}$$

Case-4: (Parallel filaments of unequal length without spacing)

The length of parallel filament pairs without spacing, as illustrated in Fig. 4.5, varies. The

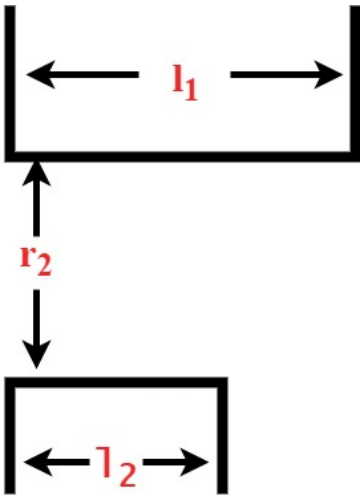


Figure 4.5: Conductor filaments of unequal length without spacing

formula for mutual inductance between closely placed conductor filaments without any spacing is as follows:

$$M_{c4}(l_1, l_2, r_2) = 0.5\{M_c(l_1 + l_2, r_2) + M_c(l_1, r_2) - M_c(l_2, r_2)\} \tag{4.18}$$

Case-5: (Parallel segments of equal length with spacing on same axis)

The conductors are positioned on the same axis with a separation distance of s, as depicted in Fig. 4.6. The mutual inductance between conductor filaments aligned on the same axis is

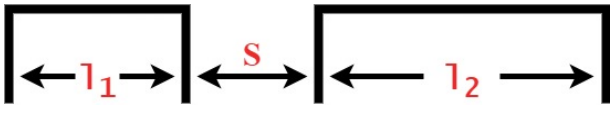


Figure 4.6: Parallel filaments of unequal length spaced apart by s

determined by:

$$M_{c5}(l_1, l_2, s) = \frac{\mu_0}{2\pi}\{(l_1 + l_2 + s)\,ln(l_1 + l_2 + s) - (l_1 + s)\,ln(l_1 + s) - (l_2 + s)\,ln(l_2 + s) + slns\} \tag{4.19}$$

Analytical expressions were employed to determine the inductance values of the proposed Planar, 3D, and multilayer inductors. These analytical results are then validated against simulation results obtained from SONNET software. The accuracy of the proposed inductors is assessed through a performance comparison illustrated in Figures 4.7, 4.8, and 4.9, respectively. It is observed that the inductance is deviating between the four extraction methods, as operating frequency increases. They are closely tallying below 6 GHz. The inductance error is negligable between analytical and SONNET results for the proposed inductors.

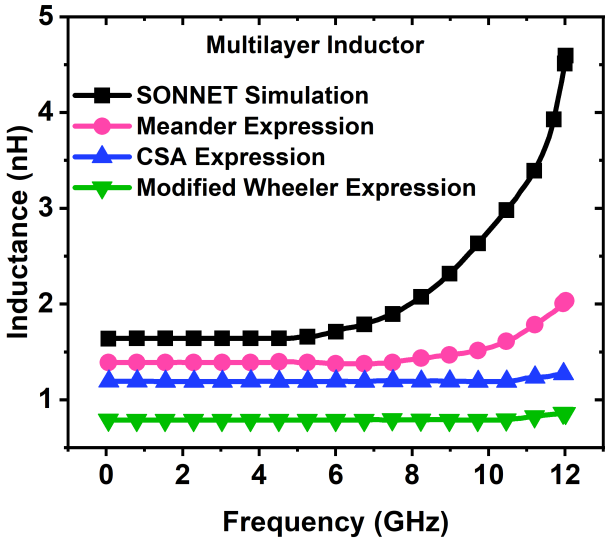


Figure 4.7: Inductance comparison of simulated and analytical expression results for a multilayer inductor

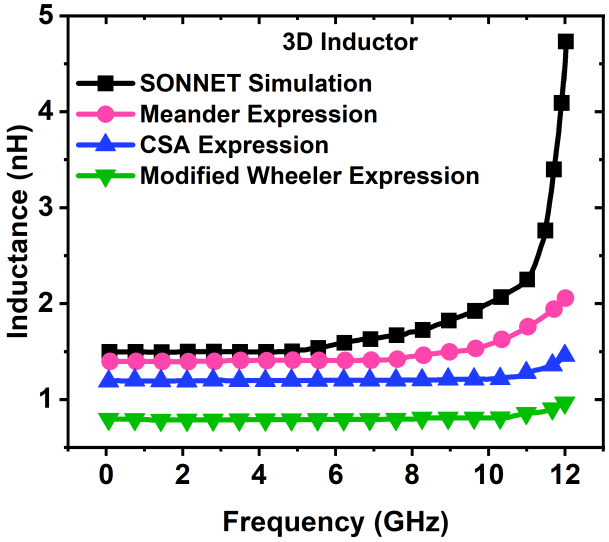


Figure 4.8: Inductance comparison of simulated and analytical expression results for a Pyramid inductor

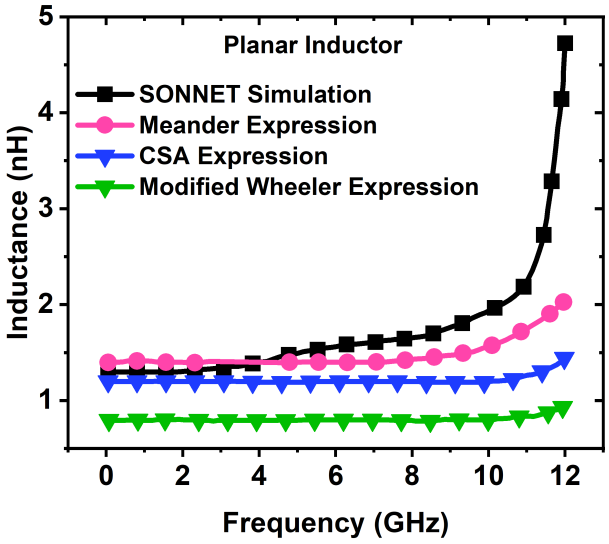


Figure 4.9: Inductance comparison of simulated and analytical expression results for a planar inductor

4.4 Frequency Dependent Inductance Extraction using Integral method

The performance validation of the previously proposed multilayer inductors is theoretically established through fundamental electromagnetic field principles. Extracting the inductance for any design structure involves solving Maxwell's equations. The magnetic potential associated with a conductor is derived from the magnetic force induced by the electromagnetic field. This force arises from three primary factors:

- The presence of current in an external magnetic field.
- Movement of charged particles.
- Interaction between two current elements.

The magnetic force found within the suggested inductors arises from the current elements situated amidst the conductors. The magnetic potential associated with line, surface, and volume currents can be described as:

$$A = \int \frac{\mu_0 I}{4\pi R} dl \; - - - - - - - - (line\ current) \tag{4.20}$$

$$A = \int \frac{\mu_0 K}{4\pi R} dS \; - - - - - - - - (surface\ current) \tag{4.21}$$

$$A = \int \frac{\mu_0 J}{4\pi R} dV - - - - - - - - (volume\ current) \tag{4.22}$$

In Fig. 4.1, we observe a 3-turn square inductor with 12 conductor segments, each numbered for easy identification. When these segments are parallel to each other, an electromagnetic field manifests between them, leading to the development of mutual inductance. This mutual inductance can be either positive or negative depending on the direction of the current flow. Positive mutual inductance occurs between specific segment combinations: {1, 5, 9}, {2, 6, 10}, {3, 7, 11}, and {4, 8, 12}. Conversely, negative mutual inductance arises between segment combinations: {1, 3, 7, 11}, {5, 3, 7, 11}, {9, 3, 7, 11}, {2, 4, 8, 12}, {6, 4, 8, 12}, and {10, 4, 8, 12}. Let's analyze the depicted conductor pair as shown in Fig. 4.10 to determine the mutual inductance value.

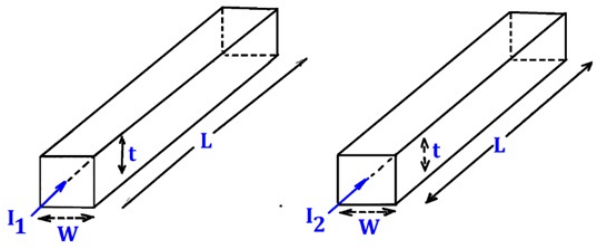


Figure 4.10: conductor pair structure to find current flow

If we have two conductor currents flowing along the Z-direction, represented as and, where I_1 and I_2 are the magnitudes of the currents, and β_1 and β_2 are the phase constants associated with each current, respectively. Assuming that the length of the conductor is much smaller than the wavelength, we can consider the phase associated with the conductor current flow to be zero over the entire length of the conductor. In this scenario, the vector magnetic potential developed due to the conductor current flow can be expressed as:

$$A_z(x, y, z) = \int \frac{\mu_0 I e^{-j\beta z}}{4\pi \sqrt{(x-0)^2 + (y-0)^2 + (z-z^{|})^2}} dz \tag{4.23}$$

If the length of the conductor is significantly shorter than the wavelength, the currents I_1 and I_2 with a density J within volume V are evenly spread throughout the rectangular cross-section. The expression for magnetic potential is

$$A_z(x, y, z) = \frac{\mu_0 I}{4\pi} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta z}}{\sqrt{(x-0)^2 + (y-0)^2 + (z-z^{|})^2}} dz \tag{4.24}$$

The magnetic field B is calculated as the curl of the magnetic potential A, expressed as

$$B = \nabla \times A \tag{4.25}$$

The magnetic flux through the center of a conductor is closely linked to the turns of metal around it. Magnetic flux refers to the magnetic field that penetrates the cross-sectional area of the second conductor.

$$\varphi_{21} = \oint Bds = \mu \int Hds = \int (\nabla \times A)\, ds \tag{4.26}$$

Stokes' theorem establishes a fundamental connection between a closed current path and the potential A associated with it. It states that the potential A can be determined by evaluating the surface integral of the curl of A over the enclosed surface S. This theorem operates under the assumption that both the potential A and its curl $\nabla \times A$ maintain continuity across the surface S.

$$\int (\nabla \times A)\, ds = \int Adl \tag{4.27}$$

When considering conductors separated by a distance d in the x-direction, the magnetic potential between them can be expressed using equation 4.21 as:

$$A_z\,(x, y, z) = \frac{\mu_0 I}{4\pi} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta z}}{\sqrt{(d)^2 + (z - z^{|})^2}} dz \tag{4.28}$$

The total flux (φ_{21}) in the second conductor is now recalculated as follows:

$$\varphi_{21} = \int A_z\,(d, 0, z)\, dz \tag{4.29}$$

Replace Eq. 4.25 with its expression in Eq. 4.22 to derive the flux as

$$\varphi_{21} = \frac{\mu_0 I_1}{4\pi} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta z^{|}}}{\sqrt{(d)^2 + (z - z^{|})^2}} dz^{|} dz = \frac{\mu_0 I_1}{4\pi} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta z^{|}}}{\sqrt{(d)^2 + (z - z^{|})^2}} dz dz^{|} \tag{4.30}$$

Assume that $t = (z - z^{|})/d$. Now perform differentiation of flux w.r.t. $z^{|}$ by considering z as constant. Then dz = d.dt. The expression for flux becomes

$$\varphi_{21} = \frac{\mu_0 I_1}{4\pi} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \left\{ \int_{-\frac{\frac{l_2}{2} - z^{|}}{d}}^{\frac{\frac{l_2}{2} + z^{|}}{d}} \frac{e^{-j\beta z^{|}}}{\sqrt{1 + t^2}} dt \right\} dz^{|} = \frac{\mu_0 I_1}{4\pi} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} e^{-j\beta z^{|}} \left\{ \int_{-\frac{\frac{l_2}{2} - z^{|}}{d}}^{\frac{\frac{l_2}{2} + z^{|}}{d}} \frac{1}{\sqrt{1 + t^2}} dt \right\} dz^{|} \tag{4.31}$$

$$\varphi_{21} = \frac{\mu_0 I_1}{4\pi} \int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} e^{-j\beta_1 z^{|}} \left\{ sinh^{-1}\left(\frac{\frac{l_2}{2} + z^{|}}{d} \right) - sinh^{-1}\left(\frac{-\frac{l_2}{2} - z^{|}}{d} \right) \right\} dz^{|} \tag{4.32}$$

The given expression can be solved using numerical integration, where higher-order terms are disregarded, resulting in the determination of the flux

$$\varphi_{21} = \frac{\mu_0 I_1}{\pi}\left\{aA\left(1 + \frac{\beta_1^2 a^2}{8} + \frac{\beta_1^4 a^4}{120}\right) - \frac{a^3 b B^3}{6} t_1\right\} \tag{4.33}$$

where,

$$a = \frac{t_1}{2}; b = \frac{t_2}{2}; A = log\left\{\frac{l_2}{2d} + \sqrt{1 + \left(\frac{l_2}{2d}\right)^2}\right\} \tag{4.34}$$

$$B = \frac{1}{\sqrt{d^2 + \left(\frac{l_2}{2}\right)^2}}; t_1 = 1 + \left\{\frac{6\beta_1^2 a^2 - 9B^2 a^2 + 15b^2 B^4 a^2}{20}\right\} \tag{4.35}$$

$$\beta_1 = \frac{2\pi}{\lambda_{eff}}; \lambda_{eff} = \frac{c}{f_0 \epsilon_{eff}}; \epsilon_{eff} = \frac{(T_{Si} + T_{Sio2})\,\epsilon_{Si}\epsilon_{Sio2}}{T_{Si}\epsilon_{Sio2} + T_{Sio2}\epsilon_{Si}} \tag{4.36}$$

Where $T_{Si}, \epsilon_{Si}, \epsilon_{Sio2}$ represents thickness, dielectric constant of silicon material and oxide dielectric constant respectively. The equation (4.30) governing magnetic flux is resolved through numerical integration, resulting in a solution which is subsequently applied within the mutual inductance equation.

Inductance refers to the relationship between the total magnetic flux linking a circuit and the current flowing through it. Self-inductance, denoted as L, is the ratio of the total magnetic flux ϕ to the current I in a circuit, expressed as L = ϕ/I. Mutual inductance, on the other hand, describes the induction of voltage in one circuit due to the changing magnetic flux produced by another nearby circuit. Specifically, the mutual inductance developed on conductor turn 2, induced by the magnetic flux from another conductor turn 1, can be mathematically represented.

$$M_{21} = \frac{\varphi_2}{I_1} = \frac{\mu_0 I_1}{4\pi}\left\{\frac{\varphi_{21}}{I_2 e^{-j\beta_2 z}}\right\} = \frac{\mu_0 I_1}{4\pi I_2}\left\{\frac{\varphi_{21}}{e^{-j\beta_2 z}}\right\} \tag{4.37}$$

When conductor losses are minimized, the currents flowing through all the conductors become equal. Consequently, the currents I_1 and I_1 in the equation cancel each other out. Thus, the mutual inductance can be expressed as:

$$M_{21} = \frac{\mu_0}{4\pi}\left\{\frac{\varphi_{21}}{e^{-j\beta_2 z}}\right\} \tag{4.38}$$

The performance of numerical integral methods is evaluated against SONNET simulation results for planar, 3D, and multilayer inductors. The comparative analysis is presented through plots in Fig. 4.11, 4.12, and 4.13. The aforementioned findings demonstrate that the proposed integral model exhibits superior accuracy in inductance calculation, as evidenced by its

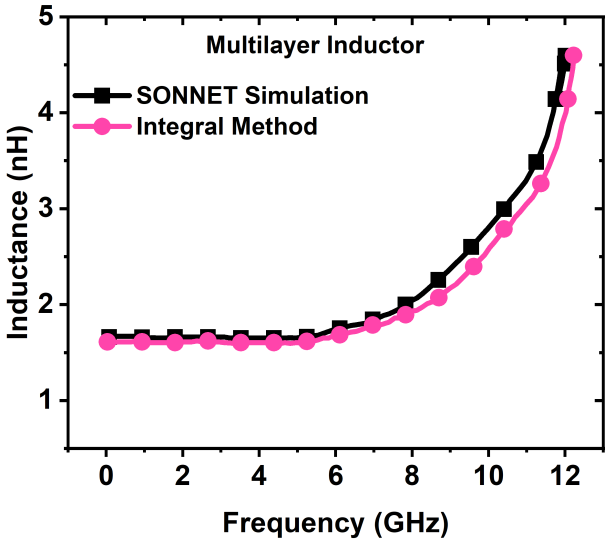


Figure 4.11: Inductance comparison of simulated and analytical expression results for a multilayer inductor

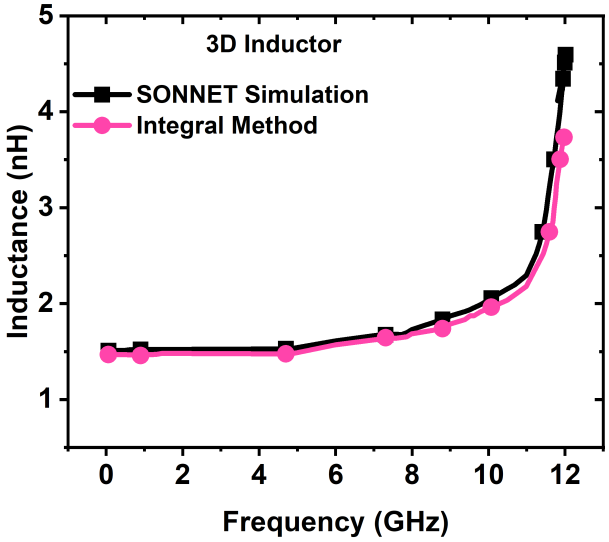


Figure 4.12: Inductance comparison of simulated and analytical expression results for a 3D inductor

close alignment with simulated results obtained from the SONNET simulation environment. The maximum error percentages for the integral solving model compared to the simulation results are 1.21%, 1.6%, and 2.3% at a frequency of 5 GHz for multilayer, 3-D, and planar inductors, respectively. Additionally, it is observed that error percentages increase beyond the Self-Resonant Frequency (SRF). It can be inferred that although the integral-based inductance extraction method offers greater precision, it necessitates a more complex numerical integration process. These findings corroborate closely with electromagnetic field solvers like SONNET, affirming the acceptability of SONNET simulation results for practical application in designing

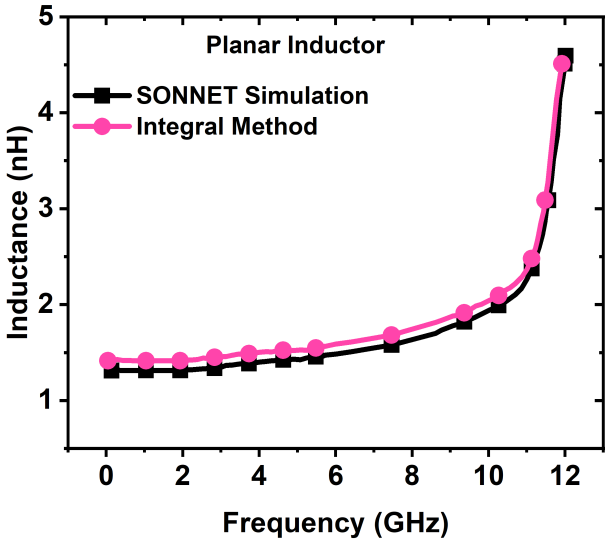


Figure 4.13: Inductance comparison of simulated and analytical expression results for a planar inductor

and developing high-performance 5G Radio Frequency Integrated Circuits (RFICs) utilizing the proposed on-chip components.

4.5 Summary

This chapter delves into inductance extraction techniques aimed at validating the simulation and experimental outcomes concerning the proposed on-chip passive components. Utilizing analytical expressions such as the modified Wheeler, Greenhouse, CSA, and numerical integration models, the study evaluates the performance of proposed inductor structures: Planar, 3D, and multilayer. The analysis reveals discrepancies between theoretical values and simulated results, particularly evident at high frequencies exceeding 6 GHz. The maximum percentage of error observed for the multilayer, 3D, and planar inductors at 5.0 GHz stands at 108%, 90%, and 87%, respectively. However, when employing the integral solving model, the maximum error percentages with respect to simulation results decrease substantially to 1.21%, 1.6%, and 2.3% at 5 GHz frequency for the aforementioned inductors, respectively. Thus, it can be inferred that numerical integral method-based inductance extraction proves more accurate, as evidenced by close agreement with field solver tool.

Chapter 5

Voltage Controlled Oscillator for Telemetry Transponder Applications

5.1 Introduction

Voltage-controlled oscillators (VCOs) are pivotal components in telemetry and transponder applications due to their ability to generate precise and tunable frequencies. One of the primary benefits of VCOs is their frequency stability. They can rapidly adjust their output frequency in response to varying control voltages, allowing for dynamic frequency selection. This adaptability is crucial in telemetry systems, which often operate in environments with significant frequency congestion or interference. The ability of VCOs to maintain stable and accurate frequencies ensures reliable communication links, which is essential for the continuous transmission of data. In transponder applications, VCOs are integral to the functioning of radar and communication systems. They enable the generation of high-frequency signals required for detecting and tracking objects, as well as for secure communication. The ability of VCOs to swiftly change frequencies allows transponders to respond accurately to incoming signals, thereby enhancing the resolution and accuracy of radar systems. Additionally, in communication transponders, VCOs facilitate frequency translation, which is crucial for ensuring that signals are transmitted and received correctly over different frequency bands. In this the design and performance metrics of the VCO is studied with various proposed On-chip inductors.

5.2 VCO design with Proposed Coupled pyramid inductor

The designed pyramid inductor finds applications in amplifiers, VCOs, and filters. The performance of the coupled inductor is assessed by using it in the resonant tank circuit of a VCO. The Clapp configuration is used to design the basic oscillator, as it performs better at higher frequencies. The oscillator is then tuned using a varactor diode to vary the output frequency. The Clapp oscillator consists of an amplifier in a common emitter configuration, providing the requisite gain and 180^0 phase shift. The resonant circuit provides an additional 180^0 phase shift to satisfy Bark Hausen criteria as shown in Fig. 5.1. The coupling capacitors at the input and output of the amplifier are used to block DC bias from disturbing the source and load. The design steps for the Clapp oscillator are given in Ref. [119]. The design is based on the above reference. The frequency of oscillation for the circuit is dependent on the inductor and the varactor capacitance and is given in Eq. 5.1.

$$\omega_0 = \frac{1}{\sqrt{L_{cpi}C_{var}}} \tag{5.1}$$

where, L_{cpi} is the inductance of the coupled inductor and C_{var} is the tunable varactor diode capacitance. The varactor diode capacitance is varied by applying a reverse bias across the diode,

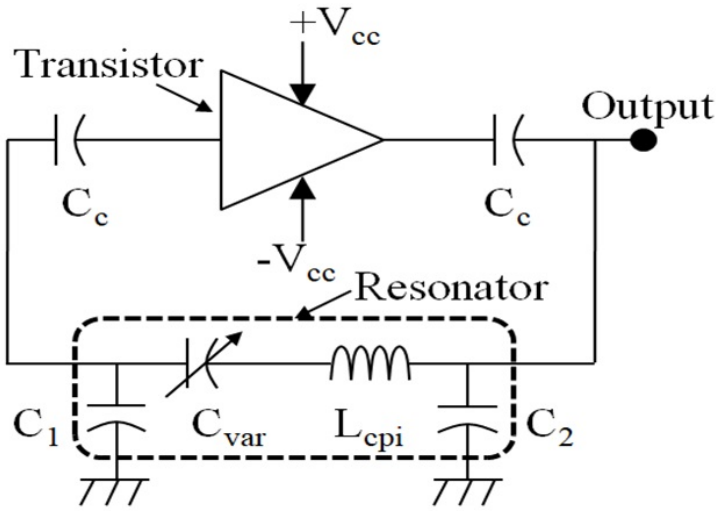


Figure 5.1: Block diagram of VCO in Clapp oscillator

and as the voltage is increased, the capacitance of the varactor diode decreases. SMV2019-040LF varactor diode is used whose capacitance varies from 0.4 pF to 1.8 pF for change in bias voltage from 0 V to 15 V.

The biasing circuit consists of a lowpass filter and a resistor to control the current. The lowpass filter blocks the RF signal from entering the DC supply. The transistor source is grounded

using multiple vias as shown in Fig. 5.2. The input and output capacitors block the DC from leaking through resonator and load resistance. The S-parameters of the coupled inductor are imported from SONNET software and used in the schematic for the resonator circuit and the varactor spice model is used. This circuit selects the output frequency of the oscillator. The tuning capacitance determines the tuning ranging for the VCO. The simulated output spectrum

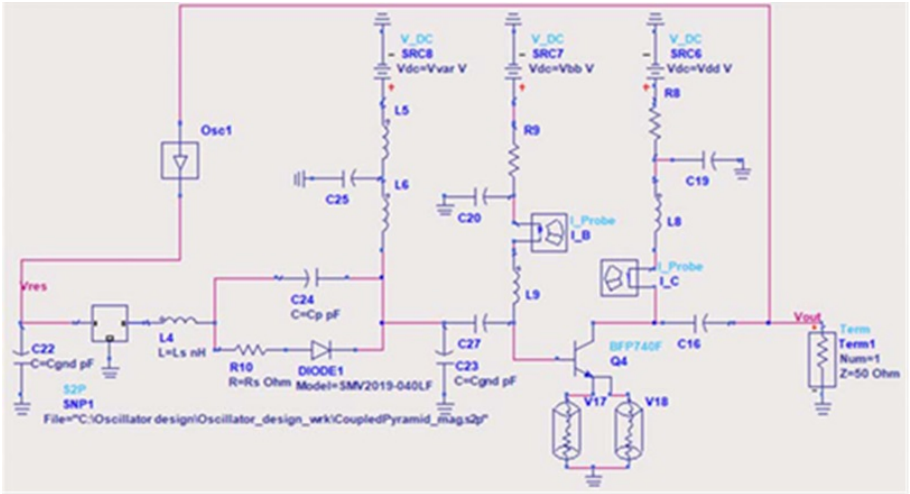


Figure 5.2: Circuit diagram of the VCO in Clapp oscillator configuration

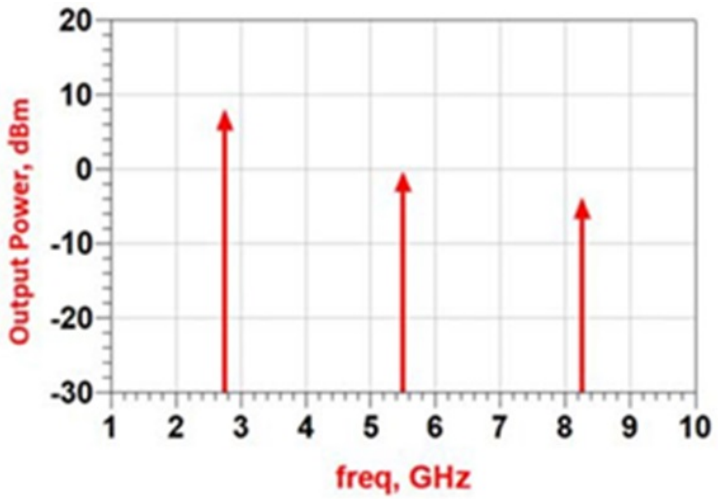


Figure 5.3: Output VCO Spectrum

of the VCO is shown in Fig. 5.3. The output power of the VCO is 7.56 dBm. The tuning range of the VCO is shown in Fig. 5.4. It is observed that the capacitance variation in the varactor results in a frequency change from 2.75 GHz to 3.59 GHz. The frequency tuning range is 0.84 GHz which is 26.4% of the centre frequency. The output power variation is shown with frequency in Fig. 5.8. It is observed that the power is constant till 3.3 GHz, and the power falls off to 4.5 dBm at 3.59 GHz.

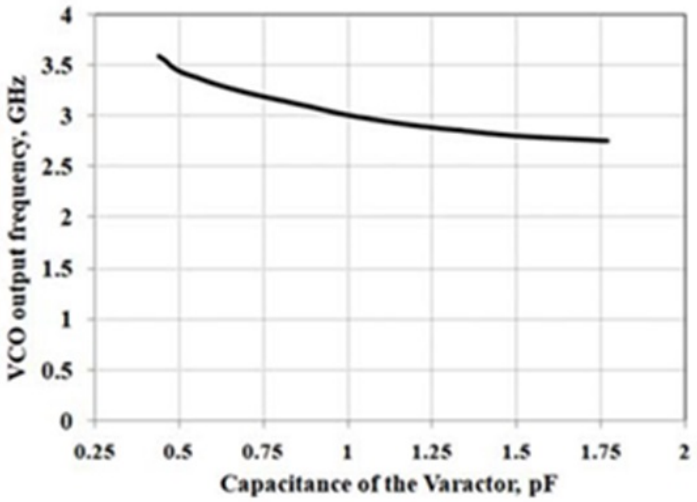


Figure 5.4: VCO output frequency variation over Varactor capacitance

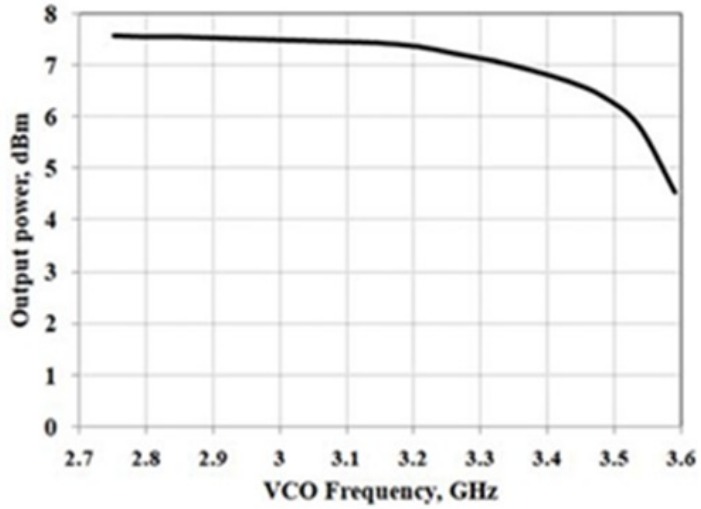


Figure 5.5: Output power over the frequency band of VCO

The VCO phase noise and FoM results are shown in Fig. 5.6 at 2.75 GHz. It is observed that the VCO exhibits a phase noise of -65.55 dBc/Hz at 1 KHz offset, -125.55 dBc/Hz at 1 MHz offset, and FoM of -215.47 dBc/Hz at 1 MHz offset. The phase noise and FoM values exhibited by the VCO are due to improved quality factors and higher inductance values in compact size. This shows that the coupling effects and the losses have been suppressed with the coupled pyramid inductor. The variation of phase noise at 1 KHz offset is shown in Fig. 5.7; it is observed that the phase noise increases as the output frequency increases due to changes in the resonator's quality factor. Finally, the Phase noise and FoM at 1 MHz are plotted for output frequency in Fig. 5.8. The variation is as predicted due to changes in the Q-factor of the resonant circuit.

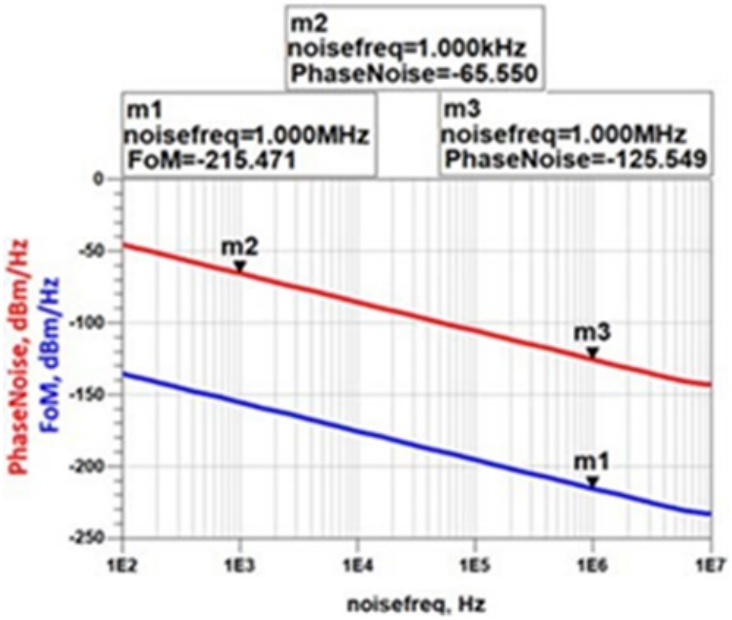


Figure 5.6: VCO phase noise and Figure of merit (FoM) at 2.75 GHz

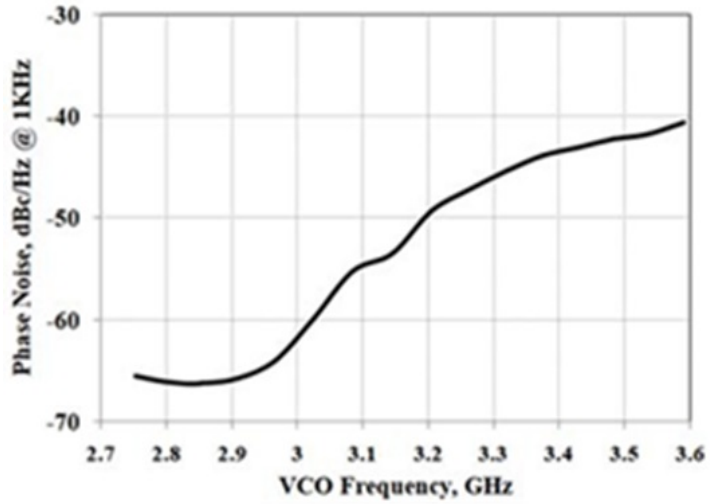


Figure 5.7: Phase noise at 1 KHz offset over the frequency band of VCO

The comparison of the performance parameters of the proposed VCO with other reported structure is shown in Table 5.1. The output power of the 7.43 dB at centre frequency is higher than other designs, however, the power dissipation is slightly higher than other designs. This is compensated with the output power. The tuning range for the reported VCO is 26.4% whereas for ref [120] it is 20%. The phase noise of the proposed VCO at 1 KHz offset is better than ref [121] at - 53.5dBc/Hz. The FoM considers all the important parameters of the VCO such as phase noise, tuning range, centre frequency and power dissipation, hence, gives the overall performance parameter of the VCO and is an important factor in comparison of the VCOs. The FoM of the proposed VCO is -204.5 dBc/Hz @ 1 MHz offset, which is the best among the reported VCOs.

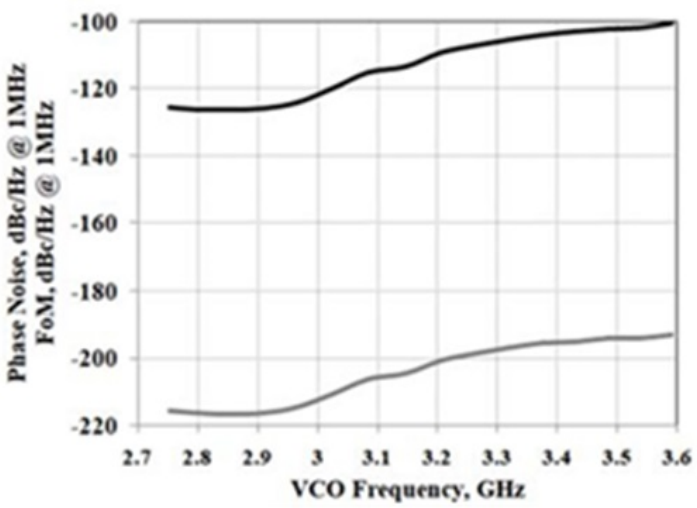


Figure 5.8: Phase noise and FoM over the frequency band of VCO

Table 5.1: Comparison of Proposed work with existing literature

Parameter	[121]	[122]	[120]	[123]	Proposed work
Supply voltage (V)	-	1.8	1.2	3.3	1.2
Power consumption (mW)	1.5	7.3	5.4	-	7.68
Tuning range (GHz)	3.6	2.506	4.5-5.5	1.6	2.752-3.59
Output Power (dBm)	-	-9.8	-	-	7.43
PN dBc/Hz @ 1 KHz	-45	-	-	-	53.5
PN dBc/Hz @ 1 MHz	-118.2	-123.7	-119.7	-139.4	-113.5
FoM dBc/Hz @ 1 MHz	-189.9	-188.9	-184.6	-184	-204.5

5.3 Design and simulation of the VCO with Proposed Multilayer Inductor

To evaluate the performance of a VCO, a multilayer inductor is incorporated into the design, aiming to assess its effectiveness in mitigating phase noise and enhancing the figure of merit (FoM) of the oscillator. The VCO is constructed using the Clapp configuration, which is particularly well-suited for high-frequency applications. This configuration entails an oscillatory circuit composed of an amplifying device and a resonant circuit. The amplifying device compensates for losses within the resonant circuit, while the resonant circuit selects the desired frequency at the oscillator's output. Both components adhere to the Barkhausen criterion, ensuring a loop gain equal to one. In this specific design, a Silicon Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) serves as the amplifying device, while the resonant circuit is created using an LC resonator circuit, as depicted in Fig. 5.9. The transistor is biased using an inductor (L_b) and a capacitor (C_b), with an additional coupling capacitor (C_c) facilitating the coupling

of the RF signal to the output. The VCO design is finalized by substituting the capacitor in the resonant circuit with a varactor diode. This substitution allows for the modulation of the output frequency by varying the capacitance of the varactor diode.

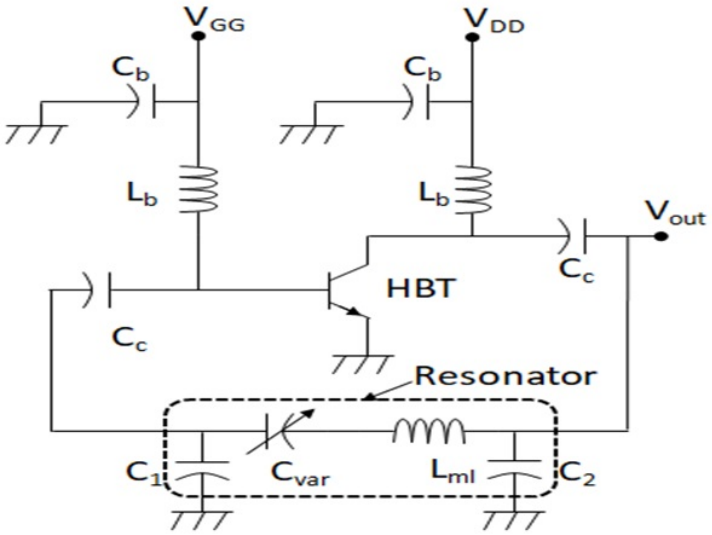


Figure 5.9: Clamp oscillator circuit with varactor diode

The initial phase of oscillator circuit design commences with the formulation of the resonant circuit [119]. This circuit configuration encompasses the integration of the multilayer inductor and varactor diode, complemented by capacitances denoted as C_1 and C_2. The selection of varactor diode and multilayer inductor values is meticulously conducted in accordance with the predetermined specifications stipulated for the VCO. The resonant frequency is given in Eq. 5.2.

$$\omega_0 = \frac{1}{\sqrt{L_{ml}C_{var}}} \tag{5.2}$$

where L_{ml} is the multi-layer inductance and C_{var} is the varactor capacitance. The proposed multilayer inductor designed is used for the design of VCO resonant circuit. The inductance value of the inductor is 3.25 nH, the Q factor of the inductor at 3 GHz is 16.65. The capacitances values for a given frequency are calculated using Eqs. (5.3 - 5.5).

$$R_s = \frac{\omega L_{ml}}{Q} \tag{5.3}$$

$$C_1^2 < \frac{g_m}{\omega^2 R_s} \tag{5.4}$$

$$X_{c_{var}} = -X_L - 2X_{C_2} \tag{5.5}$$

The design steps followed for designing the VCO are given below.

- Determine the operating point, calculate the value of g_m.
- Using the value of the inductor and unloaded Q of the inductor determine the value of series resistance of the inductor.
- Calculate the value of capacitance (C_1).
- Consider $C_1 = C_2$ and then calculate the value of C_{var} to get the oscillator frequency.

The varactor diode chosen for the given resonant frequency of 3 GHz is SMV-1408, whose capacitance value changes from 2 pF to 0.2 pF for a bias voltage of 0 V to 20 V. The SiGe HBT transistor is biased to provide a gain sufficient to meet the loop gain requirement, satisfying the Bark Hausen criterion. The FoM for an oscillator considering the phase noise, frequency and power dissipated is given by Eq. 5.6 [124]

$$FoM = L\{\Delta f\} - 20log_{10}^{\left(\frac{f_0}{\Delta f}\right)} + 10log_{10}^{\left(\frac{P_{dc}}{1mW}\right)} \tag{5.6}$$

Where, $L\{\Delta f\}$ is the phase noise, f_0 is the centre frequency, Δf is the tuning bandwidth, P_{dc} is the DC power dissipation. The schematic simulation of the VCO circuit is shown in Fig. 5.10. The design steps described above have been used in the design of the schematic VCO. The transistor is biased using an inductor of 1 nH and a capacitor of 100 pF. The current flowing through the transistor is controlled using the base resistor (100 Ω) and collector resistors (22 Ω). Finally, multiple vias are used at the emitter of the transistor to reduce the effective inductance to the ground, which might reduce the gain of the transistor and result in negative feedback.

The simulated frequency spectrum at the output of the VCO is shown in Fig. 5.11. The results show that the output power for the VCO is 7.5 dBm, and the second and third harmonics are attenuated by 20 dB and 15 dB, respectively. The time-domain signal at the output is shown in Fig. 5.12. The signal shows a sinusoidal signal with minimal distortion from the harmonic content of the oscillator. This shows that the resonant circuit can reject higher order harmonics and select the required fundamental frequencies. Further, the phase noise characteristics and the FoM are shown in Fig. 5.14. The output poer of the VCO is depicted in Fig. 5.13. These results corroborate the fact that the Q factor of the multilayer inductor results in better phase noise and FoM but also helps in reducing the effect of higher harmonics of the oscillator.

In Table 5.2, a comparative analysis of the designed VCO is presented alongside several recently published works. It becomes evident that the proposed VCO, featuring a multilayer inductor, outperforms other references in various key metrics. Notably, the proposed VCO

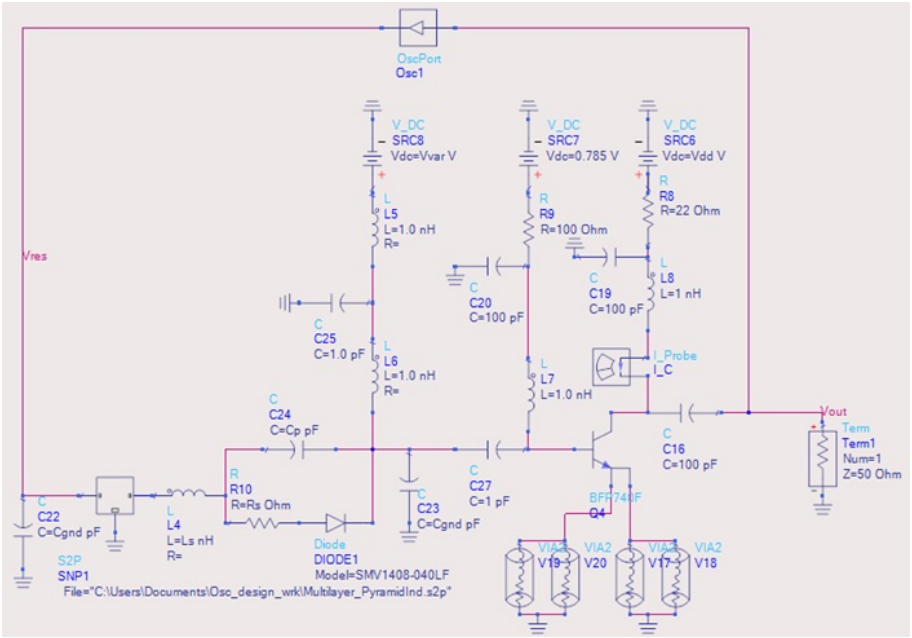


Figure 5.10: The Schematic circuit of VCO in ADS

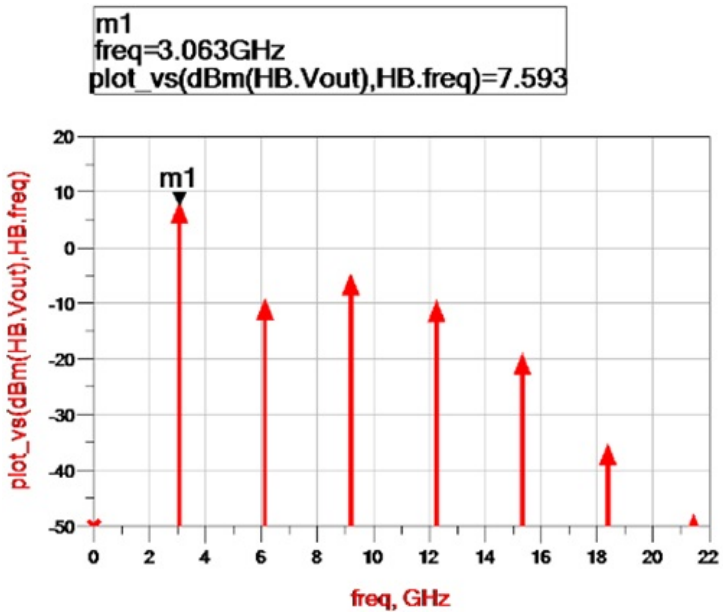


Figure 5.11: Frequency spectrum at the output of the VCO

demonstrates superior power consumption compared to works cited as [125], [126], and [120]. Additionally, its tuning range surpasses that of references [125] and [126]. In terms of phase noise, the proposed VCO exhibits the best performance at a 1 kHz offset from the carrier when compared to all referenced works. Furthermore, at a 1 MHz offset from the carrier, the proposed VCO outperforms references [126] and [127] in terms of phase noise. However, the most striking observation emerges from the FoM evaluation, where the proposed VCO achieves the highest FoM among all references, calculated at -208 dBc/Hz. This comprehensive metric accounts for various parameters such as center frequency, tuning range, power dissipation, and

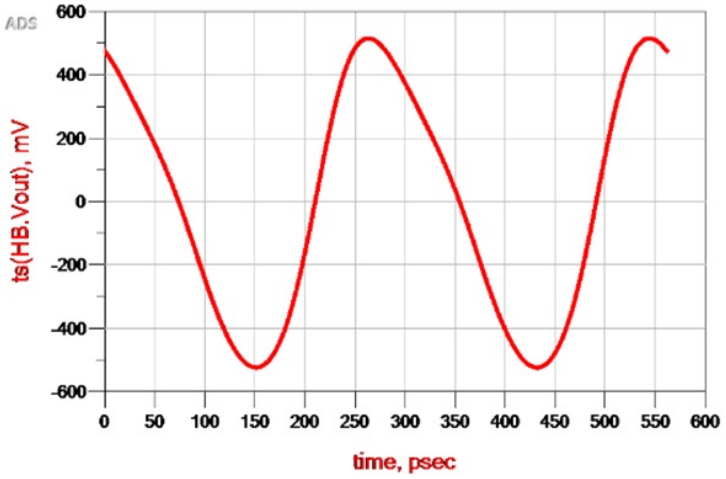


Figure 5.12: Time domain signal at the output of the VCO

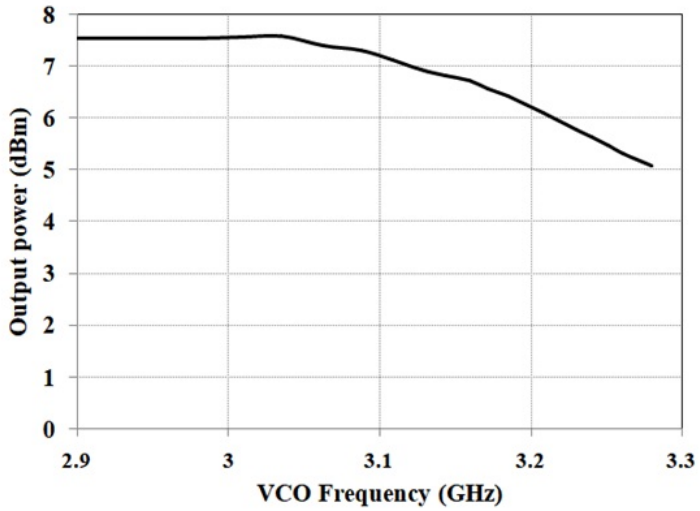


Figure 5.13: Output power of the VCO

phase noise. Consequently, it becomes evident that the proposed VCO featuring a multilayer inductor stands out as the optimal choice, offering superior performance across a spectrum of critical parameters.

Table 5.2: Comparison of Proposed work with existing literature

Parameter	**[125]**	**[126]**	**[127]**	**[120]**	**[128]**	**[124]**	**Proposed work**
Supply voltage (V)	1.2	1.8	1	-	1.2	1.2	1.2
Power consumption (mW)	8.56	50.2	0.17	22	5.4	2.4	7.7
Tuning range (GHz)	2.415-2.50	2.49-2.67	1.38-3.16	2	4.5-5.5	2	2.9-3.28
Output Power (dBm)	-	-10.09	8.34	-	-	-	5.08
PN dBc/Hz @ 1 KHz	-40	-50	-	-	-	-53	-55.5
PN dBc/Hz @ 1 MHz	-140	-108.8	-71	-124	-119.7	-130	-115.5
FoM dBc/Hz @ 1 MHz	-160	-	-143.09	-184.6	-184.6	-192.3	-208.08

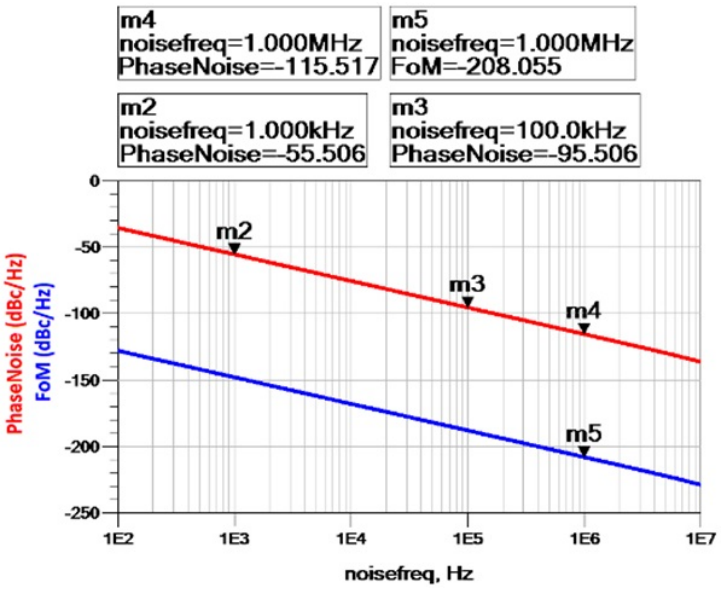


Figure 5.14: Phase noise and Figure of Merit (FoM) plot for the designed VCO

5.4 Summary

To validate the efficacy of the proposed inductors, including both coupled pyramid and multilayer variants, as VCO was designed and analyzed. The VCO with coupled pyramid demonstrates a phase noise of -53.5 dBc/Hz at 1 KHz which shows that improved quality factor of the inductor. The figure of merit of the coupled pyramid is -204 dBc/Hz demonstrating the superiority of the inductor in terms of quality factor, output power, and tuning range compared to other reported inductor based VCOs. Further, the multilayer inductor which is a modification of the coupled inductor exhibits better characteristics as mentioned in the earlier chapter. In the VCO design, the multilayer inductor provides better quality factor which results in higher figure of merit. The FoM for the multilayer inductor based VCO is -208 dBc/Hz @ 1 MHz offset with a phase noise of -55.5 dBc/Hz at 1 KHz offset. The versatility and effectiveness of the proposed inductors render them highly suitable for applications such as filtes, amplifiers, oscillators and telemetry transponder systems.

Chapter 6

Low Noise Amplifier for 5G Applications

6.1 Introduction

The Low Noise Amplifier (LNA) serves as a key component in wireless receivers, playing a pivotal role in amplifying input signals from the antenna to an appropriate level while maintaining a high signal-to-noise ratio (SNR). Crucially, LNAs must exhibit excellent input impedance matching to accommodate large signals without introducing distortions. With the ongoing evolution of telemetry and transponder applications, the performance of the front-end radio assumes paramount importance, with particular emphasis on LNA functionality. In addition to signal amplification, modern LNAs are also expected to minimize power consumption, a crucial consideration in portable mobile communications. However, designing LNAs involves navigating various trade-offs among key performance metrics such as gain, linearity, noise figure, input matching, and power consumption. The integration of LNAs into System-on-Chip (SOC) designs necessitates high-performance transistors with high f_T and high-Q inductors. One approach to enhancing LNA performance is through the use of multilayer inductors, which offer improved noise performance while minimizing on-chip area. By leveraging proposed multilayer inductors with high-Q factors, implemented LNAs can achieve superior matching with minimal parasitic capacitance.

6.2 LNA design with proposed Inductors

This section focuses on evaluating the performance of the coupled pyramid and multilayer inductors within the input noise-matching network of a LNA. The LNA employs a basic amplifier configured in a common emitter with inductive degeneration. The amplifier's input is noise-matched using a shunt inductance and series capacitance, as illustrated in Fig. 6.1. Additionally, the series capacitance serves as a blocking capacitor to prevent DC leakage. The biasing circuit for the amplifier incorporates a low-pass filter and current-controlling resistors [129]. Specifically, the base bias employs a low-pass filter comprising a shunt capacitor, while the drain bias features a parallel tank circuit, shunt capacitor, and current-controlling resistors. Output matching is achieved through an LC network, consisting of a shunt capacitor and series inductor for power matching.

Given the transistor's instability at operational frequencies, shunt inductances are employed to stabilize it, with two inductors utilized to mitigate parasitic resistance. This negative feedback resistance serves to reduce the amplifier's gain. The optimized component values for the common emitter based LNA is depicted in Fig. 6.1. To analyze the amplifier circuit's performance, S-parameters are utilized to measure parameters including gain, input return loss, noise figure, and stability.

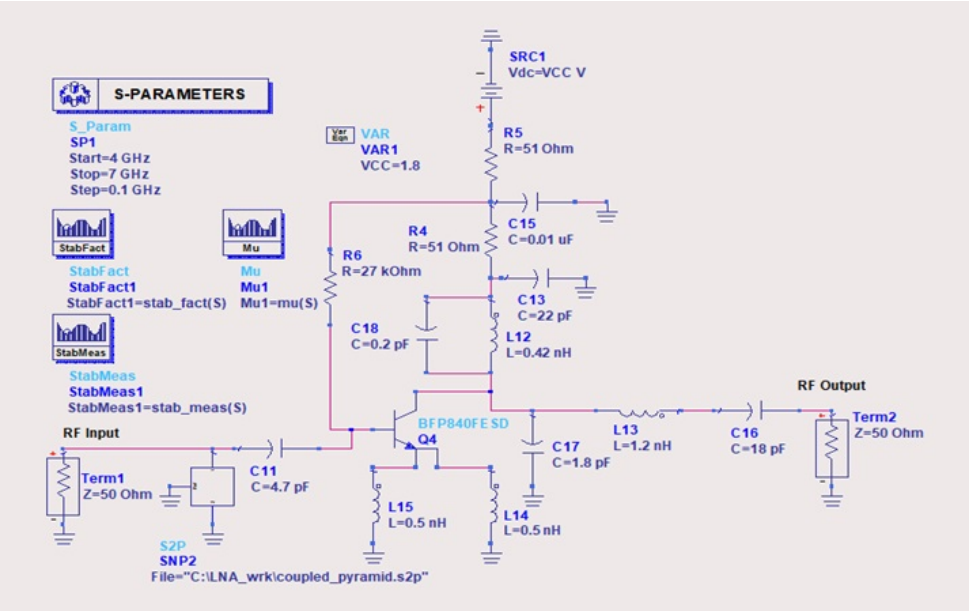


Figure 6.1: The LNA schematic

6.3 Results and Discussions

In this section the results of the both proposed coupled pyramid and multilayer inductor based LNA are analyzed.

6.3.1 LNA with coupled pyramid Inductor

In this the performance of LNA is evaluated using the proposed coupled pyramid Inductor. Fig. 6.2 illustrates a comparison between the S-parameters of the LNA utilizing the proposed Coupled Pyramid Inductor (CPI) and an inductor possessing a quality factor of 5, denoted as Q5. The single-stage LNA achieves a gain exceeding 15 dB (S_{21}), accompanied by input (S_{11}) and output return losses (S_{22}) surpassing 10 dB. Additionally, the isolation between the output and input ports exceeds 20 dB. Comparing the performance of the LNA with the proposed CPI and the Q5 inductor reveals that the proposed CPI exhibits a gain and isolation approximately 0.5 dB superior to that of the Q5 inductor. This improvement is primarily attributed to the insertion loss of the inductor. The potential for further tuning the gain of the LNA exists; however,

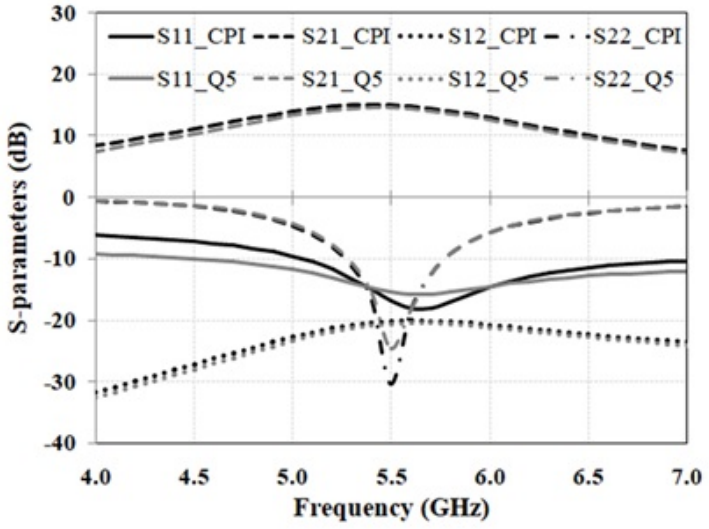


Figure 6.2: S-Parameters of the LNA

such adjustments would invariably lead to a degradation in the noise figure. This phenomenon is illustrated in Fig. 6.3, which depicts the simulated noise figure of the LNA. Specifically, at 5.5 GHz, the noise figure attributed to the proposed CPI stands at 1.09 dB, whereas that associated with the inductor possessing a quality factor of 5 is measured at 1.65 dB. The observed increase in noise figure can be attributed to the inherent quality factor and associated losses of

the inductor. This comparison underscores the efficacy of the proposed CPI in terms of quality factors. Despite the potential for a slight degradation in noise figure, the utilization of the proposed inductor offers notable advantages in terms of performance optimization and overall circuit efficiency. The stability factor of the LNA with the two inductors is shown in Fig. 6.4 .

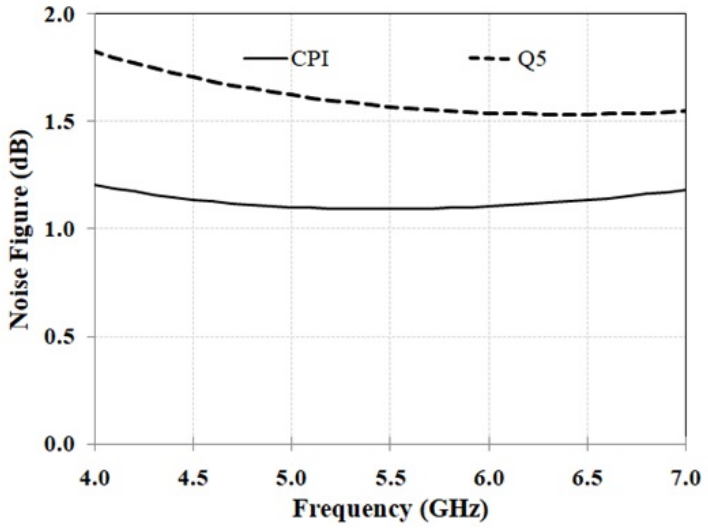


Figure 6.3: noise figure of LNA with coupled pyramid inductor

The LNA is stable with both inductors. The performance of the LNA can be estimated using a FoM given by Eq. 6.1.

$$FOM = \frac{G.F_0}{(NF_{min} - 1) * P_D} \tag{6.1}$$

Where G is the gain of the LNA, F_0 is the centre frequency in GHz, NF_{min} is the minimum

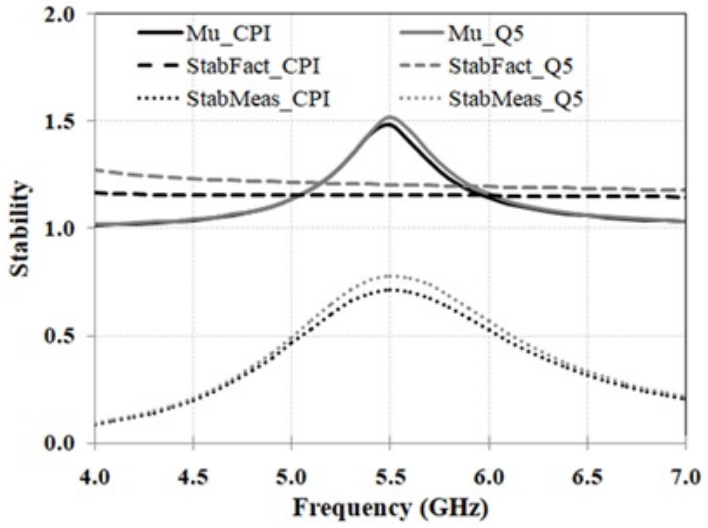


Figure 6.4: Stability of LNA with coupled pyramid inductor

noise figure value, and P_D is the power dissipated by the LNA in milli-Watts. The proposed

LNA achieves an impressive noise figure of 1.09 dB, which is the lowest among the referenced designs, demonstrating its superior noise performance. Additionally, it boasts the best FoM when compared to other designs. While the gain of the proposed LNA is somewhat lower due to its single-stage configuration, this is in contrast to other designs that employ cascaded or cascode configurations to enhance gain.

6.3.2 LNA with Multilayer Inductor

This focuses on evaluating the performance of the multilayer inductor (MLI) within the input noise-matching network of a LNA. The analysis highlights the impact of the proposed MLI on the LNA's S-parameters, noise figure and stability which are key indicators of the amplifier's performance. Fig. 6.5 illustrates the S-parameters for the LNA incorporating the proposed MLI. The single-stage LNA demonstrates a gain (S_{21}) exceeding 15 dB, indicating an effective amplification of the input signal, which is crucial for enhancing the overall sensitivity of the system. The input return loss (S_{11}) is greater than 10 dB, suggesting that the majority of the input signal is successfully transferred into the amplifier with minimal reflections, thereby maintaining signal integrity and reducing noise. Similarly, the output return loss (S_{22}) also surpasses 10 dB, ensuring that the output signal is efficiently delivered to the next stage of the system with minimal reflection back into the amplifier, optimizing power transfer and signal quality. Additionally, the isolation between the output and input ports (S_{12}) exceeds 20 dB, which is critical for preventing feedback from the output to the input, thus preserving the amplifier's performance and stability. The performance of a LNA is critically influenced by its gain and noise

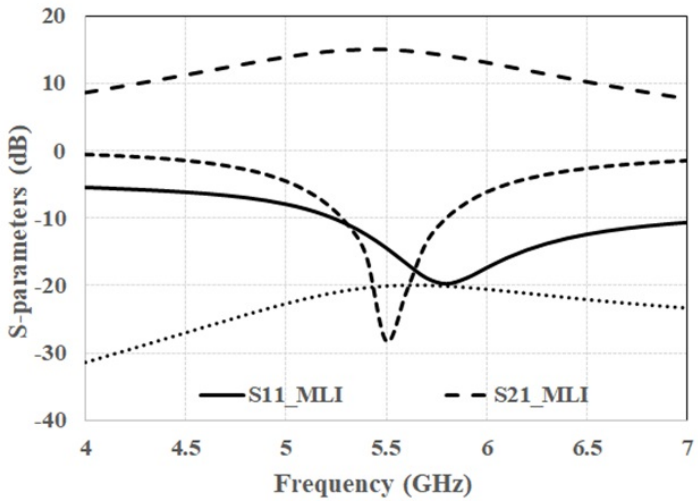


Figure 6.5: S-Parameters of the LNA

figure, both of which play significant roles in determining the amplifier's effectiveness. The

gain of an LNA can be adjusted or tuned to optimize performance; however, such tuning often comes at the cost of increased noise figure. The noise figure is a key parameter that quantifies the amount of additional noise introduced by the amplifier. In the simulation results depicted in Fig. 6.6, the noise figure of the LNA is analyzed across different frequencies. Specifically at a frequency of 5.5 GHz, where the noise figure is observed to be 1.09 dB when utilizing the proposed multilayer inductor in LNA circuit which is attributed to the quality factor (Q factor) and the associated losses of the multilayer inductor. The stability of a Low Noise Amplifier

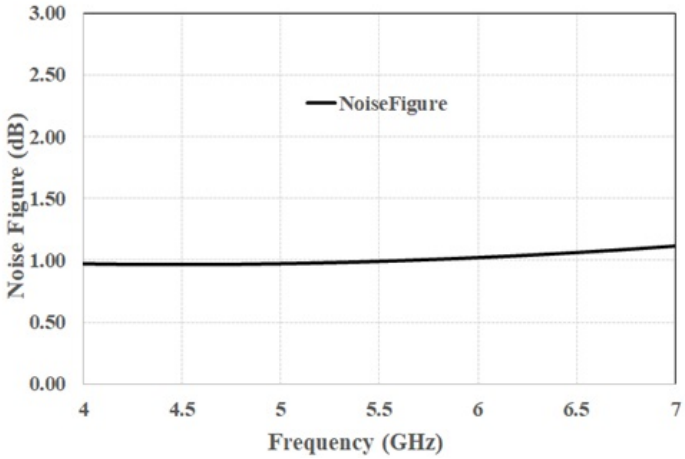


Figure 6.6: noise figure of LNA with MLI

(LNA) is crucial for its performance and reliability. Stability can be assessed using parameters such as the Stability Factor (K) and the Delta (Δ) parameter.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|} \tag{6.2}$$

where,

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{6.3}$$

Another parameter introduced to ensure the stability of the LNA for reliable operation is given by:

$$\Delta = \frac{1 - |S_{11}|^2}{\left|S_{22} - \Delta S_{11}^*\right| + |S_{12}S_{21}|} \tag{6.4}$$

In Fig. 6.7, the stability factor (K) of the LNA, indicating the impact of the multilayer inductor on overall stability, is illustrated. The stability parameters depicted include stab fact1 (K), stab meas1 (Δ), and μ_1. For the proposed LNA with a multilayer inductor, the values obtained are K = 0.800, μ = 0.633, and Δ = 0.118. Based on these results, where K > 1, Δ < 1, and $\mu_1 > 1$, it is demonstrated that the device is unconditionally stable.

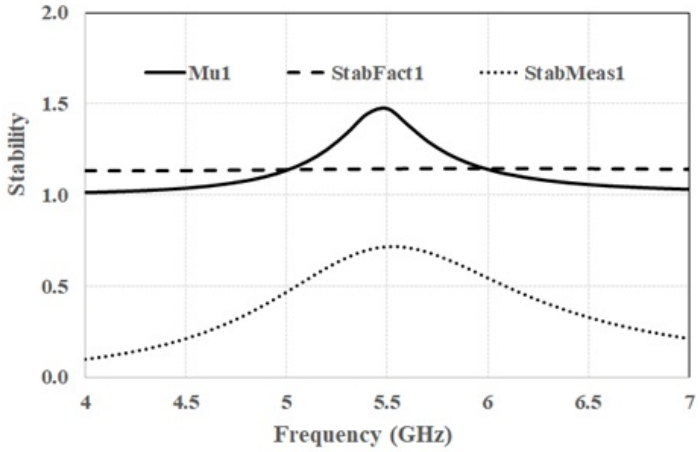


Figure 6.7: Stability of LNA with Multilayer inductor

Table 6.1: Comparison of LNA parameters

Parameters	**[130]**	**[131]**	**[132]**	**[133]**	**[134]**	**LNA with CPI**	**LNA with MLI**
Centre Frequency (GHz)	10	2.15	2.4	4.6	2.6	5.5	5.5
Gain (dB)	11	22	20	19.2	20.9	15.6	15.05
Noise Figure (dB)	1.9	2.4	3.9	3.1	2.6	1.09	0.98
Power dissipation (mW)	50	5	2	8.5	5.76	5.5	5.4
FoM	1.13	7.8	9.5	3.7	6.2	14.6	15.2

Table 6.1 compares the FOM of the proposed LNA with other recently published LNAs. The FoM for the LNA is a comprehensive metric that encapsulates all critical performance parameters, offering a robust measure of the LNA's overall effectiveness. In this context, the proposed LNA achieves a FoM of 14.6, 15.2 with couple pyramid and multilayer inductors, respectively. It reflects the proposed multilayer inductor balances and optimize the performance across various parameters such as noise figure, gain, power consumption, and linearity.

6.4 Summary

In this chapter, the design of a LNA leveraging coupled pyramid and multilayer inductors for 5G applications is discussed in detail. The validation of the inductor's performance is achieved through the design of the LNA's input matching circuit. Initially, an LNA with the coupled pyramid inductor achieves a notably lower noise figure of 1.09 dB while maintaining the gain of 15.6 dB at 5.5 GHz. To further enhance the performance, the design is subsequently modified by incorporating a multilayer inductor. This modification involves the strategic placing of each half turn into two different layers to reduce the effective capacitance, current crowding

effect and substrate losses. The LNA incorporating a multilayer inductor demonstrates a noise figure of 0.98 dB and a gain of 15.05 dB at 5.5 GHz. This substantial reduction in noise figure highlights the effectiveness of the multilayer inductor in minimizing noise and enhancing overall performance. The multilayer inductor exhibits superior inductance and quality factor compared to the coupled pyramid inductor, resulting in significant performance improvements. Specifically, the The enhanced performance characteristics of the multilayer make it exceptionally well-suited for the design of various RF components and receiver circuits. These attributes render it a valuable component in the development of advanced communication systems, particularly those operating in the demanding environment of 5G networks.

Chapter 7

Conclusions And Future Scope

7.1 Conclusions

This research has concentrated on designing on-chip multilayer passive components that exhibit high quality factor, high inductance, and high self-resonant frequency, specifically for RF integrated front-end circuits. The approach involved using thick substrates, multilayer concepts, and miniaturized areas to optimize on-chip performance. This chapter provides a summary of the work conducted and suggests potential directions for future research.

Initially, various spiral on-chip inductors, including planar inductors, half-turn split inductors, pyramid inductors, coupled pyramid inductors, and multilayer inductors, were proposed and analyzed. Among these, the half-turn split inductor demonstrated a remarkable 31.6% improvement in the quality (Q) factor compared to the standard planar inductor. Further to improve the inductance and quality factor at 5 GHz the coupled pyramid inductor designed which, offers a 35% improvement in the Q factor over the standard pyramid inductor. To improve the performance and Quality factor further the innovative design is proposed with multilayer inductor it shows a significant improvement, with a 17% increase in the Q factor over the coupled pyramid inductor. This substantial enhancement is attributed to its optimized design, which minimizes parasitic effects such as interwiring capacitance and current crowding. The optimal combination of inductance and Q factor is achieved with the multilayer inductor. This inductor's design is particularly advantageous for high-frequency RF applications, ranging from 1 GHz to 10 GHz. The simulation results underscore the efficacy of these proposed inductors, demonstrating their potential to significantly enhance the performance of RF integrated circuits.

The study employs a variety of analytical methods, including the modified Wheeler, Greenhouse, CSA, and numerical integration models, to evaluate the performance of different inductor structures: planar, 3D, and multilayer inductors. The analysis uncovers notable discrepancies between the theoretical values derived from these models and the simulated results, particularly at high frequencies above 6 GHz. These discrepancies highlight the limitations of traditional analytical models in accurately predicting inductor performance at higher frequencies. At 5.0 GHz, the study observes substantial error percentages between theoretical predictions and simulation results. Specifically, the maximum percentage errors for the multilayer, 3D, and planar inductors are found to be 108%, 90%, and 87%, respectively. These high error rates indicate significant deviations and underscore the challenges in achieving precise inductance and quality factor estimations using conventional analytical approaches. To address these inaccuracies, the study implements an integral solving model, which significantly enhances the precision of the inductance values. By solving integral equations derived from Maxwell's equations and magnetic flux expressions, this method accounts for the frequency-dependent characteristics of the inductors more accurately. As a result, the maximum error percentages with respect to the simulation results are drastically reduced. For the multilayer inductor, the error percentage decreases to 1.21%; for the 3D inductor, it drops to 1.6%; and for the planar inductor, it reduces to 2.3% at the 5 GHz frequency.

To validate the efficacy of the proposed inductors, particularly the coupled pyramid and the multilayer inductor, a voltage-controlled oscillator (VCO) was designed and subjected to detailed analysis. The VCO, when utilizing the coupled pyramid inductor, exhibited a significantly enhanced Figure of Merit (FoM), achieving -204 dBc/Hz at a 1 MHz offset. This configuration also demonstrated superior power efficiency and improved phase noise characteristics at a 1 kHz offset, underscoring the effectiveness of the pyramid inductor in high-frequency applications. Furthermore, the integration of the multilayer inductor into the VCO design yielded even more significant results. The VCO equipped with the multilayer inductor achieved an FoM of -208 dBc/Hz at a 1 MHz offset, representing a marked improvement over the pyramid inductor configuration. Additionally, this setup demonstrated enhanced phase noise performance at a 1 kHz offset and delivered higher output power, measuring at 7.5 dBm. These improvements highlight the multilayer inductor's superior ability to enhance VCO performance metrics.

The design of a Low Noise Amplifier (LNA) utilizing coupled pyramid and multilayer inductors for 5G applications is thoroughly explored in this study. The performance validation of these inductors is meticulously carried out through their integration into the LNA's input matching circuit. Initially, an LNA employing a coupled pyramid inductor is designed, showcasing a noise figure of 1.09 dB and a gain of 15.6 dB at a frequency of 5.5 GHz. To further enhance the

LNA's performance, the design is subsequently refined by incorporating a multilayer inductor. This enhancement involves a strategic placing of each half turn in to two different layers to reduce the effective capacitance, current crowding effect and substrate losses. The multilayer inductor, by virtue of its innovative design, demonstrates superior inductance and a higher quality factor in comparison to the coupled pyramid inductor. As a result of these improvements, the LNA equipped with the multilayer inductor achieves remarkable performance metrics. Most notably, the noise figure is significantly reduced to 0.98 dB, while maintaining the same gain of 15.6 dB at 5.5 GHz. This dramatic reduction in the noise figure underscores the efficacy of the multilayer inductor in minimizing noise, thereby enhancing the overall performance of the LNA. These advancements are particularly relevant for 5G communication systems, which demand high-performance, low-noise components to ensure reliable and efficient signal transmission. The multilayer inductor's ability to deliver superior performance in terms of both inductance and quality factor makes it an invaluable component for the development of advanced communication systems. Its integration into the LNA not only improves the noise figure but also maintains a high gain, essential for robust signal amplification in 5G networks.

7.2 Future Scope

The work can also be extended in multiple dimensions, as listed below.

- Machine Learning algorithms can be employed to select the optimum combination of the geometrical dimensions and process parameters to realize, the highly miniaturized 5G and 6G RFICs exhibiting high performance for developing SOC and SIP systems.
- Develop these inductors on MEMS, and integrated passive device (IPD) technologies on various substrates such as glass, silicon, GaAs, GaN, etc.
- Extend the proposed methods to the design of on-chip transformers.

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List of Publications

List of Published Journals

1. Murali Banoth, and N. Bheema Rao, “Design of Novel High Q Multilayer Inductor for VCO Applications", Silicon, Volume 14, pp. 10115-10121, February 2022. **(Springer-SCIE Indexed)**
2. Murali Banoth, and N. Bheema Rao, “A Novel Coupled Pyramid Inductor for High Figure of Merit VCO Design for Telemetry and Transponder Applications", Scope, Volume 13, June 2023. **(Scopus Indexed)**
3. Murali Banoth, and N. Bheema Rao, “Design of Low Noise Figure LNA using a Novel Coupled Inductor", Scope, Volume 13, September 2023.**(Scopus Indexed)**

List of published/Accepted conferences

1. Murali Banoth, and N. Bheema Rao, “High Q Half-turn Split Inductor for RF Applications", in IEEE International Conference on Signal Processing and Integrated Networks **(SPIN-2018)**, Amity University, Noida, India, pp. 672-675, 2018.
2. Murali Banoth, and N. Bheema Rao, “A Novel Structure of on-chip Multilayered Half-Turn Inductor for RFApplications", in Intelligent Signal Processing and Effective Communication Technologies (INSPECT), **Under Review**, IIITM, Gwalior, India
3. Murali Banoth, and N. Bheema Rao, “High Performance Multilayer Series Coupled Inductor for RF Applications", in International Conference on Technological Innovations and Advance Computing (TIACOMP-24), **Under Review**, BALI, Indonesia.
4. Murali Banoth, and N. Bheema Rao, “Design of a low noise figure LNA using Multilayered Inductor for RF Applications", in VLSI Design and Test (VDAT-2024), **Under Review**, VIT Vellore, India.