IMPROVED HIGH GAIN DC-DC CONVERTERS FOR MICROGRID AND ELECTRIC VEHICLE APPLICATIONS

Submitted in the partial fulfillment of the requirements

for the award of the degree of

DOCTOR OF PHILOSOPHY

By

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APPROVAL SHEET

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CERTIFICATE

This is to certify that the thesis entitled **"Improved High Gain DC-DC Converters for Microgrid and Electric Vehicle Applications,"** which is being submitted by **Mr. Baba Fakruddin Monakanti** (Roll No. 719038), is a bonafide work submitted to the National Institute of Technology, Warangal in the partial fulfillment of the requirement for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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DECLARATION

This is to certify that the work presented in the thesis entitled "**Improved High Gain DC-DC Converters for Microgrid and Electric Vehicle Applications"** is a bonafide work done by me under the supervision of **Dr. A. V. Giridhar**, Department of Electrical Engineering, National Institute of Technology, Warangal, India and was not submitted elsewhere for the award of any degree.

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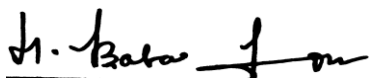

Baba Fakruddin Monakanti

ABSTRACT

KEYWORDS: Absolute common ground, Bidirectional dc-dc converter, Boost converter, High voltage gain, Interleaved converter, nonisolated dc-dc converter, Quadratic boost converter, Quasi Z Source converter, Switched Capacitor, Switched inductor, Split duty converter, Voltage lift, Voltage multiplier, Z Source converter.

The world-wide energy consumption raised by 34% with associated carbon dioxide gas emissions increased by 15% from 35.7 billion metric tons (bmt) to projected 41 bmt in 2050. These factors of increased energy consumption and CO_2 emission have attracted the alternate green energy sources with zero carbon emission regarding environmental protection concerns. The aforementioned micro sources are mostly at consumer premises and can be able to form dc microgrids. The merits of green energy micro sources are zero-emission, highly consistent, low cost and on the other hand major limitation of these sources is the low voltage at their output terminals. In order to comply with the applicability concerns power electronic-based power conditioning is required for these micro sources in terms of the low terminal dc voltage.

The amplification can be done by two types of power electronic converters i.e., isolated and nonisolated dc-dc converters. In isolated converters, the voltage transformation ratio depends on the magnetic coupling i.e., with transformer or coupled inductor technologies prime focus being on the turns ratio. These topologies are often in danger if their leakage flux is not properly processed. Moreover, this leakage flux also causes voltage spikes across the switch at the high-voltage side. The aforementioned constraints demand a peculiar design of magnetic components which in turn dictates the cost, density, efficiency, and scalability of the magnetically coupled dc-dc converters.

The nonisolated topologies i.e., non-magnetically coupled dc-dc converters are more in demand due to the absence of the aforementioned constraints. These nonisolated converters have inherent features such as simplicity in construction, compactness, efficiency, and low-cost concerns. The primitive classic boost converter is a simple solution but it has the adverse effects of drastically decreasing efficiency at extreme duty ratios at which it has to be operated to attain high and or ultra-high voltage gains. The later evaluated versions of boost converters like passive, active, and hybrid switched inductor converters, switched capacitor topologies, and voltage lift-voltage multiplier-based converters have major demerits such as high current stress, elevated component count, and reduced efficiency. Recent elegant interleaved integrated passive-switched-inductor topologies of common grounding with split duty and

reduction in long conducting intervals for switches are the viable alternate solutions for the aforementioned converters.

The interleaved split duty-based converters possess the feature of low duty for the switches but the overall cumulative duty cycle is still high with a relatively high element count and elevated output capacitor inrush currents at the end of each switching cycle. In addition, the overall elevated duty ratios make the efficiency of the converter to be less followed by the heating concerns. This typical concern demands the evolution of dc-dc converters consisting of high boosting factors at low duty ratios, such analogous featured converters are quadratic boost dc-dc converters. This converter features a high boost factor at a low duty which in turn lowers the voltage and current stresses, and improves the efficiency. Here much attention is required for the design of the second inductor because of its high voltage excitation and high sizing requirements.

The feature of high boost factor at low duty especially at lowered upper bound limit is also possible with impedance (L-C) network-based Z-Source converters that are highly volatile by having discontinuous input currents, this makes them less adoptable for majority applications. To overcome this demerit an analogous converter featuring similar voltage gain and more importantly, a series inductor at the input terminals is reported namely by a Quasi Z Source dc-dc converter, nevertheless because of the low charging interval for the inductors due to their limited upper bound on duty cycle makes the inductors to be bulky and henceforth associated packaging concerns, economical and spacing concerns will persist. In this regard, a single switched inductor modified Sheppard Taylor-based converter is proposed which surpasses the high inductor size and packaging concerns.

The recent evolution of dc-dc converters is also abundantly emphasizing the bidirectional dc-dc converters (BDC) for hybrid energy source-based electric vehicle propulsion systems. Among the plethora of BDC's quadratic boost-buck converters are popular because of their paramount amplification and attenuation consisting of a wide range of duty ratio flexibility, featuring simple topological synthesis and economical concerns towards the stated applications.

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Abbreviations

AC	Alternating Current
ASC	Active switched Capacitor
ASL	Active switched inductor
BDC	Bidirectional DC-DC converter
C	Capacitors
CCM	Continuous conduction mode
CG	Common ground
CIC	Continuous input current
CSG	Common switch grounding
DC	Direct Current
DCM	Discontinuous conduction mode
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
EI	Effectiveness index
EMI	Electromagnetic interference
ESD	Energy store devices
ESR	Equivalent series resistance
EV	Electric vehicle
FC	Fuel cell
FPGA	Field Programmable Gate Array
HES	Hybrid energy source
HGQB	High gain quadratic boost
HSL	Hybrid switched inductor
IB	Interleaved boost
KVL	Kirchhoff's voltage law

L	Inductors
NDVS	Normalised diode voltage stress
NMP	Non-minimum phase
NSVS	Normalised switch voltage stress
NTVS	Normalised total voltage stress
PCB	Printed circuit board
PI	Proportional-integral
PV	Photovoltaic
PWM	Pulse width modulation
QBDC	Quadratic buck-boost bidirectional DC-DC converter
QZS	Quasi Z-source
RHS	Right hand side
RMS	Root mean square
S	Switches
SB	Single boost
SC	Switched capacitor
SL	Switched inductor
SSM	Small signal modelling
VG	Voltage gain
VTR	Voltage transfer ratio
VS	Voltage stress
UPS	Uninterrupted power supplies
UVG	Ultra voltage gain
VMC	Voltage multiplier cell
ZS	Z-source

List of Symbols

A	Ampere
D	Duty ratio
dB	Decibels
deg	Degrees
f_S	Switching frequency
G	Voltage gain
I_C	Capacitor current
I_D	Diode current
I_{in}	Input current
I_L	Inductor current
I_O	Load current
I_S	Switch current
K_P	Proportional coefficient
K_I	Integral coefficient
R_0	Load resistance
rad	Radians
r_C	Equivalent series resistance of capacitor
r_d	On-state resistance of diode
r_s	On-state resistance of MOSFET
r_L	RL Series resistance of inductor
$Sec.$	Seconds
s	Laplace representation
t	time
T	Switching time
V	Volt
V_C	Capacitor voltage
V_D	Voltage across diode
V_{in}	Input voltage
V_L	Inductor voltage
V_O	Output voltage
V_S	Voltage across switch
W	Watt
X	Average state variable

$\hat{x}$	Small-signal variable
τ_L	Inductor time constant
Δi	Current ripple
Δv	Voltage ripple

Superscript:

^	Small-signal variable representation
^{o}	Degrees

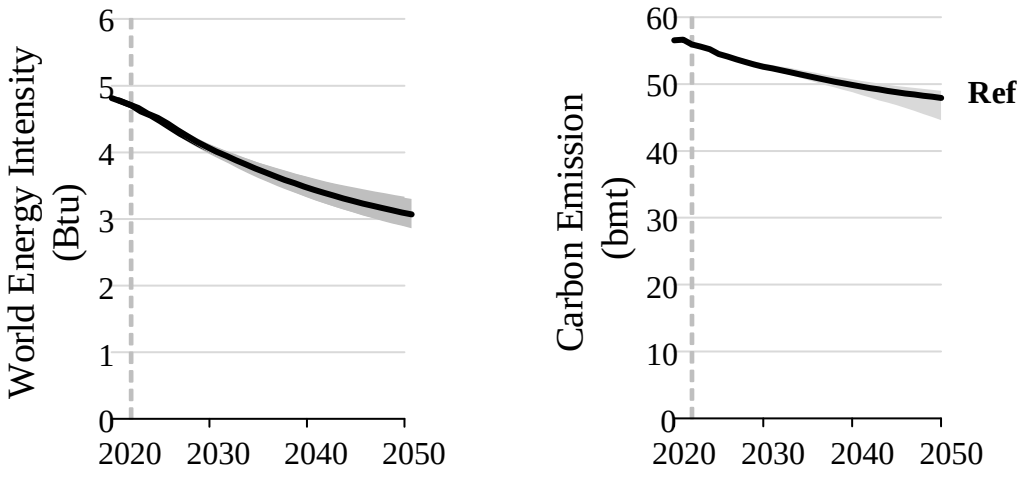
Chapter 1

Introduction

1. Introduction

1.1 Background

Reducing energy and carbon intensity have a neutralizing effect on emissions due to rising wealth and population. Global energy consumption and emissions in the future will follow a trajectory that is set by intricate relationships that occur throughout time, across sectors, and across geographies [1]. In the Reference scenario, the world's energy consumption rises by 34% from 638 quadrillion British thermal units (Btu-quads) in 2022 to 855 quads in 2050; in the worst-case scenario, the figure fluctuates between 739 and 999 quads by 2050 as shown in Figure 1.1. Emissions of CO_2 linked to energy in the Reference scenario increase by 15% from 35.7 bmt in 2022 to 41.0 bmts; in the other instances, the amounts vary from 35.1 bmts (a reduction from 2022 levels) to 47.9 bmts by 2050. Figure 1 presents the predicted projections as a dependent of two major factors: energy intensity (energy per dollar GDP), and carbon intensity (CO_2 emissions per unit of primary energy). This helps to understand the dymamics reflecting world wide energy consumption and its related $C0_2$ emission.

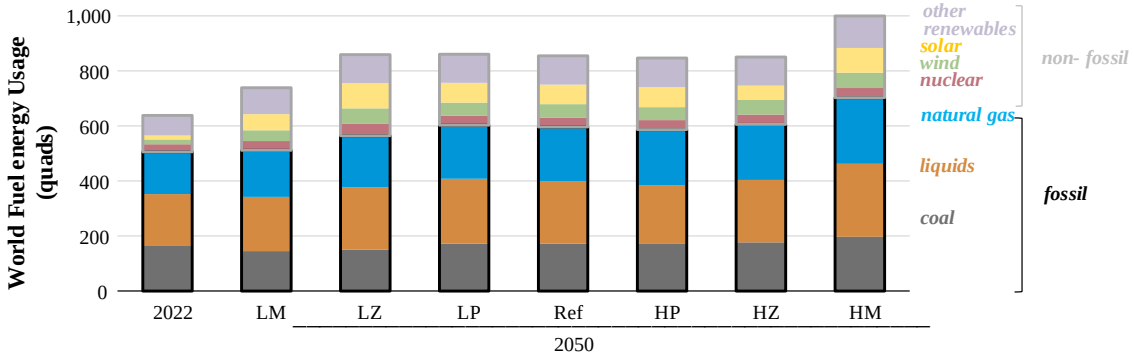


Data source: U.S. Energy Information Administration, *International Energy Outlook 2023* (IEO2023)

Figure 1.1 World wide energy consumption and CO_2 emission.

Population increase and GDP have a variety of effects on energy use. First, as GDP per capita rises, economic activity is dispersed throughout sectors. Richer customers gravitate towards energy-intensive goods and services as family incomes grow. Since different sectors have different energy intensities, this reallocation usually results in a higher overall energy consumption. Second, advancements in energy efficiency and technology frequently coincide with economic expansion. As energy efficiency increases, less energy is used for each unit of output. Third, changes in the population have an impact on the economy and it is a major factor in the overall amount of energy consumed. The succeeding discussion would be on fossil and non-fossil fuel utilization, indices of transportation, worldwide total installed energy and their impact on sustainable energy outreach.

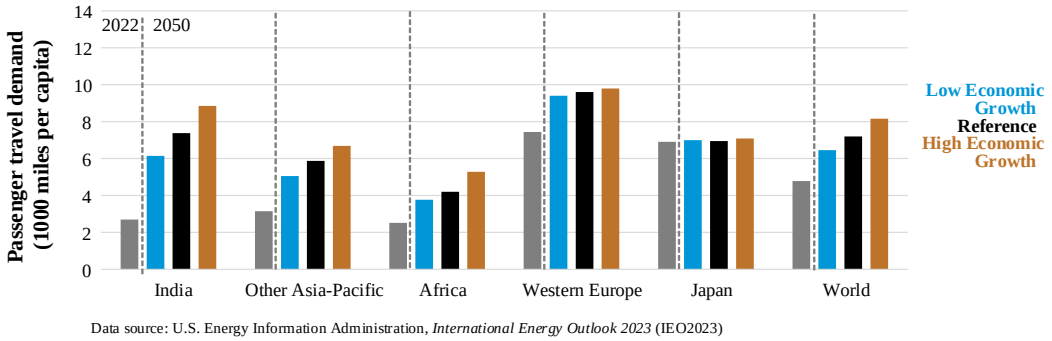
Ranging from 166 quads in 2020, the world's coal utilization rises in certain scenarios and falls in others. The scenario with the highest economic growth (19%) has the biggest increase in coal consumption from 2022 to 2050, whereas the case with the lowest economic growth (13%) has the largest decline as shown in Figure 1.2. Natural gas is the fossil fuel with the highest rate of growth in the world. By 2050, consumption of natural gas will have increased by 11% to 57%, from 2022-153 quads to 170-241 quads range. The consumption of renewable energy, specifically wind and solar power, is increasing at a higher rate than the remaining sources. In all scenarios, the non-fossil fuel portion of primary energy increases from 21%-2022 to a 29%-34% range in 2050. The growing usage of renewable energy for the production of electricity is the main factor driving the anticipated growth in its consumption.



Data source: U.S. Energy Information Administration, *International Energy Outlook 2023* (IEO2023)
Note: Biofuels are included in the "other renewables" category. Quads=quadrillion British thermal units; HZ=High Zero-Carbon Technology Cost case; LZ=Low Zero-Carbon Technology Cost case; HM=High Economic Growth case; LM=Low Economic Growth case; HP=High Oil Price case; LP=Low Oil Price case; Ref=Reference case.

Figure 1.2 Source based Energy usage in the world.

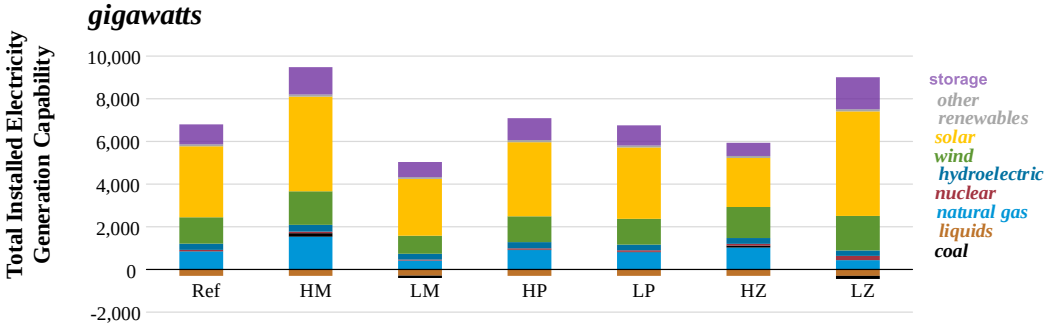
Travel demand growth, regional differences in electrification, and a sluggish fleet turnover rate causes the transportation sector's carbon emissions to rise. Global transportation energy consumption is driven by rising demand for both passenger and freight travel, and is expected to rise by 8% to 41% in various scenarios between 2022 and 2050 as presented in Figure 1.3. The need for travel is fueled by steady population growth as well as increased wages, employment, and industrial output. Between 2022 and 2050, there will be a 64%–108% increase in the demand for passenger transport, measured by passenger miles traveled. This increase will mostly be caused by rising income and population levels. This rise is consistent with an increase in the number of travelers as well as the average distance traveled by each individual. Approximately one-third of the anticipated rise in the demand for passenger travel between 2022 and 2050 can be attributed to the growing global population.



Data source: U.S. Energy Information Administration, *International Energy Outlook 2023* (IEO2023)

Figure 1.3 Travel demand of passengers.

The worldwide change in total installed generating capacity of electricity is reported in Figure 1.4, from which it is evident that the total rise in solar installation across the globe is over powering all other forms of electricity generation.



Data source: U.S. Energy Information Administration, *International Energy Outlook 2023* (IEO2023)
Note: Ref=Reference; HM=High Economic Growth; LM=Low Economic Growth; HP=High Oil Price; LP=Low Oil Price; HZ=High Zero-Carbon Technology Cost; LZ=Low Zero-Carbon Technology Cost.

Figure 1.4 Global total installed generating capacity.

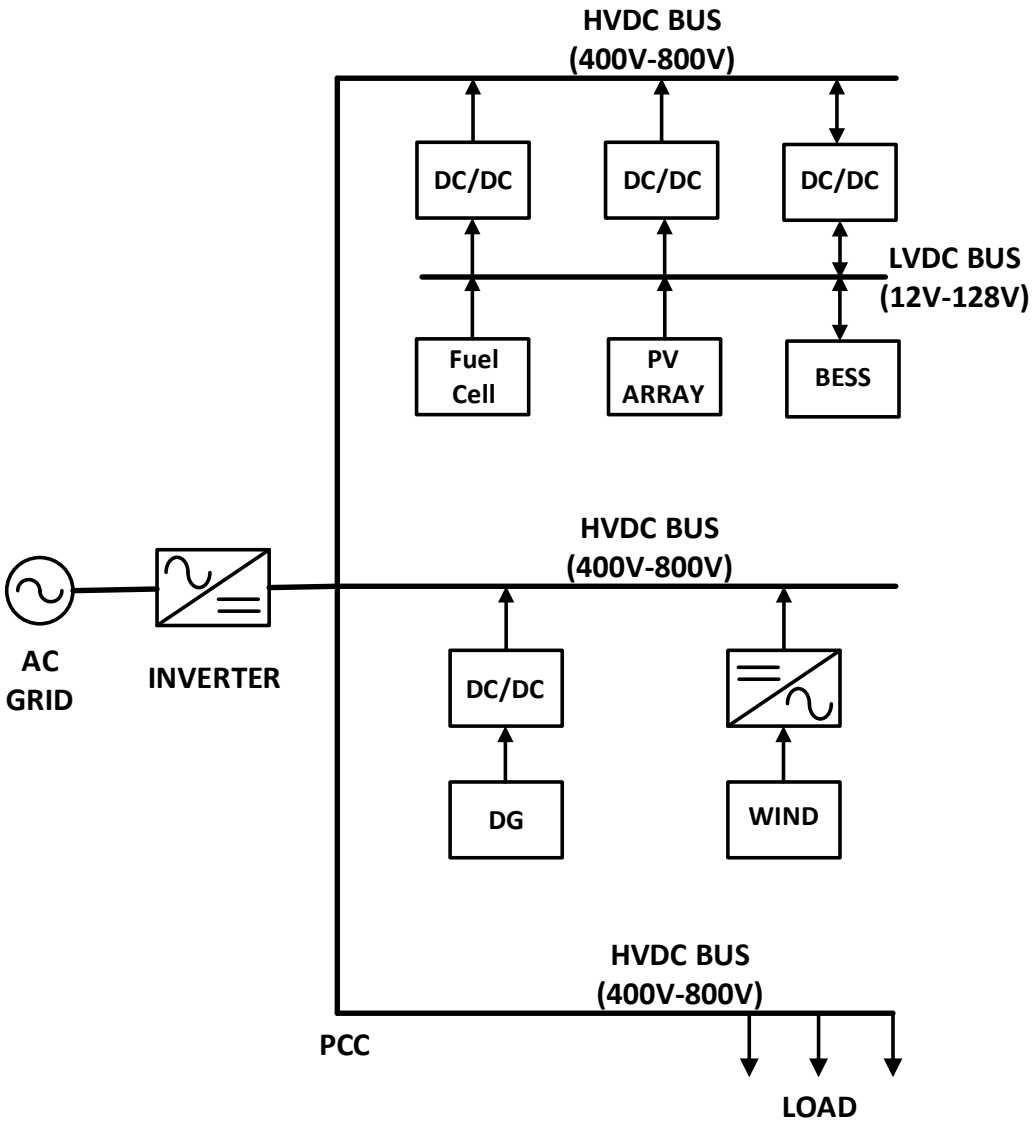


Figure 1.5 General architecture of DC microgrid

The conclusive remarks from the aforementioned discussion are that the conventional fossil fuel cells are depleting at faster rate because of the increased demand for the electrical energy consumption and this in turn causing greater amount of $C0_2$ emission into the atmosphere. The depletion of conventional energy resources led to the development and penetration of green energy micro sources into the energy sector. These micro sources are mostly at consumer premises and can be able to form DC micro grid [2] as shown in Figure 1.5. The aforementioned micro sources also known as green energy sources include photovoltaic cells, a stack of fuel cells, battery energy management systems, etc. The merits of green energy sources are low emission, highly consistent, low cost and on the other hand, the major limitation of these sources is the low voltage at their output terminals. The terminal voltage range of green energy sources is typically 12-48 V, therefore to be compatible with DC microgrid efficient power electronic interface i.e., DC-DC voltage step-up converters are

needed [3]-[6]. The general voltage of green energy micro sources is in the aforementioned range (12 V to 48 V), in some exceptional cases it would be 128 V, where it is necessary to form a low voltage DC bus. Later, this low DC bus voltage must be stepped up in the range of 400 V to 800 V by DC-DC converters to comply with the requirements DC microgrid. In addition to the previously mentioned DC microgrid application, DC-DC converters are used in other industries including telecommunication, stand-alone UPS systems, bulk data centre power management, on-road lighting in the automotive industry, and power conditioning in medical equipment.

The precise applications of the nonisolated dc-dc converter topologies in terms of power rating, input, and voltage rating are as reported in Table 1.1 and as shown in Figure 1.6.

Table 1.1 Precise applications of nonisolated dc-dc converters in terms of power rating, input and output voltages

Application	Power rating (W)	Input voltage (V)	output voltage (V)
Street Lightning	< 200	<20	<100
Auto Mobile Headlight	< 200	<20	<100
LED Lighting	< 100	<20	<100
Wireless power transfer	< 200	<20	<100

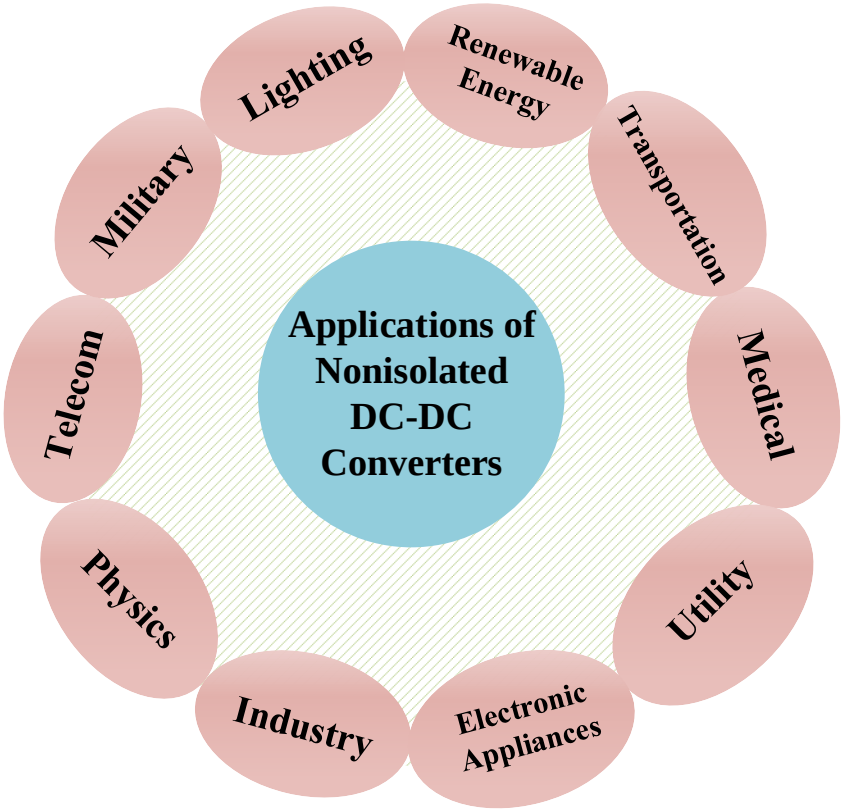


Figure 1.6 Overview of nonisolated dc-dc converters applications.

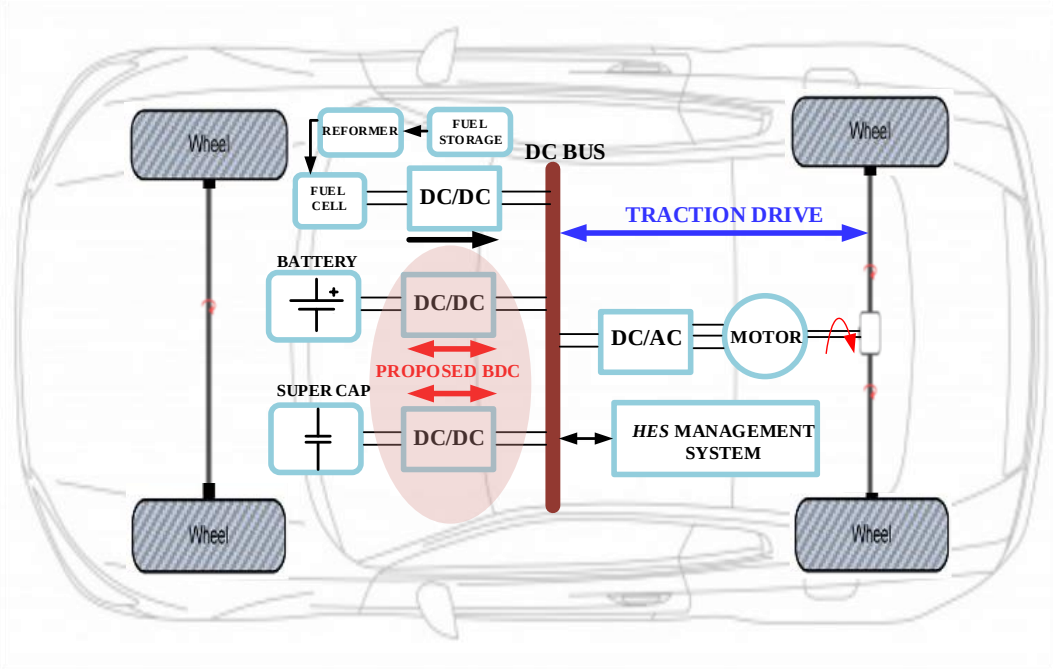


Figure 1.7 Power architecture of HES driven EV.

Decarbonization is gaining a lot of attention due to the rapid acceleration of problems associated with global warming. The decarbonization measures are pushing the governments and private sectors to lower the consumption rate of fossil fuels and at the same time to increase investment in electric vehicles (EV) [7]. EV power architecture with HES source is as shown in Figure 1.7. The rapid penetration of energy store devices (ESDs) or hybrid energy sources (HES) in the sustainable and renewable energy sector is widely recognized in [8], [9]. The interface between HES and dc-link of the inverter [10], [11] is a major challenge in EVs. The HES along with super capacitors are used to power the propulsion system in EV during accelerating periods and to be powered (store energy) in regenerative braking. The super capacitors operate at a very lower voltage compared with the dc-link of the inverter and moreover, they may persist a wide range of voltage swings depending on their state of charge [12],[13]. The problem of mismatching voltage levels between HES along with supercapacitors and dc-link of inverters is solved by the bidirectional dc-dc converter (BDC). The wide voltage gain range is an eminent feature that the BDC should possess to operate under the fluctuation of voltage levels in HES.

1.2 Motivation

The amplification of voltage can be done with two types of converters i.e., isolated and nonisolated. Numerous technologies have been established in the literature depending on the requirements of voltage transfer ratio (VTR) and isolation. The higher VTR is achieved through magnetic coupling i.e., with transformer or coupled inductor technologies. These topologies are often in danger of overshoot voltages across power switches if their leakage flux is not properly processed. Different methods of recycling the leakage flux i.e., usage of snubber circuits to divert it or actively clamping the leakage flux are reported. Moreover, this leakage flux also causes voltage spikes across the switch at HV (secondary) side. The aforementioned concerns demand customized design of magnetic or coupling components which in turn dictate the cost, density, efficiency, and scalability of these isolated topologies. Nevertheless, these magnetic coupled converters are often prone to pulsating current at input terminals which makes them unsuitable to PV applications because it reduces the life of PV array. The nonisolated topologies i.e., without magnetic coupling is of more demand due to the non-existence of aforementioned issues. Moreover, these non-isolated topologies are simple in architecture, compact, efficient, and economical.

However, the nonisolated topologies has the following drawbacks such as low voltage gain by the classic boost converters; high current stress of passive switched inductor and switched capacitor topologies; increased component count, and reduced efficiency in voltage multipliers and voltage lift techniques-based converters. Recent elegant switched inductor topologies with split duty and reduction in long conducting duty cycles for switches are the viable solutions for the aforesaid concerns. The absence of common ground makes these type converters unfit for most renewable energy-based applications. The inter leaved converter with the integration of passive switched inductor (PSL), common switch grounding and split duty technique will over come the stated short falls.

The split duty converters are capable of providing high boost factor with possible low voltage stress on the semiconductor elements but still the overall duty ratio quantitatively remains high. This high duty causes the low charging time for the output capacitor and hence huge inrush currents in each switching interval. In addition, elevated duty ratios make the overall efficiency of the converter to be less followed heating concerns of the converters. This peculiar concerns demands the evolution of dc-dc converters consisting of high boost factor at low duty ratios. One such analogous featured converter is a quadratic boost converter. Because of its quadratic nature high VTR is possible at low duty which in turn lowers the voltage and current stresses, and improves the efficiency. Here much attention is required for the second inductor because of its high voltages and high sizing requirements.

The aforementioned concerns of high element voltage stress and low efficiency due to elevated duty ratios are prevailed by low duty operated converters. One such type of converter is the impedance source or Z source converter (ZSC). Here an impedance (L-C) network is employed between the dc source and converter or inverter for dc-ac and ac-dc power conversion. To enhance ZSC voltage gain further three topologies i.e., single, and double Quasi-Z-source (QZS) integrated, and QZS embedded Z-source dc-dc converters are popular in recent trends. Nevertheless, these ZSC and QZS converters comes at a cost of two inductors in the topology therefore demanding high sizing requirements and lowering the packaging concerns of the converters. In this regard a single switched inductor analogous QZS based on modified sheppard Taylor converter surpasses the high inductor count and packaging concerns.

The recent evolution of dc-dc converters is also abundantly emphasizing on the bidirectional dc-dc converters (BDC). These BDC's finds their suitability in HES driven electric propulsion systems and dc micro grids. Among all the BDC's quadratic boost-buck converters are popular because of their extreme amplification and attenuation with wide duty flexibility. These converters are simple in construction and economical to meet their concerned applicability.

1.3 Thesis objectives

The thesis aims to adopt simple, economical, and effective nonisolated unidirectional and bidirectional power flow dc-dc converters with superior steady-state and control performance. The following are the enlisted objectives of this thesis.

i. The cumulative benefits of interleaving, switched inductor, split duty and common ground are possibly integrated into a single converter by means of common switch grounding and thus improving the voltage profile of the inductors especially in split duty interval. Thereby, attaining the objective of high VTR with distributed conducting intervals among the switches.
ii. The quadratic boost converters inherently possess the feature of moderate VTR with possible low duty at the expense of elevated voltage burden for the second inductor. Therefore, VTR enhancing methodologies especially diode-capacitor voltage lift arrangement brings the significant improvements in lowering the duty ratio, voltage-current stresses and improving the converter efficiency.
iii. The single stage quadratic boost-busk BDC's significantly reduces the overall element count making them most suitable for bidirectional power flow applications in dc micro grids and EV's. One additional possible feature of this type of BDC is low semiconducting element in the forward path. However, the VTR attained is still not adequate by these

topologies.

iv. Implementation of low duty based QZS analogous converters preferably with single ended primary inductor by alleviating the semiconductor voltage-current stresses and enhancing the operating efficiency. More importantly fast dynamic response is possible against the perturbations at source and load ends by retaining the aforesaid features with low settling time.

1.4 Organization of thesis

The collocate of this research work on the nonisolated dc-dc converters is presented below, along with a synopsis of the chapters' contents.

Chapter 1 briefly presents an overview of the background of the research work in terms of worldwide energy consumption, CO_2 emission, need of green energy micro sources and their power electronic based power conditioning converters. This chapter also emphasizes the motivation and objectives of the research work.

Chapter 2 provides a thorough analysis of the existing research on nonisolated non-coupled unidirectional and bidirectional power flow dc-dc converters. The merits and short falls along with topological derivation-synthesis are also emphasized in this chapter.

Chapter 3 presents the interleaved-switched inductor integrated split duty converter with common switch grounding. The inherent features of this converter are reduction in long conducting duty intervals for the switches there by improved thermal and reliability aspects are achieved.

Chapter 4 explains the operation of an active switched inductor- switched capacitor integrated diode-capacitor voltage lift aided quadratic boost dc-dc converters. The converters steady state operation and control formulation is simple and does not involve any complex analytical methodologies.

Chapter 5 addresses the limitation of capacitor-to-capacitor energy transfer and the importance low forward path conducting elements in quadratic boost converter. A simple rearrangement in the posture of rear end inductor and capacitor makes the converter to have only one element in the forward path there by improved terminal voltage. The topological synthesis based on flux balance and cascading of the sub converters is also presented in this chapter.

Chapter 6 describes an optimized low forward path element featured bidirectional quadratic boost-buck converter. The converter is capable of attaining extreme boosting and attenuating factors with simple and economical converter configuration having superior control

performance owing to its lower order.

Chapter 7 reports a low duty modified sheppard Taylor based Quasi Z Source analogous single ended primary inductor converter. This low duty makes the converter viable to operate with alleviated voltage-current stresses and losses, superior thermal aspects, and enhanced efficiency of the converter.

Chapter 8 enumerates the important conclusions drawn from the entire study as well as the future directions of the research.

1.5 Summary

This chapter briefs the research work carried out for the doctoral thesis. The motivation and objectives are formulated after the introduction of relevant literature pertaining to nonisolated unidirectional and bidirectional dc-dc converters. Furthermore, this chapter presents the organization of this thesis.

Chapter 2

Literature Review

2. Literature Review

2.1 Introduction

The semiconductor switches era between 1950s and 1960s accelerated the advancements of switched mode converters originally originated from pulse width modulated boost converter. A plethora of dc-dc converters are derived in recent trends among which nonisolated dc-dc converters are gaining attention because of their simplicity in topological synthesis and flexibility in control aspects. The current chapter emphasizes classification and in detail synthesis schemes of nonisolated dc-dc converters enlightening their respective merits, limitations, and crucial current research works in this domain. In addition, this chapter will also review the literature available on nonisolated dc-dc converters for dc microgrids and EVs. A discussion of the gaps found from the thorough literature study concludes the chapter.

2.2 Nonisolated Unidirectional High Voltage Gain DC-DC Converters

The previous chapter emphasizes that the green energy based micro sources (GEMS) are not suitable for any direct application because of their low terminal voltage. Hence these sources require power conditioning by incorporating power electronic converters. The four main types of power converters or power conversions used in dc micro grids and EVs applications are AC-DC, DC-DC, DC-AC, and AC-AC as shown in Figure 2.1. The main scope of this thesis is to enlight the topologic structures related to DC-DC converters. Henceforth, the other power conversion methodologies are not discussed because their viability is beyond the scope of this thesis.

As reported in Figure 2.1 the nonisolated dc-dc converters (NSDC) along with isolated dc-dc converters (IDC) belongs to voltage source-based converters. In isolated topologies to get the required voltage gain turns ratio of the transformer is increased. Numerous drawbacks in isolated converters are as follows; the leakage inductance in high frequency transformer causes voltage spikes in the active switches, increased voltage stress across output diode, lower efficiency especially when operated for higher gains [14], pulsating current at input terminals which makes them unsuitable to PV applications because it reduces the life of PV array [15]. Recent dual active bridge topologies are capable of achieving zero voltage switching by the integration of resonant converters at fixed or variable frequency modulation. Some of the aforementioned demerits in isolated topologies can be overcome by adopting rectifiers, voltage doublers-quadruplers at the secondary side and more over reverse power flow, circulating currents can also completely eliminated.

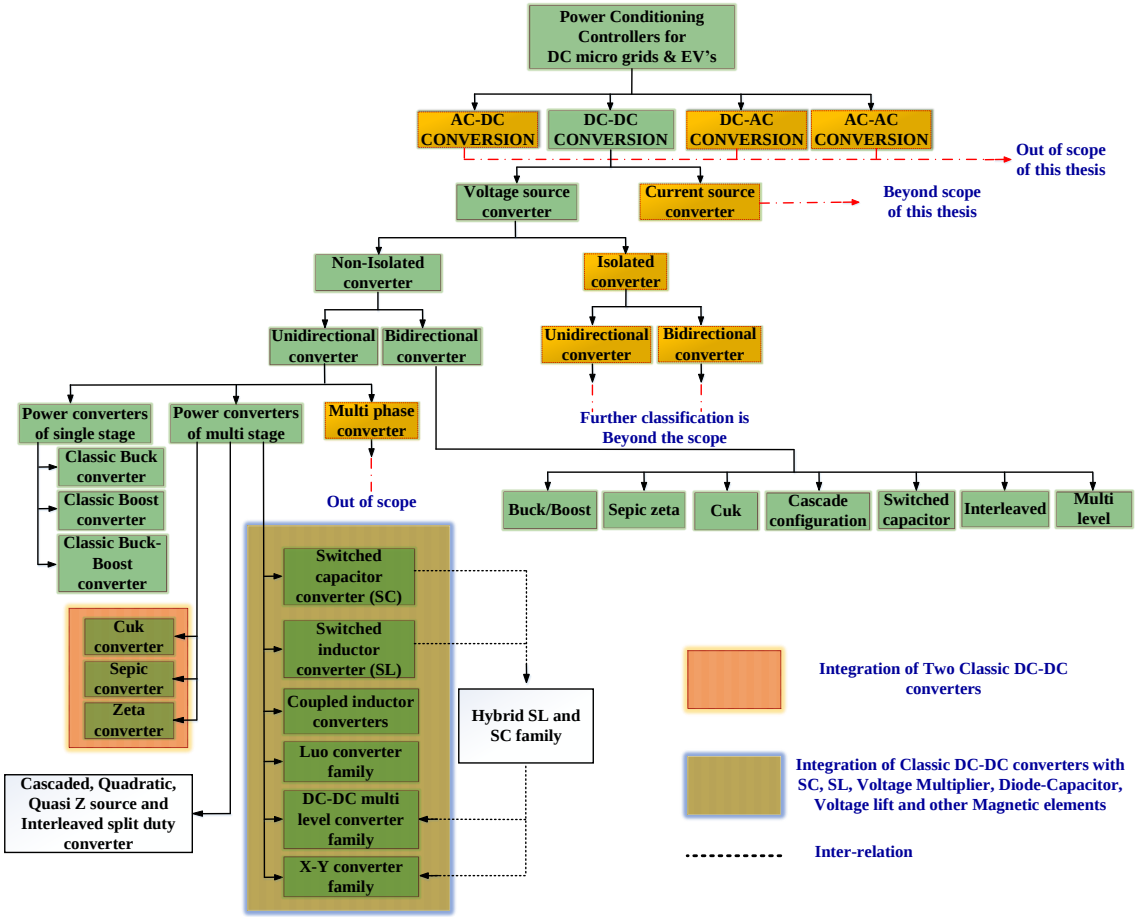


Figure 2.1 Classification of Power conditioning-power electronic converters emphasizing nonisolated DC-DC converters.

The origin for all modern era unidirectional NSDC converters is classic buck, boost, and buck-boost converters. Later in a second phase of evolution multistage i.e., cascaded-quadratic and another family involving switched-inductor (SL), switched-capacitor (SC), coupled inductor, Luo, multilevel dc-dc, and X-Y converters are developed. All these three categories are not discrete, in fact any of the aforesaid classification reflected in Figure 2.1 is not operated in independent nature. All these converters especially multistage power converters are integrated, cascaded and or merged to synthesize a particular converter i.e., hybrid switched-inductor and switched-capacitor based topologies depending upon the voltage amplification and applicability. Though the aforesaid classification deals with various types NSDC's it does not reflect any information regarding grounding aspects of input and output ports. Therefore, from this prospect of grounding the NSDC's are classified into common grounded where input and output ports share same ground, and floating type converters in which output port floats with respect to the source ground as shown in Figure 2.2 (a) and (b). The same kind of classification is also holds good for multistage converters as shown in Figure 2.2 (c) and (d).

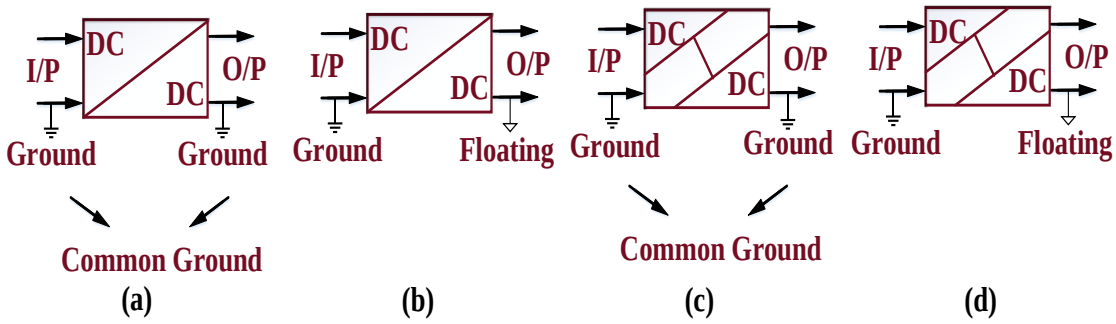
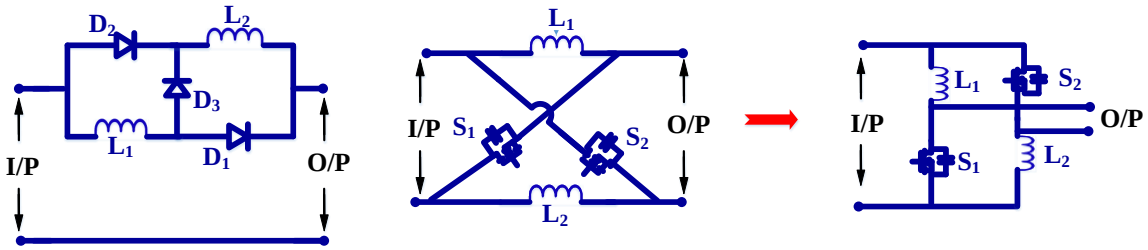


Figure 2.2 Non-Isolate Uni- Bidirectional DC-DC converter configuration focusing on grounding aspects (a) single stage common ground structure (b) single stage floating structure (c) multi stage common ground structure (d) multi stage floating structure

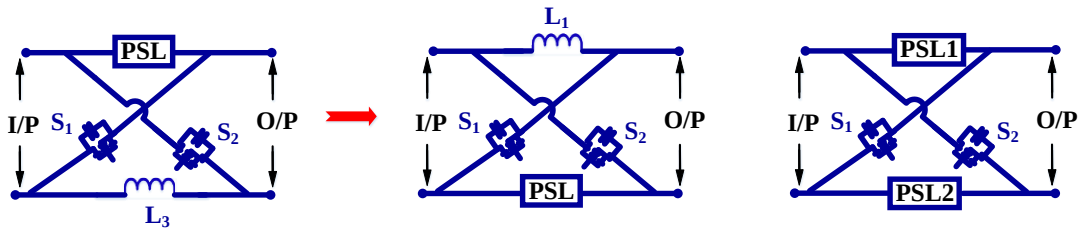
Since the micro sources are dispersed in nature, when all these micro sources are added to form a local dc micro grid, they are capable of providing low voltage and high current at the source terminals. So, classic boost converter is not a viable solution for this scenario to handle the high currents. A simple single stage passive switched inductor (PSL) altered boost converter as presented in Figure 2.3 (a) is reported in [16]. However, this converter has three major drawbacks; the ON (DT_s) state forward path contains three power devices, OFF ($(1-D)T_s$) state consists of two devices in forward path and more importantly the switch voltage stress equal to output voltage. This forward path elements can be reduced by the classic interleaved approach reported in [17], [18] and [19] where in which active switched-inductor cell (ASL) is used as shown in Figure 2.3 (b). This ASL cell alone independently consists of only one forward path element in switch OFF interval. The integration of ASL with PSL to form a hybrid switched-inductor (HSL) is also reported in [19] to attain higher voltage gains. However, except PSL all other stated switched-inductor topologies are lacking of common ground and more importantly the source current ripple content will be high. Though the asymmetric and symmetric structures of HSL as shown in Figure 2.3 (c) and (d) achieves enhanced voltage gains but it comes at the cost of higher element count.



(a) Passive Switched Inductor(PSL)

(b) Active Switched Inductor(ASL)

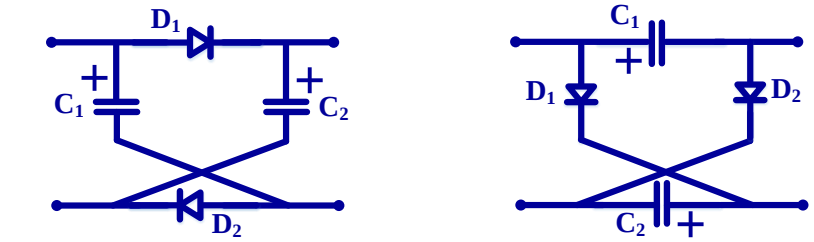
Interleaved



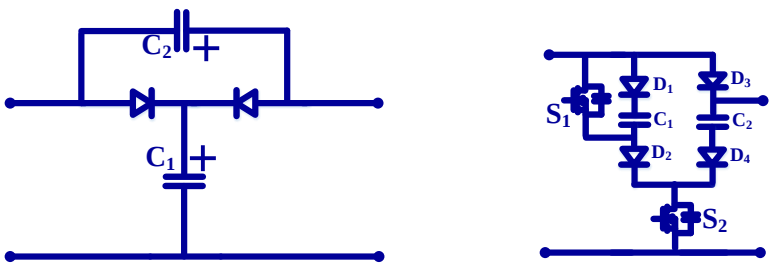
(c) Asymmetric Hybrid SL (HSL) **Asymmetric Hybrid SL (HSL)** **(d) Symmetric Hybrid SL (HSL)**

Figure 2.3 SL and SC based hybrid boost converters (a) PSL arrangement (b) ASL structure (c) asymmetric HSL and (d) symmetric HSL.

The former discussion emphasizes that after certain voltage gain it is not advisable to use switched-inductors because of their space requirements. Hence, it is advisable to adopt front end converter based on SL's and later SC voltage doublers or voltage multiplier cells can be used to further elevate the voltage gain. These structures are presented in Figure 2.3 (e)-(h); in which voltage doublers for non-inverting and inverting output is reported in Figure 2.3 (e) and (f), a voltage multiplier cell is presented in Figure 2.3 (g) and (h) representing the modified switched-capacitor arrangement. Despite their ability to enhance the volage, these structures are often prone to capacitor-to-capacitor energy transfer which causes high inrush currents at the starting of each switching interval.



(e) Voltage doubler for non-inverting output **(f) Voltage doubler for Inverting output**



(g) Voltage multiplier with capacitors **(h) Switched capacitor arrangement**

Figure 2.3 (contd.) Capacitor based voltage boosting arrangements; voltage doublers for (e) noninverting output (f) inverting output (g) voltage multiplier and (h) switched capacitor (SC)

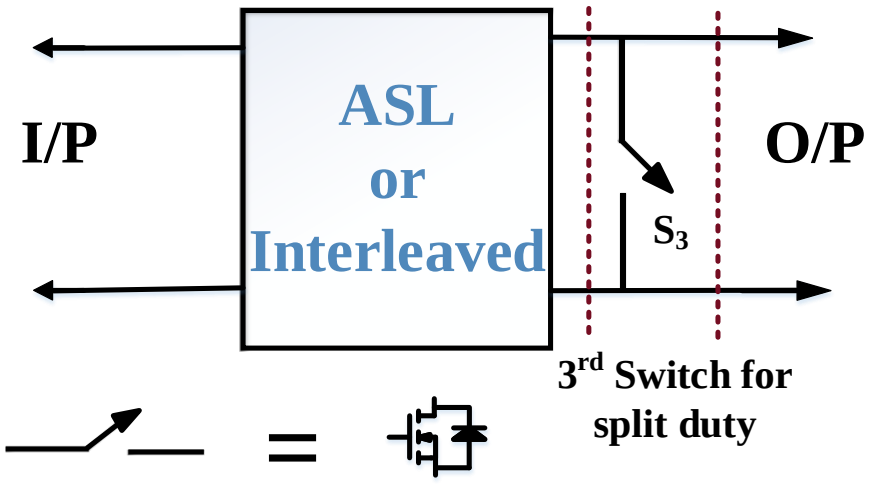


Figure 2.3 (contd.) ASL or interleaved structure based (i) split duty converter.

A plethora of one-to-one combinations with SL's and SC's can be formed to formulate any dc-dc converter. The systematic summarization of these combinations exclusively with SL's is presented in Figure 2.4. The usage of PSL, ASL, HSL, and interleaving structures to attain high voltage gains is often accompanied by elevated switching intervals and duty ratios. To overcome this limitation, splitting of duty cycle from D to D_1 and D_2 is made possible with an additional switch (S_3) as shown in Figure 2.3 (i). Therefore, this arrangement can attain high voltage gain with split duty and reduced conduction intervals for switches. On the contrary this arrangement is having high switch count and lack of common ground which makes it unsuitable for majority applications.

As the previous literature conclusively emphasizes numerous voltage boosting techniques [20]-[29] such as SL, SC, SL-SC, VMC, charge pump, voltage lifting, multistage-multilevel structure, interleaving and split duty converters. The stated methodologies can be combined or overlapped to form a particular step-up converter. Nevertheless, a PWM boost converter [30] with concise integration of stated boosting methodologies and with other features in demonstrated in Figure 2.4. The Figure 2.4 also illustrates the various topologies proposed in this doctoral thesis. The primary structures between the source and switch or DC-link capacitor resembles first stage of voltage boosting. The second stage involves either intermediate-inductor or VMC for floating output or SL, SC, SL-SC, VMC, Charge pump which are powered by VMC and or diode-capacitor cell stacked above the source as shown in Figure 2.4. This second stage can be repeated for successful formation of n^{th} stage cascading and or multistage NIDC's. After the second stage a switch or diode is used to comply for unidirectional and bidirectional power flow applicability. The output voltage filtering consists of single, modular and multilevel capacitor structure depending on the preceding converter

structure. At the end the output consists of three major categories i.e., non-inverted voltage, inverted voltage, and quantitative input voltage for bidirectional dc-dc converters.

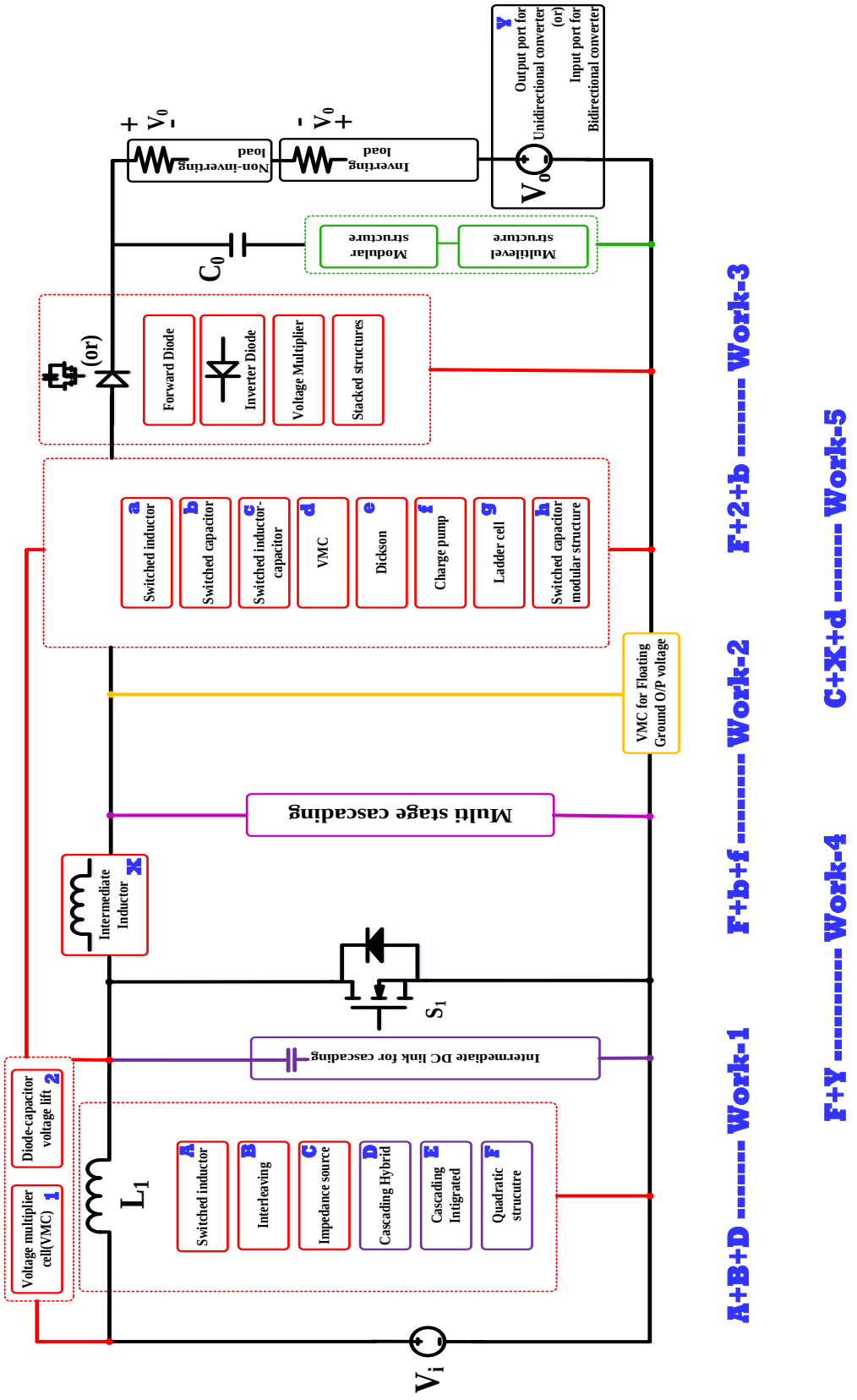


Figure 2.4 Nonisolated high Gain DC-DC converters power conditioning structures and voltage enhancing methodologies applied to boost converters.

2.3 Nonisolated Unidirectional Quadratic Boost DC-DC Converters

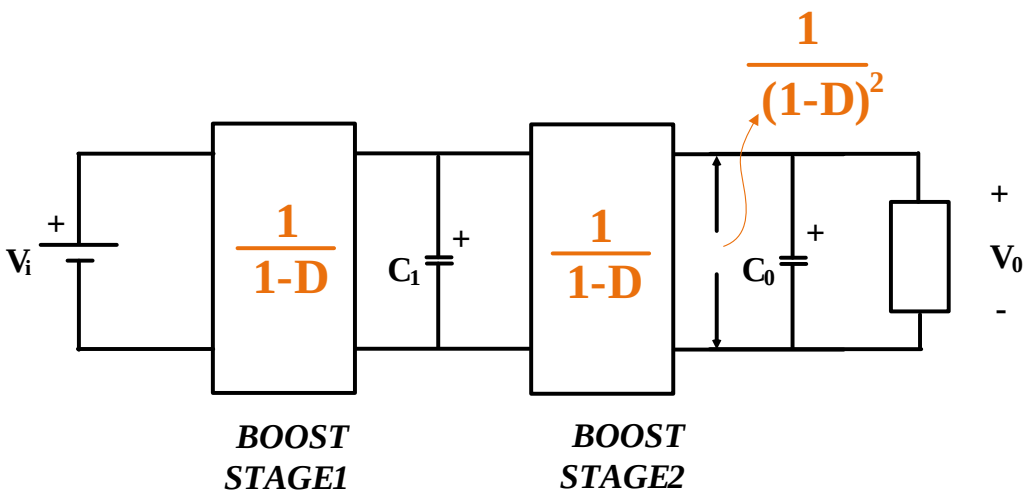


Figure 2.5 Two stage Quadratic boost converter.

Fundamentally quadratic boost converter is cascading of two classic boost converters in which the first stage output is used as an input to the second stage via an intermediate DC-link capacitor between the two stages as shown in Figure 2.5. However, the overall efficiency of the cascading section is low. Therefore, literature has been continuing in the direction of integration and or possible overlap as presented in Figure 2.6 with front end and rear end cascaded boost converters consisting of only one switch. However, here the voltage stress on intermediate capacitor is high. To overcome this concern a simple quadratic structure derived from PSL is reported in Figure 2.7. Though this structure comes with a merit of low intermediate capacitor voltage stress but the source current ripple will be high because of their interleaving nature in the switch ON period.

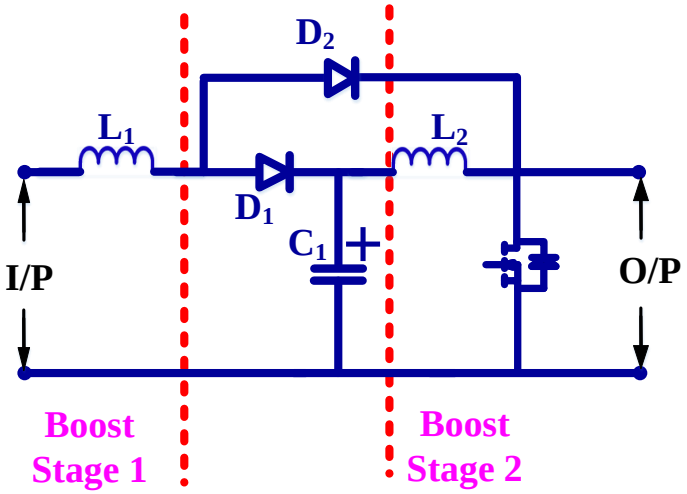


Figure 2.6 Single stage Quadratic boost converter.

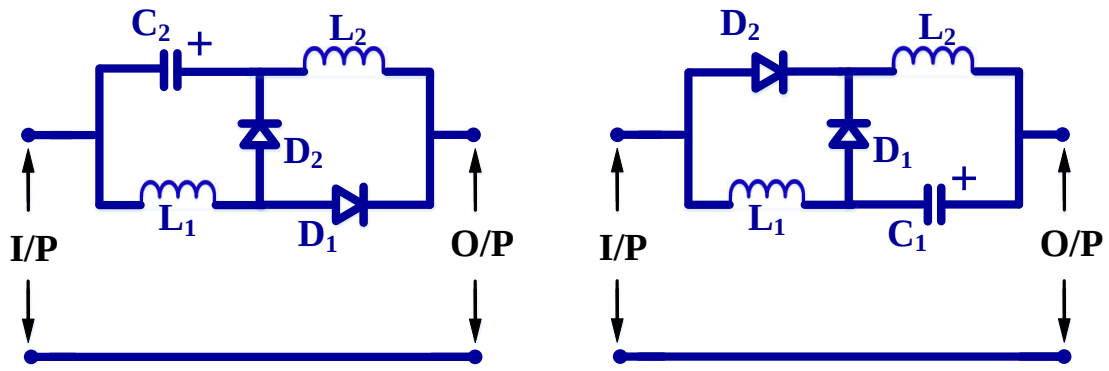


Figure 2.7 Quadratic boost structures derived from PSL.

The switched capacitor arrangement is used for voltage lifting purposes in most of the conventional nonisolated DC-DC converters. The converter in [31] uses switched capacitor arrangement as a voltage lift mechanism added to active switched inductor, however, the voltage gain attained is not quite high. To overcome this short fall of low voltage gain, a multistage switched inductor arrangement integrated with the switched capacitor is proposed in [32] but here the component count is high. The posture of capacitor-diode (C_2-D_2) arrangement in converter [33] is exclusively used for voltage lifting. However, this posture of the capacitor-diode can be altered as the arrangement (C_2-D_2, C_3-D_3) in the proposed converters to combine the positive features of regenerative energization for one of the inductor and voltage lifting. One of the simple and efficient ways to enhance the voltage step-up conversion ratio with the optimized component count is to use this switched capacitor arrangement as an energizing (regenerative from the front-end inductor) element to the rear-end inductor. Thereby the voltage gain is improved with simple and efficient converter construction.

The aforementioned discussion on numerous techniques to attain ample amplification of input voltage in DC-DC converters has some constraints like; extreme duty ratio, probable failure of switches due to voltage spikes, high voltage-current stress, and bulky in nature etc., except the approach of rear-end inductor energization by the active switched capacitor arrangement. In order to have the merits of low duty ratio, simple construction, ease of operation and low voltage-current stress quadratic boost configuration with an integrated active switched capacitor arrangement would be one of the feasible solutions.

A plethora of high step-up nonisolated dc-dc converter have been presented in [34] in regard to attaining high voltage gain, power electronic interface to the grid, and micro source applications. Despite having duty ratio flexibility of wide range and high amplification, nonisolated converters have elevated switching intervals, which results in high switching losses and poor efficiency. The coupled inductors are often integrated to the nonisolated converters in which by adjusting the turns ratio high voltage gains are achieved. The flux

leakage paths other than the core in the coupled inductor cause leakage inductance and the effect of this leakage inductance in terms of static voltage gain is loss of duty ratio.

The nonisolated dc-dc converters having high voltage conversion ratio at low duty cycles, low input current ripple and are free from coupled inductors is the promising solution for the aforementioned constraints. A three-switching state split duty nonisolated dc-dc converter is proposed in [35]. Here, one additional switch is used to avoid long conducting intervals for the interleaved switches but still the output capacitor has to support the load voltage profile for longer intervals. The converters in [36], [37] suggested an alternate approach to have high dc static gain at a low duty ratio. The inductor charging profile in [36] is improved with the aid of a dc source and capacitor (C_1) but the problems of high source current ripple and absence of common ground persist in the stated converter. The elevated ripple content can be reduced by having an inductor as stated in [37] at the input port. Though at low duty ratio the topology in [37] has improved voltage conversion ratio with moderate component count but the peak switch current stress is substantially higher.

The passive and active switched inductors (P-SL and A-SL) are integrated into a single converter [19] to form a hybrid switched inductor (HSL). Here symmetrical and asymmetrical HSL configurations are reported to attain high voltage gain. The converter stated in [38] used HSL arrangement with tri-switching states to enhance the voltage gain and also to avoid extended duty intervals for the switches. The above stated two converters are having high component count and the number of devices acting in the forward path is significantly high. A Zeta derived converters with and without output inversion are proposed in [39]. Although these converters acquire significant voltage gain, the problem of discontinuity in the input current persists. In recent trends [40]-[43], modified SEPIC converters or integration of SEPIC converters to the existing dc-dc converters is gaining attraction with improved voltage gain and other performance indices. The converter in [40] used a capacitor (C_M) which is in the previous state charged by a boost converter to power the second inductor. Similar to the previous case, the converter in [41] is proposed but here the only difference is instead of a boost converter at the primary end an active switched-interleaved dc-dc converter is used. The converter in [40] has low voltage gain than that of the converter in [41], although it is having enhanced voltage gain lack of common ground for source and load terminals overpowers all its merits. The improved SEPIC converters with diode-capacitor voltage lift arrangement [42] and with quadratic voltage gain are reported in and [43]. The converter in [43] synthesized by integrating SEPIC and conventional PSL arrangement at front end to obtain quadratic voltage gain. The converter in [42] attains a noticeable voltage gain but it has high elements and the

topology in [43] has a dc static gain of $\left(d/(1-d)^2\right)$, with a high inductor count which makes the power density to be low.

The switched-capacitor arrangement integrated to fundamental dc-dc converters is also prominent in nonisolated converters. A wide variety of these kinds of converters with inductor count at two are reported in [16],[44]. The switched-capacitor arrangement in the form of a voltage multiplier or voltage doubler integrated to a single or multi-inductor arrangement is proposed in [45]. Here a wide variety of converters with enhanced voltage gain are reported at the elevated component count. A switched-capacitor-integrated-inverted output dc-dc converter is stated in [46] with an output voltage profile near to a quadratic boost converter. But here the first inductor voltage is not transferred to the output side.

The aforementioned discussion emphasizes that high dc static gain at moderate duty ratio as well as with low component count is only realizable with a quadratic boost converter. A switched-capacitor-based quadratic boost arrangement is proposed in [47] by strengthening the inductor L_2 charging profile. Since the inductor L_1 voltage of the converter in [47] is not transferred to output side the voltage gain attained is low. A voltage multiplier cell (VMC) integrated two-stage converter is stated in [48], where the step-up gain has been improved with the aid of coupled inductors. Despite the enhanced voltage gain and quadratic action of the stated converter, the component count is high which overpowers its other positive features. A ladder type VMC based active switched-inductor quadratic boost converter with low duty ratio and elevated voltage transfer ratios is presented in [49]. The shortfalls of the converter in [49] are high switch count and the absence of common ground.

2.4 Nonisolated Bidirectional Quadratic Boost DC-DC Converters (BDC)

The wide voltage gain range is a foremost eminent feature that the BDC should possess to operate under the fluctuation of voltage levels in HES [50]. Numerous BDC technologies have been established in the literature depending on the requirements of VTR and isolation. The higher VTR is achieved through magnetic coupling i.e., with transformer or coupled inductor technologies. These topologies are often in danger of overshoot voltages across power switches if their leakage flux is not properly processed. Different methods of recycling the leakage flux i.e., usage of snubber circuits to divert it or actively clamping the leakage flux are reported in [51]-[53] and [23]. Moreover, this leakage flux also causes voltage spikes across the switch at HV (secondary) side. The aforementioned concerns demand customized design of magnetic or coupling components which in turn dictate the cost, density, efficiency, and scalability of these

BDC topologies. The nonisolated topologies i.e., the BDC without magnetic coupling is of more demand due to the non-existence of aforementioned issues. Moreover, these non-isolated BDCs are simple in architecture, compact, efficient, and economical.

In literature, numerous nonisolated BDCs are reported namely buck-boost [54], inter-leaved [55], switched capacitor-inductor [56], [57], quasi z source [58], and multilevel or multiport BDCs [59]. The EV applications require high VTR at low or moderate duty ratios. The classic boost converter with cascaded structure and bidirectional switches is an initial attempt for the bidirectional converter with quadratic buck-boost VTR (QBDC). However, lower efficiency and elevated switch voltage stresses are its shortfalls. An extended two-stage QBDC is proposed [60] for battery-driven EV applications. Though it has improved VTR its component count is high and it has diodes to enhance its output voltage. The QBDC topologies with the same VTR as in [59] are reported in [61], [62] with reduced input current ripple and electric stress. Recently, a novel BDC with continuous currents and quadratic buck-boost VTR has been proposed in [63]. Furthermore, an improved semiconductor utilization factor-based QBDC is proposed in [64]. Even though all the aforementioned converters report high VTR they also possess higher element count and control complexity.

2.5 Nonisolated unidirectional Quasi Z Source (QZS) Converters

The formulation of QZS converter in the form of PSL and cascaded structures in regard of synthesis point of view is discussed in this section. All the diodes in PSL arrangement (except the diagonal one) are replaced by capacitors to formulate the QZS converter but for quadratic boost converter development it is sufficient to replace any one of these diodes by a capacitor as shown in Figure 2.8 (a). However, this structure is not popular because of its non smooth current at its source terminals. Similarly, in cascade section also the diode D_2 is replaced by a capacitor to form QZS as shown in Figure 2.8 (b).

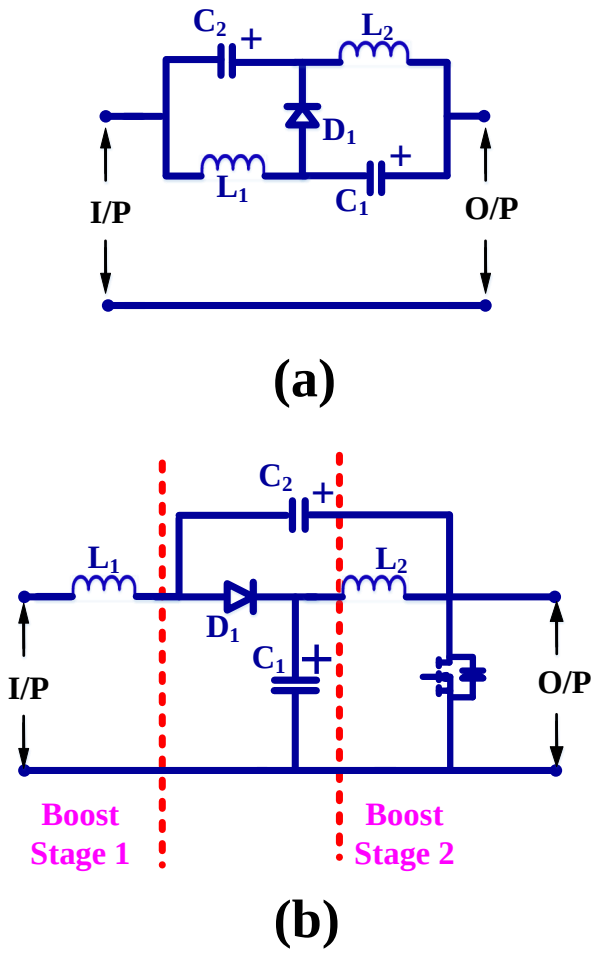


Figure 2.8 Formulation of QZS from (a) PSL and (b) two stage boosting.

The aforementioned concerns of high element voltage stress and low efficiency due to elevated duty ratios are prevailed by low duty operated converters. Reduction in upper bound duty is an alternate solution for the stated concerns, one such type of converter is the impedance source or Z source converter (ZSC). Here an impedance (L-C) network is employed between the dc source and converter or inverter as in [65] for dc-ac and ac-dc power conversion. To enhance ZSC voltage gain further three topologies i.e., single, and double Quasi-Z-source (QZS) integrated, and QZS embedded Z-source dc-dc converters are reported in [66]. In addition to the above stated topologies numerous converters are reported in the literature to enhance the boosting factor of ZSC [67]-[75] but these topologies are lack of realizing the low dc source ripple current. The converters in [76], [77] achieves improved voltage gain with voltage multiplier cells and or charge pump networks at low source ripple current by means of an inductor at the input port. The shortfalls of these topologies are their higher order and control complexity.

A voltage gain similar to QZS with the aid of Sheppard-Taylor H- Bridge type switched capacitor (HBSC) is proposed in [78] with constant voltage at the output terminals. This HBSC

structure is modified in [36] integrating charge pump cells to enhance the boosting factor but here the source current persists high inrush at starting and moreover this topology does not comprise of common ground. A capacitor clamped type of HBSC structure is reported in [79], [37] with voltage multiplier cells to amplify the boosting factor. Though these converters have the features like common ground and low source current ripple but their L-C component count is high which leads to increased order of the system and complexity in control.

2.6 Summary

In this chapter, pertinent literature on the nonisolated unidirectional and bidirectional dc-dc converters is extensively evaluated. The thesis research endeavours are driven by the identification of the gaps in the stated literature as well as the benefits and shortfalls of nonisolated dc-dc converters.

Chapter 3

Nonisolated High Gain Hybrid Switched-Inductor DC-DC Converter with Common Switch Grounding

3. Nonisolated High Gain Hybrid Switched-Inductor DC-DC Converter with Common Switch Grounding

3.1 Introduction

This chapter presents a methodology that integrates the hybrid switched inductor (HSL) and split duty ratio techniques to synthesize a high gain converter with common switch grounding (HSL-CSG). The dc-dc converter's high gain feature is required for micro source power processing in low voltage renewable energy systems. The amplification in voltage gain of the proposed converter is achieved without using transformer, common core coupled inductors, voltage multipliers, intermediate capacitors and voltage lifting methods so that the topology is simple in construction and operation. Moreover, with a split duty ratio the proposed converter switches are less prone to current stress due to reduction in extreme conducting duty intervals. The topological derivation, operating principle, and analysis of continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are presented. The theoretical analysis is validated with the aid of a laboratory prototype. This chapter proposes a topology with split duty ratio and hybrid switched inductor configuration and the key merits are explained as follows:

- Split duty control makes the proposed converter superior in terms of avoiding the longer conducting duty ratio that exists in single switch converters.
- The switch proximate to the power supply will have voltage stress less than the output voltage.
- Among three switches only one switch is operated at input current for a low duty cycle whereas the remaining two switches are operated at half of the input current.
- The proposed converter can achieve higher voltage amplification without using any clamping circuits, switched capacitor, and voltage multiplier cell techniques making the converter construction simple and compact.

The chapter has the following organization: Section-3.2 emphasizes the synthesis Section-3.3 describes operation and analysis along with Section 3.4 DCM analysis, Section-3.5 presents the element design, and Section-3.6 describes the efficiency measures. Section 3.7 comprises discusses the experimental results. Section-3.8 emphasizes the performance comparison and the summary is presented in 3.9.

3.2 HSL-CSG Topological Derivation

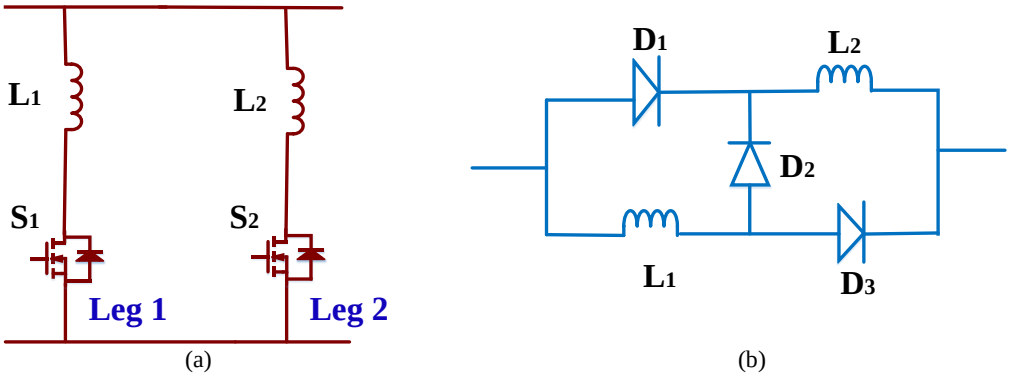


Figure 3.1 (a) ASL-CSG (b) PSL

An active switched inductor with the common switch grounding structure (ASL-CSG) is derived by combining the active switched inductor (ASL) technique [80], [84] with the common switch grounding arrangement as shown in Figure 3.1 (a). This ASL-CSG network consists of two legs, in leg 1 the inductor L_1 is followed by switch S_1 and in leg 2 inductor L_2 is followed by switch S_2. The inductors are shunted across the source when the switches are turned on. Since one end of the two switches is connected to the ground and hence the name common switch grounding. Further, the passive switched inductor (P-SL) arrangement as depicted in Figure 3.1 (b) is also integrated in ASL-CSG to develop the proposed hybrid switched inductor-common switch grounding network (HSL-CSG) topology as shown in Figure 3.2.

The split duty technique is proposed in [84], in which during the second switching period (D_2T_S) each inductor is powered by half of the supply voltage which makes the inductor *di/dt* to fall and store less energy. In the proposed converter with HSL-CSG topological enhancement, each inductor is applied with total input voltage even during the period of D_2T_S. To accomplish this, a third switch is incorporated in the proposed topology across the switch S_2. The parallel switches S_2 and S_3 will share the charging interval of the inductors.

Since the switches, S_2 and S_3 are in parallel the choice of considering one switch in the place of two would not be feasible because it leads to additional current stress and long conducting interval for the residue switch.

3.3 CCM Operation and Analysis

The proposed converter contains four diodes (D_0, D_1, D_2 and D_3), three switches (S_1, S_2 and S_3) followed by passive elements of two inductors (L_1 and L_2) and one capacitor (C_0) as shown in Figure 3.2. The two inductors contain an equal number of turns and similar core is used, hence these two are postulated to be identical.

$$L_1=L_2=L \tag{3.1}$$

For the steady-state operation equivalent series resistance (ESR) of all components, forward voltage drop of the diodes and the voltage drop due to ON state resistance of the switches are neglected to make the system ideal.

In CCM, one operating cycle of the HSL-CSG converter there exists three different modes with two duty ratios as shown in Figure 3.3 (b). The waveforms of various element voltages and currents are as shown in Figure 3.3 (a).

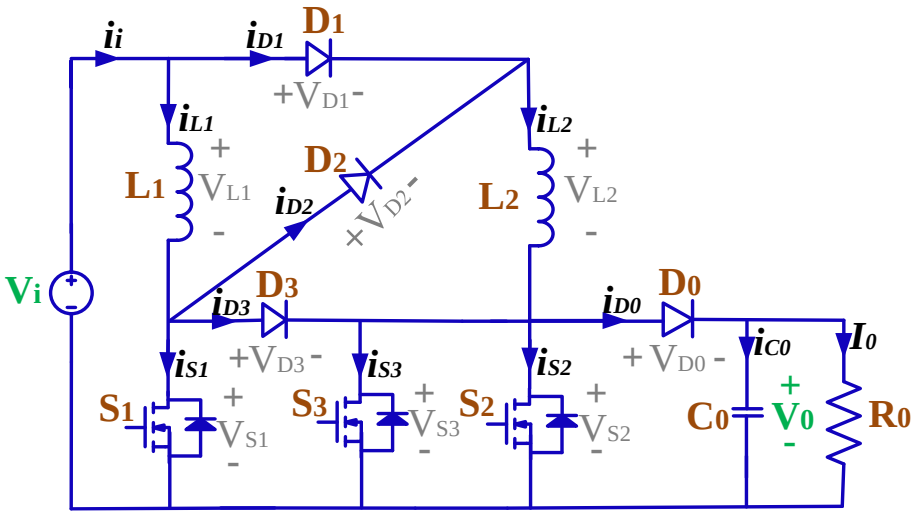


Figure 3.2. Proposed HSL-CSG Topology

3.3.1 Mode I of Operation

In this mode (t_0-t_1), switch pair S_1, S_2 of leg 1 and leg 2 are turned ON by magnetizing the inductors L_1, L_2 with a voltage of V_i and intermediate switch S_3 being turned OFF. In this mode diode D_3 is forward biased i.e., floating which makes the voltage across switch S_3 zero. The path for conduction with forward biased diode D_1 along with reverse biased diodes D_0, D_2 is as shown in Figure 3.3 (b) and the capacitor (C_0) discharges through the load.

The identical voltage and current profile across the two inductors are specified by the following equations.

$$v_{L1}=v_{L2}=V_i \tag{3.2}$$

$$i_{L1}=i_{L2}=i_L \tag{3.3}$$

The gradient in inductor currents (3.5) is derived by using (3.2) and (3.3), which is as follows

$$L\frac{di_{L1}}{dt}=L\frac{di_{L2}}{dt}=L\frac{di_L}{dt}=V_i \tag{3.4}$$

$$\frac{di_{L1}}{dt}=\frac{di_{L2}}{dt}=\frac{di_L}{dt}=\frac{V_i}{L}, \qquad t_0 \le t \le t_1 \tag{3.5}$$

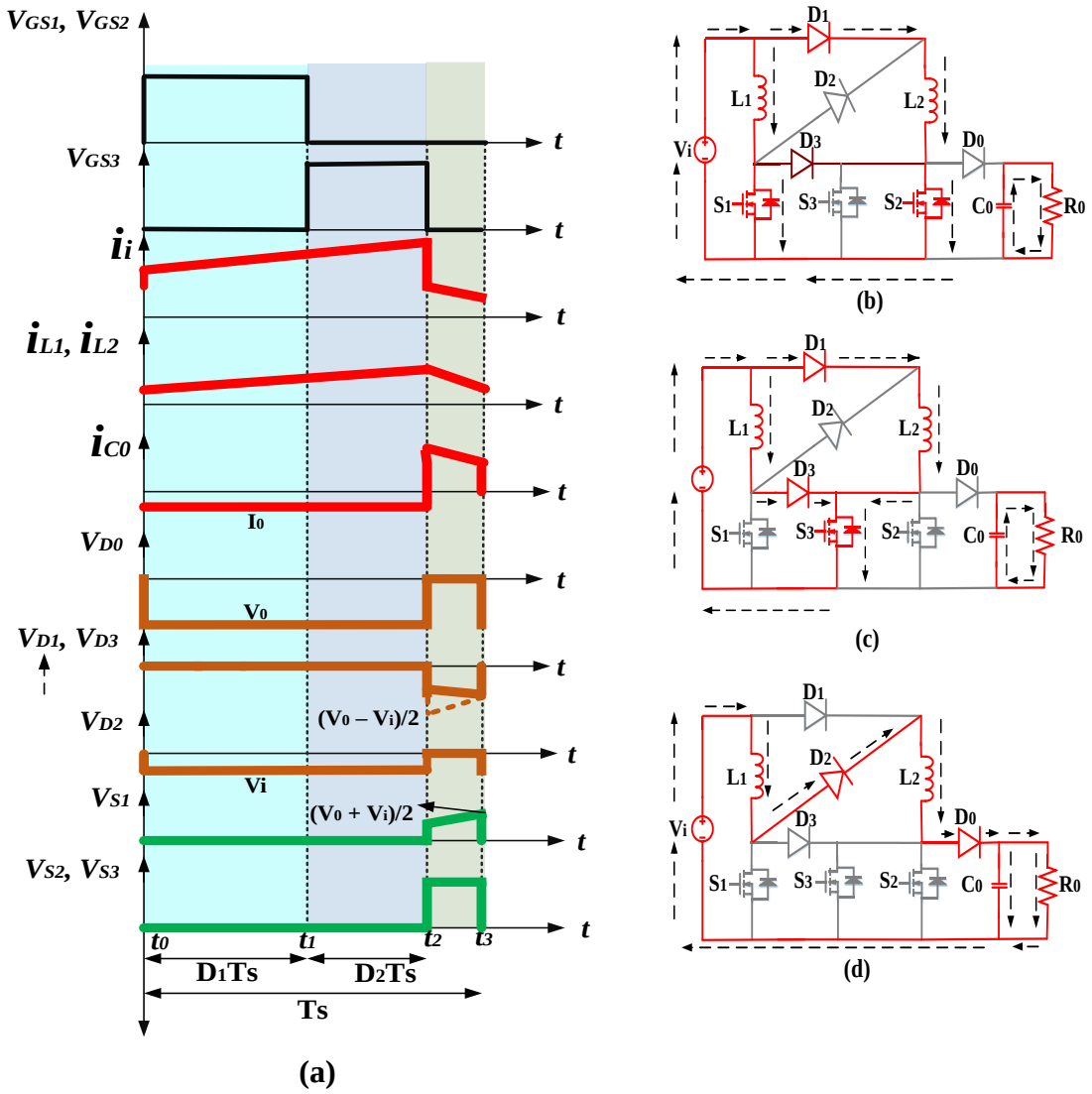


Figure. 3.3 HSL-CSG converter (a) typical waveforms in CCM; modes of operation (b) S_1, S_2 ON for Mode I (c) S_3 is ON for Mode II and (d) S_1, S_2, S_3 are OFF for Mode III.

3.3.2 Mode II of Operation

During this mode (t_1-t_2), the energization of inductors L_1, L_2 is similar to the previous mode by keeping S_3 at ON and S_1, S_2 are at OFF condition, which makes diode D_3 to conduct. Each inductor consists of total input voltage across it and the capacitor C_0 will power the load as depicted in Figure. 3.3 (c).

The identical voltage and current profile of the two inductors are specified by the following equations.

$$v_{L1}=v_{L2}=V_i \tag{3.6}$$

$$i_{L1}=i_{L2}=i_L \tag{3.7}$$

The gradient in inductor current (3.8) is obtained using (3.6) and (3.7), which is as follows

$$\frac{di_L}{dt}=\frac{V_i}{L}, \qquad t_1 \leq t \leq t_2 \tag{3.8}$$

3.3.3 Mode III of Operation

During this interval of time (t_2-t_3) switch pair S_1, S_2 and intermediate switch S_3 are at OFF condition with diodes D_1, D_3 are reverse biased. The conduction path is as shown in Figure 3.3 (d), which contains forward biased diodes D_0 and D_2. In this mode the source along with two inductors charge the combination of capacitor C_0 and load R_0.

The inductor voltages and currents are as follows

$$v_{L1}=v_{L2}=\frac{V_i-V_0}{2} \tag{3.9}$$

$$i_{L1}=i_{L2}=i_L \tag{3.10}$$

Solving (3.9), (3.10) for the rate of change of inductor current, which is as follows

$$\frac{di_L}{dt}=\frac{V_i-V_0}{2L}, \qquad t_2 \leq t \leq t_3 \tag{3.11}$$

By applying state space averaging method on (3.5), (3.8) and (3.11) the following equation is obtained.

$$\int_0^{D_1T_S}\left(\frac{di_L}{dt}\right)^{I}dt+\int_0^{D_2T_S}\left(\frac{di_L}{dt}\right)^{II}dt+\int_0^{(1-D_1-D_2)T_S}\left(\frac{di_L}{dt}\right)^{III}dt=0 \tag{3.12}$$

The superscripts denote the corresponding mode of operation. By solving (3.12), the HSL-CSG converter CCM voltage gain is as follows

$$G_{CCM}=\frac{V_0}{V_i}=\frac{1+D_1+D_2}{1-D_1-D_2} \tag{3.13}$$

The voltage gain in (3.13) for fixed duty ratio D_2 is plotted against the duty ratio D_1 as shown in Figure 3.4 and for the vice-versa case, the plot is identical because voltage gain is symmetrical even if the duty ratios D_1 and D_2 are interchanged in (3.13). It is evident from the plot that if the duty ratio D_1 or D_2 is increased then gain will also increase in proportion with a factor specified in (3.13).

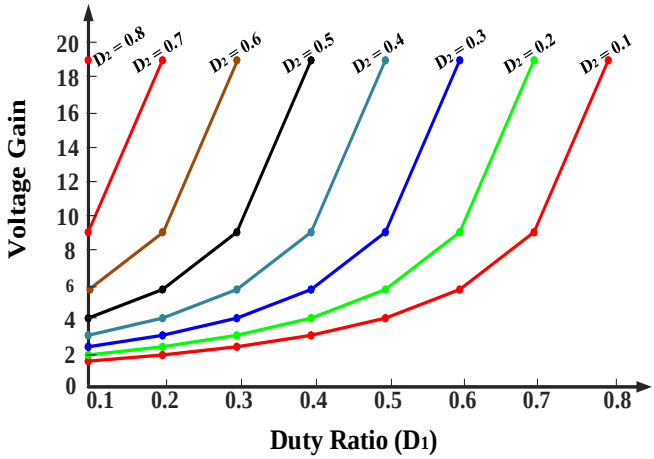


Figure 3.4. Voltage gain (CCM) corresponding to variation in D_1

3.4 DCM Analysis

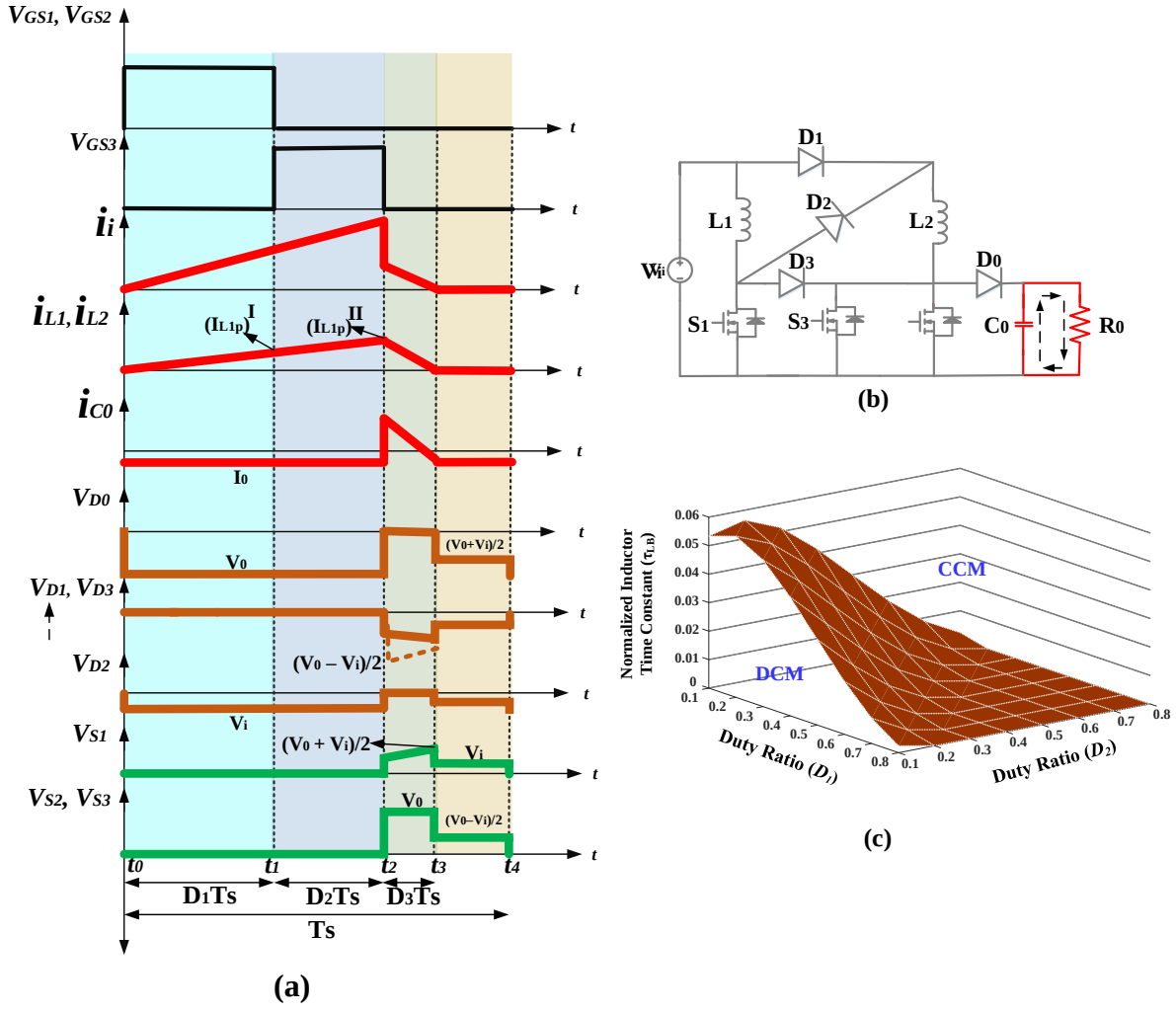


Figure 3.5. HSL-CSG converter DCM Operation (a) operating wave forms and (b) mode IV operation

The ideal operating waveforms and mode IV of HSL-CSG converter in DCM operation are presented in Figure 3.5. From Figure 3.5 (a), the peak currents of two inductors L_1 and L_2 at (the end of) mode II and (the beginning of) mode III are equal.

$$\frac{V_i}{L}\ (D_1+D_2)T_S=\frac{V_0-V_i}{2L}\ D_3T_S \tag{3.14}$$

Solving the above equation for the formulation of D_3

$$D_3=\frac{2V_i(D_1+D_2)}{V_0-V_i}$$

The Capacitor C_0 current in DCM mode of operation is expressed as

$$I_{C0}=\frac{1/2\ (D_3\ T_S)\ \left(i_{L1p}\right)^{II}}{T_S}-I_0$$

Using the formulation of D_3 in the above expression and equating it to zero, the DCM voltage gain of HSL-CSG converter is expressed as

$$G_{DCM}=\frac{V_0}{V_i}=\frac{1}{2}+\sqrt{\frac{1}{4}+\frac{(D_1+D_2)^2}{\tau_L}} \tag{3.15}$$

Where the normalized inductor time constant (τ_L) is expressed as

$$\tau_L=\frac{Lf_s}{R_0}$$

The boundary inductor time constant is evaluated by equating the CCM and DCM voltage gains and is expressed as follows

$$\tau_{LB}=\frac{(D_1+D_2)\ \left(1-(D_1+D_2)\right)^2}{2(1+D_1+D_2)} \tag{3.16}$$

The variation of time constant with respect to duty ratios is represented in Figure 3.5 (c).

3.5 Inductor and Capacitor Selection

The selection of inductors (L_1=L_2=L) and output capacitor C_0 depends on the factors like input voltage (V_i), duty ratio (D_1), inductor ripple current (Δi_L), switching frequency (f_s); load wattage (P_0), rated voltage (V_0) and voltage ripple of capacitor (ΔV_c). The critical values of inductors (L_{1c}, L_{2c}) and capacitor (C_{0c}) for CCM operation are as follows

$$L_{1c}=L_{2c}=\frac{V_i\ D_1}{\Delta i_L\ f_s} \tag{3.17}$$

$$C_{0c}=\frac{P_0}{V_0\ \Delta V_c\ f_s} \tag{3.18}$$

3.6 Efficiency Analysis

The majority portion of performance indices of any power converter depends on parasitics of the elements in the power circuit. Hence, topological visualization of these parasitic parameters is shown in Figure 3.6, where r_{L1}, r_{L2}, r_{C0} are the ESR of the passive elements L_1, L_2 and C_0. The ESR and forward voltage drops of the diodes are r_{D0}, r_{D1}, r_{D2}, r_{D3} and V_{D0}, V_{D1}, V_{D2}, V_{D3} respectively.

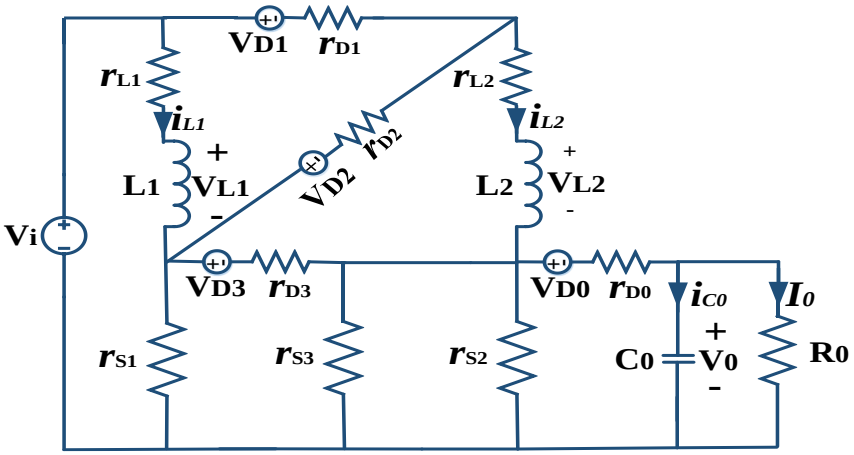


Figure. 3.6. Equivalent circuit with parasitic parameters

Similarly, r_{S1}, r_{S2}, r_{S3} represents the conduction resistance (drain to source) of S_1, S_2 and S_3 respectively. Further, the capacitor current analysis is carried out by neglecting the ESR voltage drop because it is very small and also to make the calculations simple.

Mode I: In this mode switch pair S_1, S_2 are operated similar to the previous CCM case. The forward voltage drop V_{D1} of diode D_1 is neglected on the basis that the percentage deviation caused by V_{D1} in the inductor current i_{L2} from i_{L1} is 0.76%, 4% concerning inductor current i_{L1} and ripple current ΔI_{L1} respectively. This assumption makes the two inductor currents identical in this mode of operation.

The capacitor current and inductor voltages are as follows

$$(i_{C0})^{I} = -\frac{V_0}{R_0} \tag{3.19}$$

$$(v_{L1})^{I} = V_i - i_{L1}(r_{L1} + r_{S1}) \tag{3.20}$$

Mode II: In this mode intermediate switch is operated. The capacitor current and inductor voltages are given by the following equation.

$$(i_{C0})^{II} = -\frac{V_0}{R_0} \tag{3.21}$$

$$(v_{L1})^{II} = V_i - i_{L1}\left(r_{L1} + r_{D3} + 2r_{S3}\right) - V_{D3} \tag{3.22}$$

Mode III: In this mode S_1, S_2 and S_3 are at OFF condition. The capacitor current and inductor voltages are specified as follows

$$(i_{C0})^{III} = I_{L1} - \frac{V_0}{R_0} \tag{3.23}$$

$$(v_{L1})^{III} = \frac{V_i - i_{L1}(r_{L1}+r_{L2}+r_{D2}+r_{D0}+r_{C0}) - (V_{D2}+V_{D0}) - V_0}{2} \tag{3.24}$$

Applying the amp-sec balance for the capacitor C_0

$$\int_0^{D_1T_S} (i_{C0})^{I}\, dt + \int_0^{D_2T_S} (i_{C0})^{II}\, dt + \int_0^{(1-D_1-D_2)T_S} (i_{C0})^{III}\, dt = 0 \tag{3.25}$$

Substituting (3.19), (3.21) and (3.23) in (3.25) and solving for I_{L1}

$$I_{L1} = \frac{V_0}{R_0(1-D_1-D_2)} \tag{3.26}$$

Similarly applying volt-sec balance to inductor L_1

$$\int_0^{D_1T_S} (v_{L1})^{I}\, dt + \int_0^{D_2T_S} (v_{L1})^{II}\, dt + \int_0^{(1-D_1-D_2)T_S} (v_{L1})^{III}\, dt = 0 \tag{3.27}$$

Substituting (3.20), (3.22) and (3.24) in (3.27) and solving for V_0

$$V_0 = \frac{V_i(1+D_1+D_2) - (2V_{D3})D_2 - (V_{D2}+V_{D0})(1-D_1-D_2)}{(1-D_1-D_2) + 2\left(\frac{AD_1+BD_2+C(1-D_1-D_2)}{R_0(1-D_1-D_2)}\right)} \tag{3.28}$$

Where

$$\begin{cases} A = (r_{L1}+r_{S1}) \\ B = (r_{L1}+r_{D3}+2r_{S3}) \\ C = (r_{L1}+r_{L2}+r_{D2}+r_{D0}+r_{C0}) \end{cases}$$

The proposed HSL-CSG converter input and output powers are acquired as follows

$$P_i = 2\, V_i\, I_{L1}\, (D_1+D_2) + V_i\, I_{L1}\, (1-D_1-D_2) \tag{3.29}$$

Using (3.26) in (3.29) the input power is written as

$$P_i = \frac{V_i V_0}{R_0} \left(\frac{1+D_1+D_2}{1-D_1-D_2}\right) \tag{3.30}$$

The HSL-CSG converter output power is written as

$$P_0 = \frac{V_0^2}{R_0} \tag{3.31}$$

From (3.28), (3.30) and (3.31), the efficiency of proposed converter is written as

$$\eta = \frac{(1-(D_1+D_2)^2)-\left(\frac{(2V_{D3})(1-D_1-D_2)+(V_{D2}+V_{D0})(1-D_1-D_2)^2}{V_i}\right)}{(1+D_1+D_2)\left\{(1-D_1-D_2)+2\left(\frac{AD_1+BD_2+C(1-D_1-D_2)}{R_0(1-D_1-D_2)}\right)\right\}} \quad (3.32)$$

The switching losses must be deducted from (3.32) to account for this portion of losses in efficiency calculations.

3.7 Experimental Results

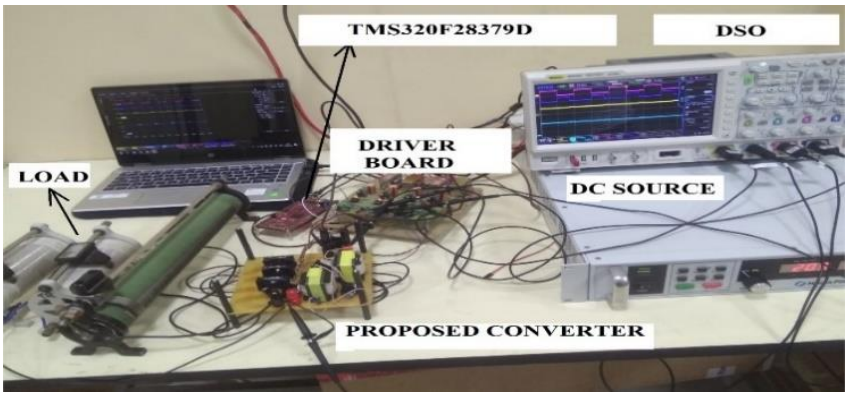


Figure 3.7. Experimental setup

The proposed converter theoretical analysis has been validated with a prototype as shown in Figure 3.7 and its specifications are provided in Table 3.1. The gate pulses V_{GS1}, V_{GS2} are of 50% duty ratio and identical to each other as shown in Figure 3.8. The gate pulse V_{GS3} is of 35% duty ratio and 180˚ phase shift with respect to V_{GS1}.

A voltage gain of 11.75 is attained for an input voltage of 20 V. The HSL-CSG converter draws an average input current (i_i) of 7.4 A to deliver a load current (i_0) of 590 mA as shown in Figure 3.8 (b). Since, the converter operates in CCM the inductor currents i_{L1} and i_{L2} are continuous as shown in Figure 3.8 (c). The instantaneous capacitor current i_{C0} is shown in Figure 3.8 (d). The blocking voltage of switch S_1 is equal to an average of V_i, V_0 and that of S_2 and S_3 is V_0 as shown in Figure 3.8 (e) and (f). From Figure 3.8 (g) it is evident that the diodes D_0 and D_2 are at a voltage stress of V_0 and V_i respectively. The diodes D_1 and D_3 will have equal voltage stress of half of the difference of V_i and V_0.

The proposed converter is operating with an experimental efficiency of 93.7% at rated power condition. From Figure 3.9 (a) it is evident that the proposed converter efficiency is well above 91% for different load conditions. The proposed HSL-CSG converter distribution of power loss at rated power of 150 W is shown in Figure 3.9 (b), where the switches are having the highest loss proportion of 51% and next diodes with a loss proportion of 34%. In other words, among total power loss 85% is contributed by only switches and diodes.

The feasibility of HSL-CSG converter for dynamic changes in the load and duty ratio is experimentally validated as shown in Figure 3.10 (a), (b), (c) and (d). The load variations are considered from half load to full load and vice versa. The variation in the duty ratio is considered in two cases as shown in Figure 3.10 (c) and (d), where in the first schematic the duty variation is from 85% to 60% and that of in the second three step variation of duty ratio (85% - 50% - 70%) is accounted.

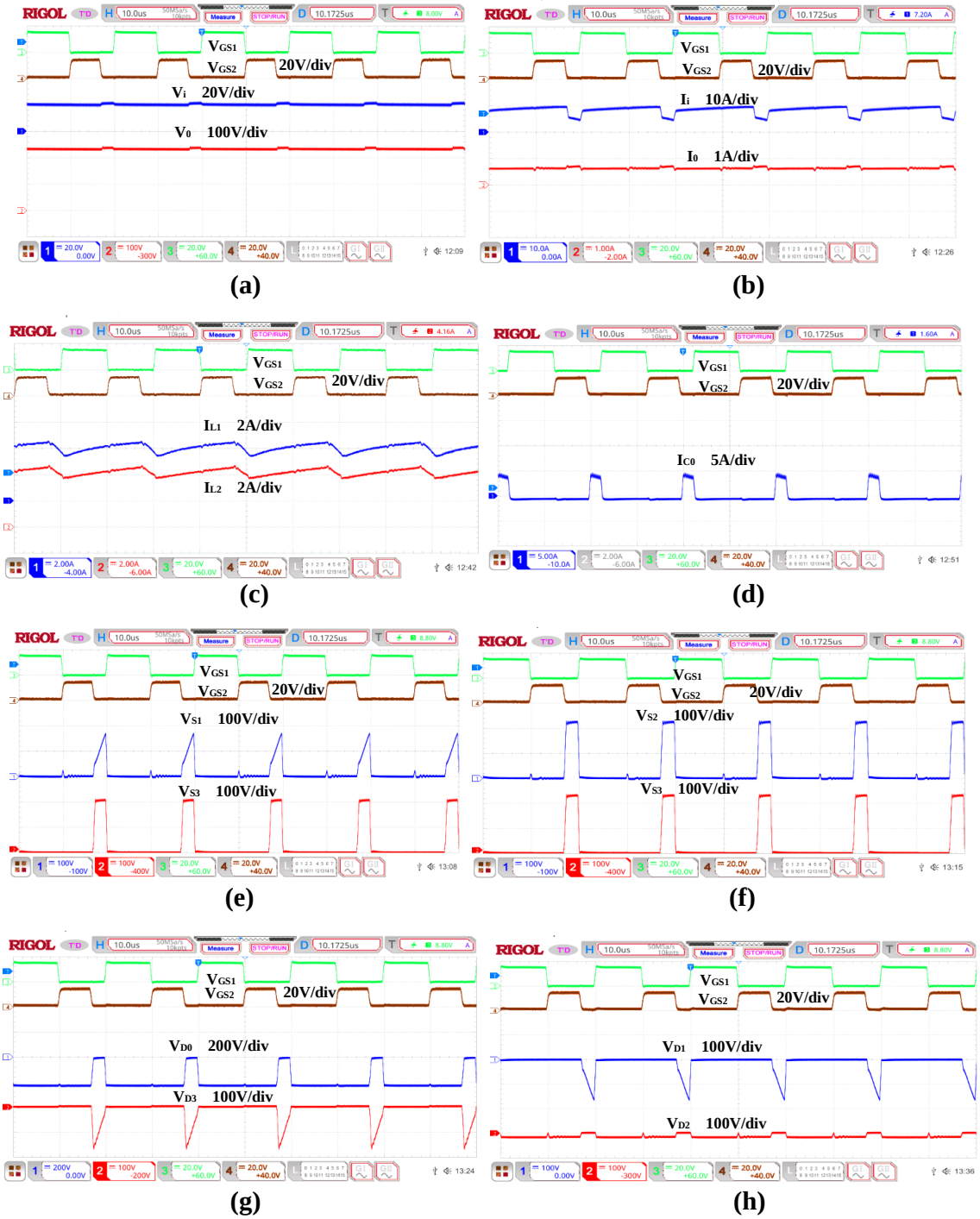


Figure. 3.8. Experimental results(a) Input and output voltages (V_i and V_0) (b) Input and output currents (i_i and i_0) (c) Inductor currents (i_{L1} and i_{L2}) (d) Capacitor current (i_{C0}) (e) Switch voltages (V_{S1} and V_{S3}) (f) Switch Voltages (V_{S2} and V_{S3}) (g) Diode voltages (V_{D0} and V_{D3}) (h) Diode voltages (V_{D1} and V_{D2}).

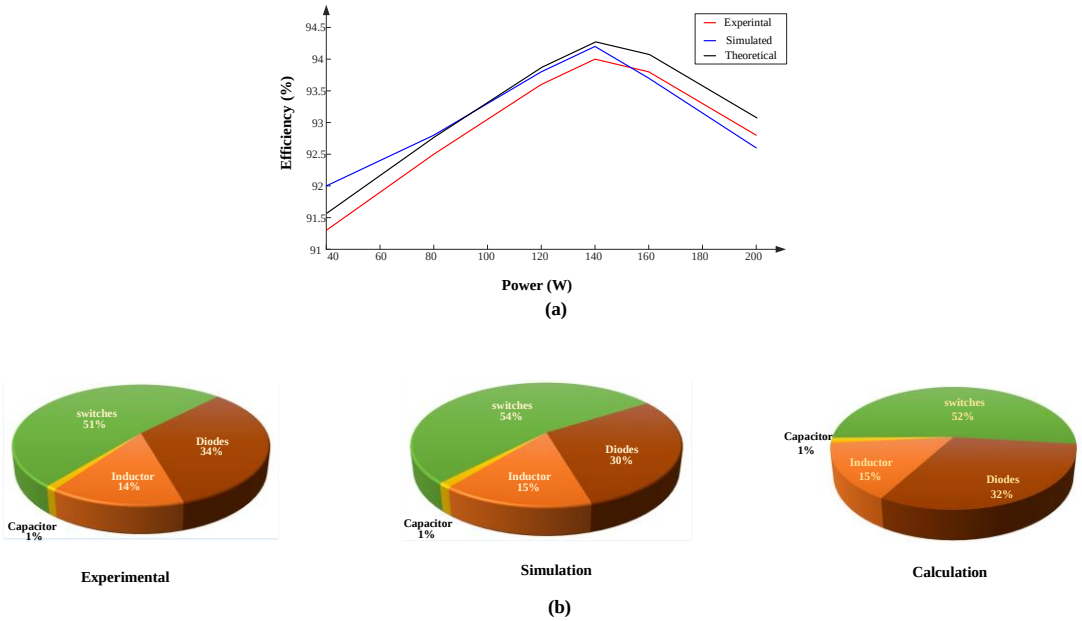


Figure 3.9. (a) Efficiency corresponding to output powers and (b) Power loss distribution.

The stability of the converter is validated by state space averaging method in which a control to output transfer function like standard passive switched inductor is adopted. Since there are two duty ratios in HSL-CSG converter therefore in control logic it is implemented that for the duty ratios less than 50% only switch pair S_1 and S_2 will respond, and for the duty ratios more than 50% the switch S_3 will come into picture by sharing the additional duty ratio above 50%. The closed loop validation of the proposed converter with controller is reported in Figure 3.11.

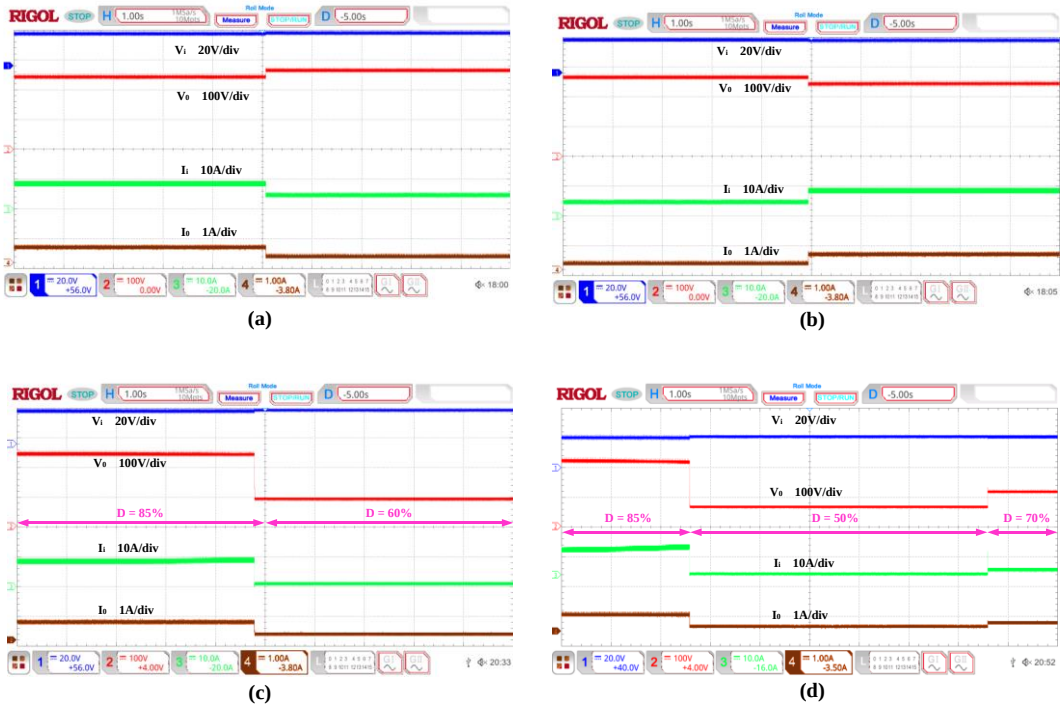


Figure 3.10. Dynamic variation of HSL-CSG converter in terms of (a) load increase (66% to 100%) (b) load decrease (100% to 66%) (c) two step variation in duty ratio (d) Three step variation in duty ratio.

Table 3.1 Prototype Specifications

Rated Power (P_0)	≅150 W
Input Voltage (V_i)	20 V
Duty Ratio (D_1)	50%
Duty Ratio (D_2)	35%
Switching Frequency (f_s)	50 kHz
Inductors (L_1, L_2)	400 µH
Capacitor (C_0)	10 µF
Mosfet (S_1, S_2 and S_3)	STW28N65M2
Diode (D_0)	STPSC10H065

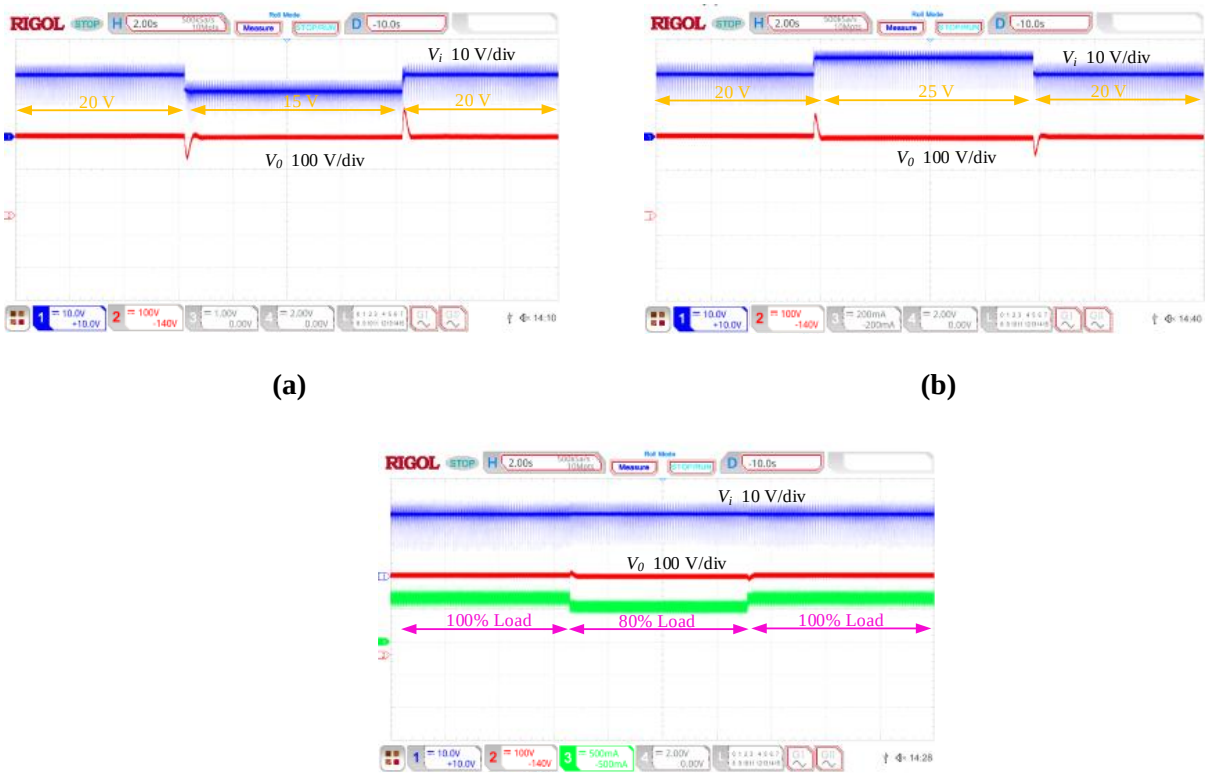


Figure 3.11 Closed loop validation of HSL-CSG converter (a) 20V-25V step change in input voltage (b) 20V-25V step change in input voltage and (c) step change in load from 100% to 80 % of rated load.

The bode plots are also formulated to strengthen the closed loop validation of HSL-CSG converter and are as shown in Figure 3.12. To obtain a stable output voltage PI tuning is carried out with the aid of Ziegler–Nichols method. The ideal operating conditions validation is reflected in the Figure 3.13. From the simulated results one can conclude that the experimental results are in good accord with the ideal simulated results.

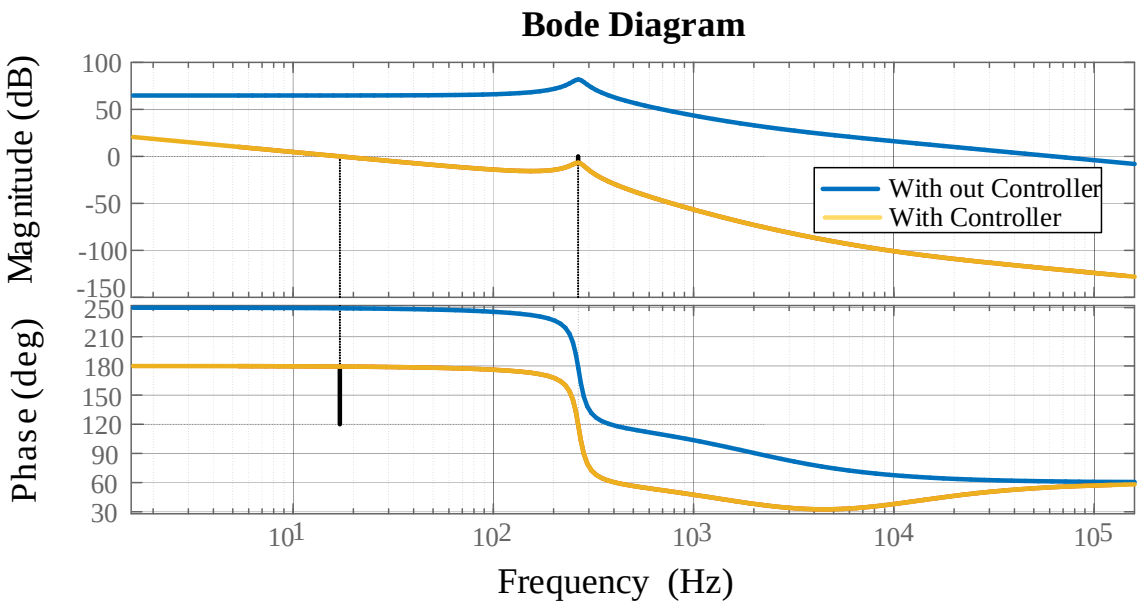


Figure 3.12 Bode plot of HSL-CSG converter

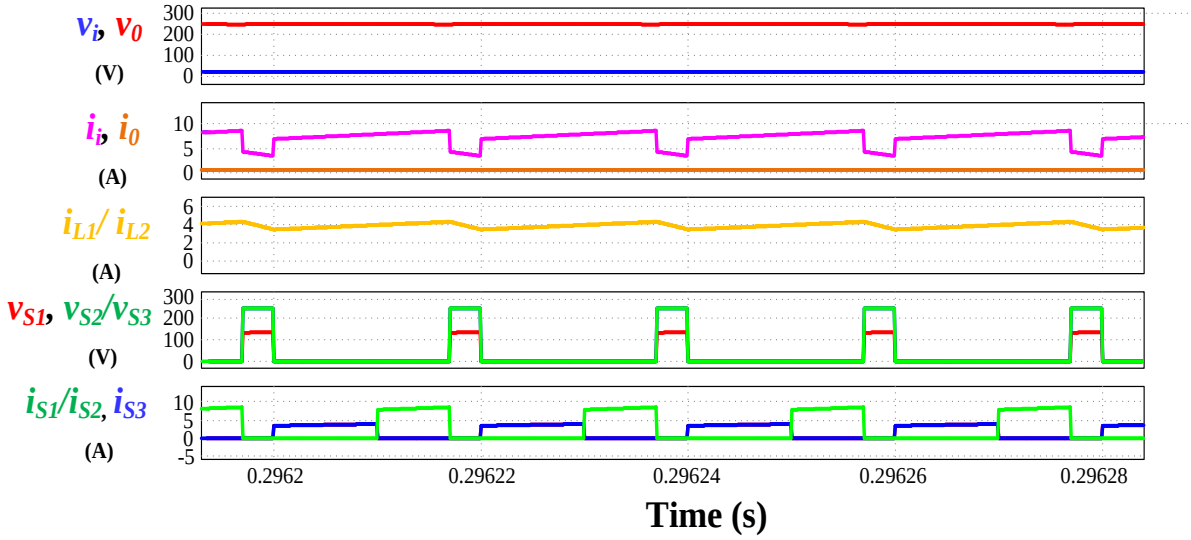


Figure 3.13 Simulated results of HSL-CSG converter

3.8 Performance Comparison

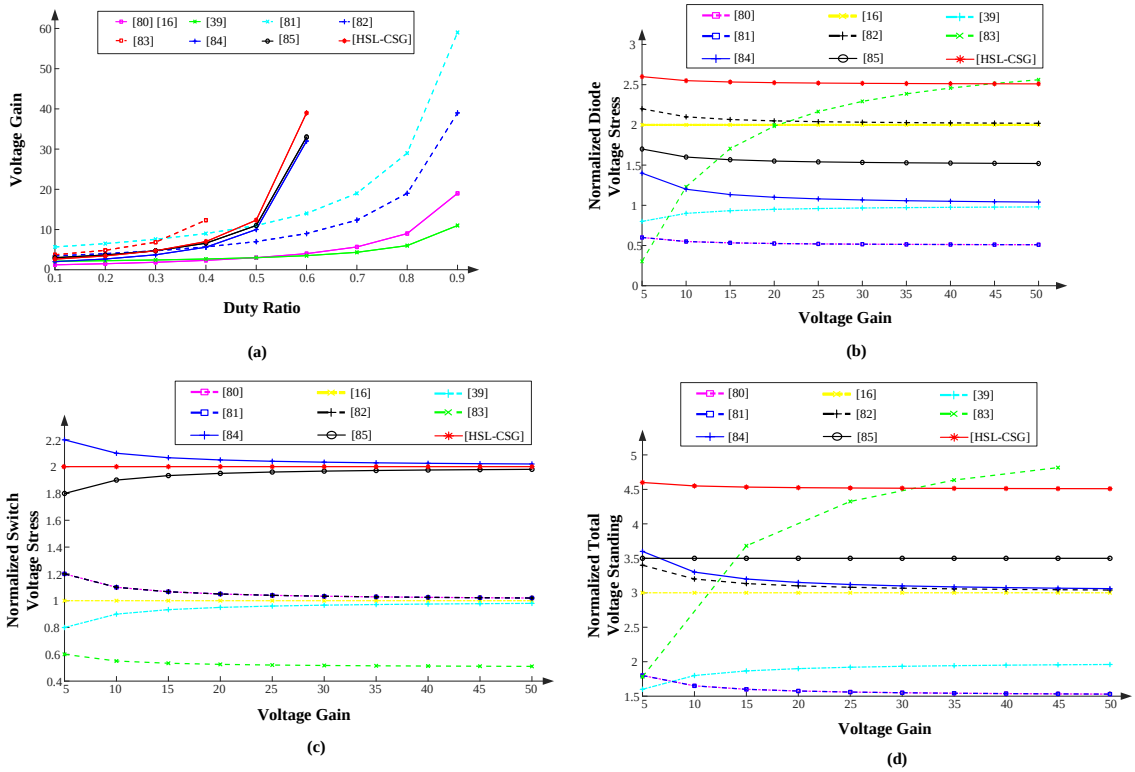


Figure. 3.14 Performance comparison (a) voltage gain (b) NDVS (c) NSVS and (d) NTVS

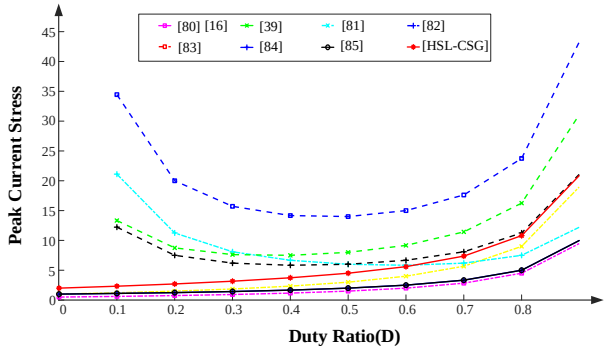


Figure. 3.15 Peak current stress versus duty ratio of Switches

The comparative analysis of proposed converter with existing high gain converters in terms of stepup gain, element count, device voltage stress i.e. normalized voltage stress of diodes, switches, total voltage standing, peak current stress on switches, possibility of split duty, common grounding between source and load is provided in Table 3.2. The split duty converters [84] and [85] in comparison with the single duty converters will reduce the long conducting duty cycles for the switches. As depicted in Figure 3.14 (a), for the duty ratio $D_1 = 0.6$ and $D_2 = 0.35$ the theoretical voltage gain attained by HSL-CSG converter is 39, whereas the gain of the converters in [84] and [85] are 32 and 33 respectively. These voltage gains are far superior to those of the converters in [80], [16] and [39] which provide a voltage gain of 4 and 3.5 for

the same operating conditions stated above and among [81], [82] and [83] only [83] is in par with the voltage gain for the aforementioned conditions.

The normalized voltage stress across various elements of different converters in comparison with the proposed converter are presented in Table 3.2 and as shown in Figure 3.14 (b), (c) and (d). The normalized voltage stress on diodes of HSL-CSG is similar to the converters in [84], [85] and this is higher comparing to the other converters because of no intermediate capacitors in the proposed converter as shown in Figure 3.14 (b). The switch voltage stress and total voltage standing as shown in Figure 3.14 (c) and (d), it is similar to above mentioned switch voltage profile. The proposed converter switch count is the same as that of the converters in [84], [85]. The inductor and capacitor counts are equal to the converters in [80], [16], [84] and this count is less than the converters in [39],[81], [82] and [83]. The switches S_2, S_3 will have high voltage stress and this is permissible because of the facts that split in overall duty and high voltage gain provided by the HSL-CSG converter. The voltage gain per device count and the efficiency are also moderate for the HSL-CSG converter comparing with the other converters.

The intermediate switch S_3 will have the highest current stress compared to all elements because it has to carry the entire input current for a time period of D_2T_s as shown in Figure 3.15. The current stress profile of the HSL-CSG converter is better than the converters in [81, [82] and [83].

The ideal and experimental results comparison of the HSL-CSG converter is also carried out and reflected in Table 3.3, from which in can be concluded that the experimental results are in par with the ideally acquired magnitudes.

Table 3.2 Comparison of Nonisolated and Split Duty Converters

Topology	Voltage Gain (G)	Voltage Gain per component (G/C) At D=0.85 or D=0.43*	Normalized Diode Voltage Stress ($\sum V_D/Vo$)	Normalized Switch Voltage Stress ($\sum V_S/Vo$)	Normalized Total Voltage Standing	Peak Switch Current Stress ($\hat{I}_S/I_o$)	Common Ground	Constant Input Current	Split Duty	Long Conducting Duty Ratio	% η at 100w	Element Count			
												C_S	C_D	C_L	C_C
[16]Δ	$\left(\frac{1+D}{1-D}\right)$	1.5	2	1	3	$\frac{1+D}{1-D}$	YES	YES	NO	YES	88%	1	4	2	1
[39]□	$\left(\frac{2-D}{1-D}\right)$	0.8	$1-\frac{1}{G}$	$1-\frac{1}{G}$	$2-\frac{2}{G}$	$\frac{2-D}{D(1-D)}$	NO	YES	NO	YES	86%	1	3	2	4
[80]◊	$\left(\frac{1+D}{1-D}\right)$	2.5	$\frac{1}{2}+\frac{1}{2G}$	$1+\frac{1}{G}$	$\frac{3+3G}{2G}$	$\frac{1+D}{2(1-D)}$	NO	NO	NO	YES	92%	2	1	2	1
[81]	$\left(\frac{5+D}{1-D}\right)$	2.8	$\frac{1+G}{2G}$	$\frac{1+G}{G}$	$\frac{3+3G}{2G}$	$\frac{3+D}{D(1-D)}$	NO	NO	NO	YES	94.8%	2	5	4	3
[82]	$\left(\frac{3+D}{1-D}\right)$	1.8	$\frac{1+2G}{G}$	$\frac{1+G}{G}$	$\frac{2+3G}{G}$	$\frac{1+D}{D(1-D)}$	NO	NO	NO	YES	96.7%	2	5	4	3
[83]	$\left(\frac{3-3D-2D^2}{(1-D)(1-2D)}\right)$	1.2*	$\frac{8D-1}{3-3D-2D^2}$	$\frac{2-3D}{3-3D-2D^2}$	$\frac{3+5D}{3-3D-2D^2}$	$\frac{1+2D}{D(1-2D)}$	NO	NO	NO	YES	94%	2	4	3	5
			$D=\frac{(3G-3)-\sqrt{(3G-3)^2-(4(2G+2)(G-3))}}{2(G+2)}$												
Split Duty Converters															
[84]	$\left(\frac{1+D_1}{1-D_1-D_2}\right)$	1.3	$1+\frac{2}{G}$	$2+\frac{1}{G}$	$3+\frac{3}{G}$	$\frac{1}{1-D_1-D_2}$	NO	NO	YES	NO	93.6%	3	2	2	1
[85]*	$\left(\frac{2-D_2}{1-D_1-D_2}\right)$	1.1	$\frac{3}{2}+\frac{1}{G}$	$2-\frac{1}{G}$	$\frac{7}{2}$	$\frac{1}{1-D_1-D_2}$	YES	NO	YES	NO	91%	3	4	2	1
HSL-CSG*	$\left(\frac{1+D_1+D_2}{1-D_1-D_2}\right)$	1.2	$\frac{5}{2}+\frac{1}{2G}$	2	$\frac{9}{2}+\frac{1}{2G}$	$\frac{(1+D_1+D_2)(2-D_1-D_2)}{1-D_1-D_2}$	YES	NO	YES	NO	93.2%	3	4	2	1

◊=converter 1, Δ=Figure. 9, □=Sepic Derived (Switch and load side diode only), G =Voltage Gain, C_S= switch count, C_D = Diode count, C_L = Inductor count, C_C = Capacitor count, *Magnitude of device voltage stress is only considered

Table 3.3 Performance comparison of simulation and experimental findings of HSL-CSG converter

Performance Indices	Simulation	Experimental
Output voltage (V_0)	240 V	235 V
Output current (I_0)	0.587 A	0.590 A
Input current (I_i)	7.243 A	7.4 A
Inductor currents (I_{L1} & I_{L2})	3.915 A & 3.915 A	4 A & 4.1 A
Switch voltage stresses ($\hat{V}_{s1}$, $\hat{V}_{s2}$ & $\hat{V}_{s3}$)	133 V, 248 V& 248 V	170 V, 235 V & 235 V
Switch current stresses ($\hat{I}_{s1}$, $\hat{I}_{s2}$ & $\hat{I}_{s3}$)	4 A, 4 A & 8.64 A	4.2 A, 4.55 A & 9.2 A

3.9 Summary

This chapter presented a high gain nonisolated dc-dc converter namely HSL-CSG by integrating switched inductor and spit duty ratio flexibility. The converter operates with a split duty ratio to reduce the long conducting time intervals of the switches thus, make them less prone to failure. High stepup voltage gain was accomplished without transformers, voltage multipliers cells and numerous voltages lifting techniques. The proposed converter experimental validation was done with a prototype to verify voltage gain, efficiency and voltage stresses and the feasibility of the converter for dynamic variations in terms of load and duty ratio is also validated. A comparative analysis had been presented by considering existing similar switched inductor-capacitor topologies and other ultra-voltage gain converters including the converter based on quasi z source paradigm. The converter operated well above 91% efficiency for all load conditions and for full load an efficiency of 93.7% was attained. Finally, the proposed converter provides high voltage gain of 11.75 with HSL and split duty ratio flexibility.

Chapter 4

Active switched capacitor based ultra voltage gain quadratic boost dc-dc converters

4. Active switched capacitor based ultra voltage gain quadratic boost dc-dc converters

4.1 Introduction

This chapter presents active switched capacitor integrated ultra voltage gain quadratic boost converters (ASC-QBC). The step-up conversion ratio provided by quadratic boost converter is not ample to meet the renewable micro source applications. The active switched capacitor integrated quadratic boost converter is a propitious alternate to acquire high voltage conversion ratios. A simple diode-capacitor voltage lift arrangement is used in one of the introduced converters thereby further enhancing the voltage gain and also reducing the input current ripple to a greater extent. The voltage stress on semiconductor devices is greatly alleviated with the aid of diode-capacitor voltage lift arrangement. The control feasibility of the proposed converters against input voltage and load perturbations are experimentally demonstrated for a power rating of 100 W. The theoretical analysis and performance indices of proposed converters are validated with a fabricated laboratory prototype.

The chapter has the following organization: Section-4.2 describes topological derivation, Section-4.3 comprises of operation and analysis of ASCQBC-I converter, Section-4.4 presents operation and analysis of ASCQBC-II converter, Section 4.5 emphasizes control aspects. Section-4.6 discusses the experimental results, Section-4.7 presents the comparison of converters and the summary is presented in Section 4.8.

4.2 The Proposed Topology Power Circuit Derivation

The power circuit of ASC-QBC-I converter is constructed by integrating ASC cell with the quadratic boost configuration as shown in Figure 4.1. The switch S_1 along with diode D_1 and capacitor C_1 forms ASC cell and the rest of the circuit resembles the quadratic boost converter. The prime objective of capacitor C_1 of ASC cell in ASC-QBC-I converter is to charge the inductor L_2 along with the DC source (V_i) and capacitor (C_2).

The proposed ASC-QBC-I converter is a basic constructing element for the ASC-QBC-II converter in which switch S_2, diode D_2, and capacitor C_2 form ASC cell-II as shown in Figure 4.2. The diode-capacitor arrangement (D_4-C_4) is used for voltage lifting. Unlike capacitor C_1, the only purpose of capacitor C_2 in ASC cell II is to provide voltage lift but not to charge any of the two inductors (L_1 and L_2). By integrating ASC cell-II and diode (D_4)-capacitor (C_4) arrangement to the ASC-QBC-I, the ASC-QBC-II converter is obtained.

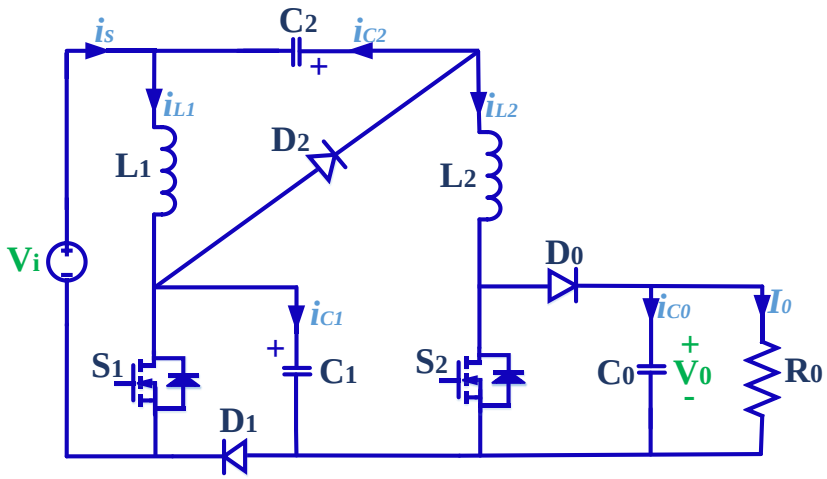


Figure 4.1. ASC-QBC-I converter

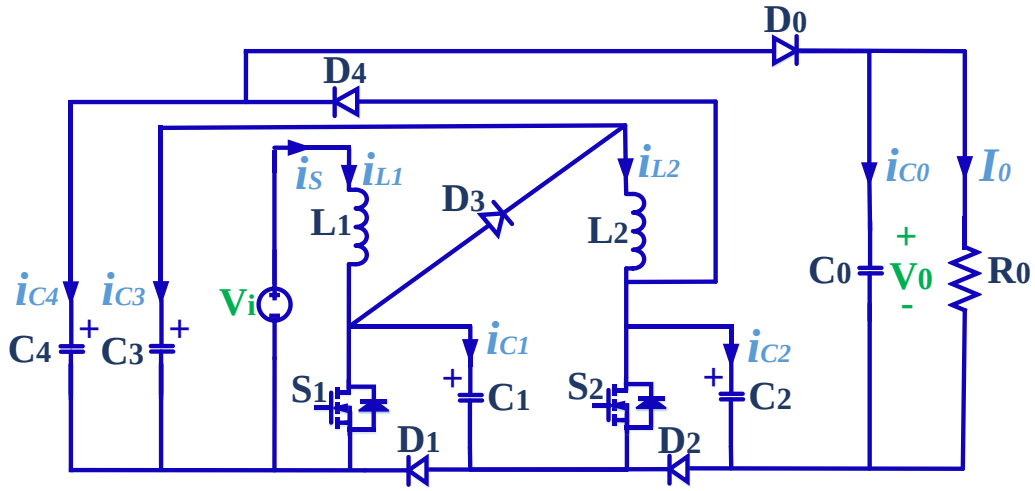


Figure 4.2. ASC-QBC-II converter

4.3 Analysis of ASCQBC-I Converter

The following analysis of ASC-QBC-I converter in terms of performance indices like voltage gain, element voltage and current stress, the effect of element parasitics, and converter efficiency is carried out for CCM operation. The theoretical waveforms for the ASC-QBC-I converter are as shown in Figure 4.3 (a).

4.3.1 Operating State I ($0 \le t \le t_1$; DT_S)

The operating state I for a duration of DT_s corresponds to the turn ON of the switches (S_1 and S_2) at the instant t_0 as shown in Figure 4.3 (b). The input voltage (V_i) is applied across the inductor L_1, whereas the inductor L_2 will have a sum of voltages of V_i, V_{C1} and V_{C2}. Since diode D_0 is reverse biased load (R_0) is powered by capacitor C_0. In this operating state, all the intermediate capacitors are in discharging mode.

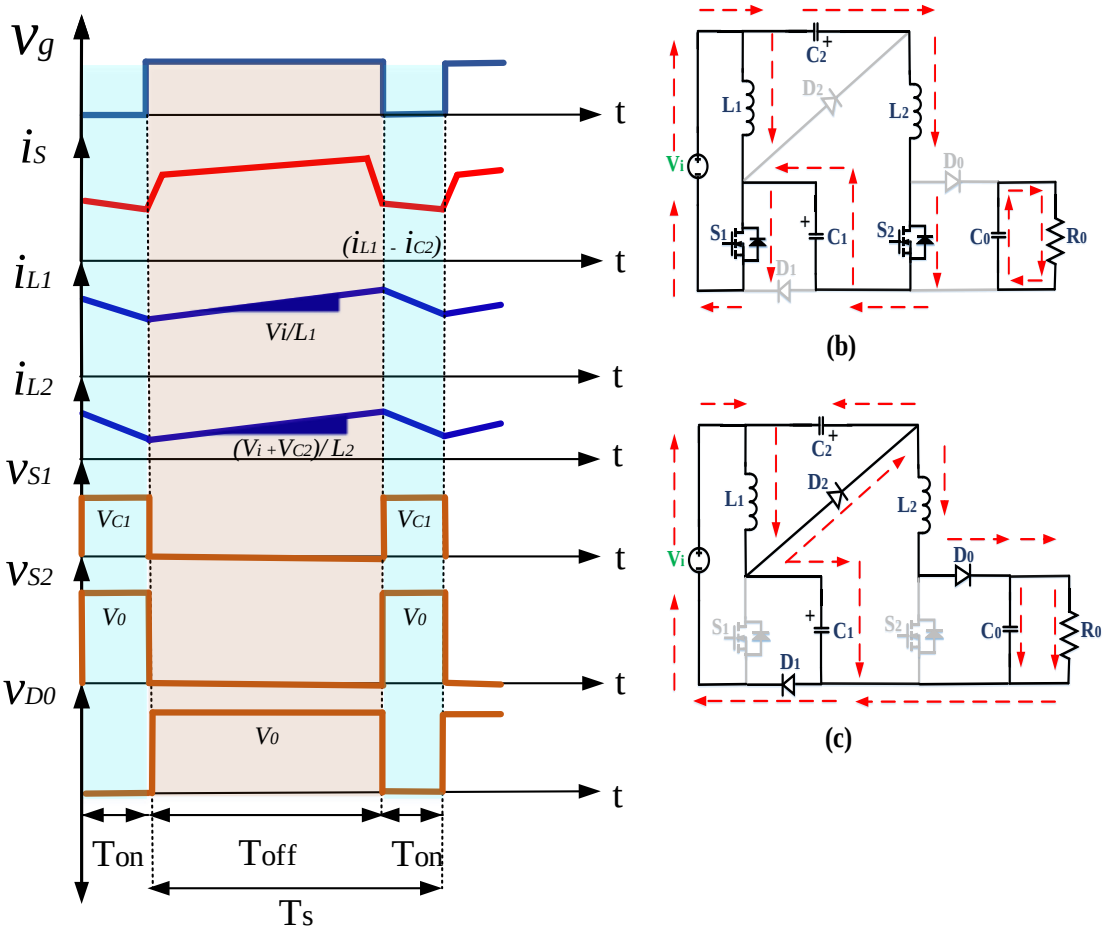


Figure 4.3. ASC-QBC-I converter (a) ideal wave forms (b) and (c) operating modes

The voltage profile of the two inductors is governed by the following equations

$$v_{L1}=V_i \tag{4.1}$$

$$v_{L2}=V_i+V_{C1}+V_{C2} \tag{4.2}$$

4.3.2 Operating State II ($t_1 \le t \le t_2$; $(1-D)T_S$)

This is the operating state in which both the switches at the instant t_1 are turned OFF as shown in Figure 4.3 (c). The source along with inductor L_1 charges the capacitor C_1 and the capacitor C_2 is charged by the inductor L_1. Since the diode D_0 has forward biased the source along with the two inductors powers the combination of capacitor C_0 and load R_0.

The voltage profile of the two inductors L_1 and L_2 is as follows

$$v_{L1}=V_i - V_{C1} \tag{4.3}$$

$$v_{L2}=V_i+V_{C2} - V_0 \tag{4.4}$$

For the instants t_0-t_1 and t_1-t_2, the volt-sec balance for the inductor L_1 is as follows

$$\int_{t_0}^{t_1} (V_i)\, dt + \int_{t_1}^{t_2} (V_i - V_{C1})\, dt \tag{4.5}$$

Simplifying the above expression

$$V_{C1}=\frac{V_i}{1-D} \tag{4.6}$$

Similarly, for the aforementioned time instants the volt-sec balance for inductor L_2 is written as

$$\int_{t_0}^{t_1}(V_i+V_{C1}+V_{C2})\,dt+\int_{t_1}^{t_2}(V_i+V_{C2}-V_0)\,dt \tag{4.7}$$

For the instants t_1-t_2,

$$V_{L1}=-V_{C2} \tag{4.8}$$

Using (4.8) in (4.3) the capacitor C_2 voltage is obtained as

$$V_{C2}=V_i\left(\frac{D}{1-D}\right) \tag{4.9}$$

Using (4.3), (4.6) in (4.4) the CCM voltage gain is written as

$$G_1\left(\frac{V_0}{V_i}\right)=\frac{1+D}{(1-D)^2} \tag{4.10}$$

4.3.3 Diode-Switch Voltage Stress Analysis

The blocking voltages will appear across semiconductor elements when the diodes are reverse biased and the switches are at turn OFF condition. Considering the aforementioned operating conditions and writing appropriate KVL equations for the suitable loops, the blocking voltages are specified as in Table 4.1.

Table 4.1 Diode-Switch Voltage Stress of ASCQBC-I Converter

Diodes			Switches	
V_{D0}	V_{D1}	V_{D2}	V_{S1}	V_{S2}
V_0	$\frac{V_i}{1-D}$	$\frac{V_i}{1-D}$	$\frac{V_i}{1-D}$	V_0

4.3.4 Diode-Switch Current Stress Analysis

The following current expressions are produced by using KCL for the two operating states of the ASC-QBC-I converter on individual capacitors.

$$\left.\begin{matrix} I_{C1\text{-}ON}=-I_{L2} \\ I_{C2\text{-}ON}=-I_{L2} \\ I_{C0\text{-}ON}=-I_0 \end{matrix}\right\} \quad \left.\begin{matrix} I_{C1\text{-}OFF}=\frac{I_{L1}-I_{L2}}{2} \\ I_{C2\text{-}OFF}=\frac{I_{L1}-I_{L2}}{2} \\ I_{C0\text{-}OFF}=I_{L2}-I_0 \end{matrix}\right\} \tag{4.11}$$

Since, the average current through the capacitor C_0 is zero,

$$(-I_0)D+(I_{L2}-I_0)(1-D)=0 \tag{4.12}$$

Rewriting the above expression, the inductor L_2 is written as

$$I_{L2}=\frac{I_0}{1-D} \tag{4.13}$$

By making the average current of capacitor C_1/C_2 equal to zero

$$(-I_{L2})D+\left(\frac{I_{L1}-I_{L2}}{2}\right)(1-D)=0$$

Rewriting the above expression, the inductor L_1 is written as

$$I_{L1}=\frac{I_{L2}\,(1+D)}{1-D} \tag{4.14}$$

Using (4.13) in (4.14), the current I_{L1} is expressed as

$$I_{L1}=\frac{I_0(1+D)}{(1-D)^2} \tag{4.15}$$

The peak current stress on the switch S_1 is obtained as

$$I_{S1}=I_{L1}-I_{C2\text{-}ON}$$

Using (4.11) and (4.15) in the above expression

$$I_{S1}=\frac{2\,I_0}{(1-D)^2} \tag{4.16}$$

Similarly, the current stress on switch S_2 is written as

$$I_{S2}=\frac{I_0}{1-D} \tag{4.17}$$

The semiconductor current stress is as shown in Table 4.2.

Table 4.2 Diode-Switch Current Stress of ASCQBC-I Converter

Diodes			Switches	
I_{D0}	I_{D1}	I_{D2}	I_{S1}	I_{S2}
$\frac{I_0}{1-D}$	$\frac{I_0}{(1-D)^2}$	$\frac{I_0}{(1-D)^2}$	$\frac{2\,I_0}{(1-D)^2}$	$\frac{I_0}{1-D}$

4.3.5 Parasitic parameters influence on voltage gain and efficiency

Each element in the power circuit of the proposed ASC-QBC-I converter contains some parasitics such as; capacitance with series ESR of r_C, inductors with series ESR of r_{LX} (x=1-2), semiconducting elements i.e., diodes with respective ESR of r_{DX} (X=0-2) and forward voltage drop of V_{FDX} (X=0-2), and for the switches during conducting period the parasitic element is a resistance r_S. By incorporating the parasitics of the respective elements into the ideal power circuit then the ASC-QBC-I converter is as shown in Figure 4.4.

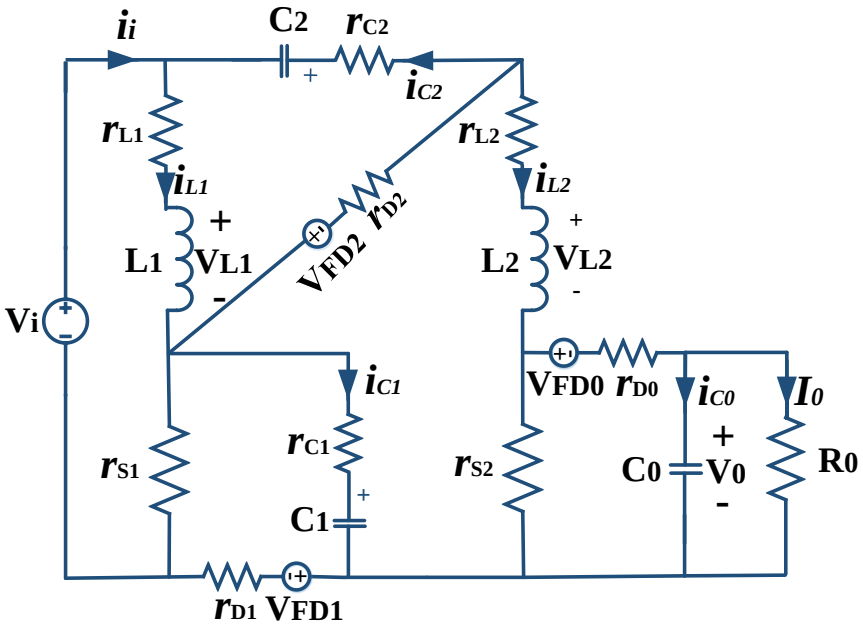
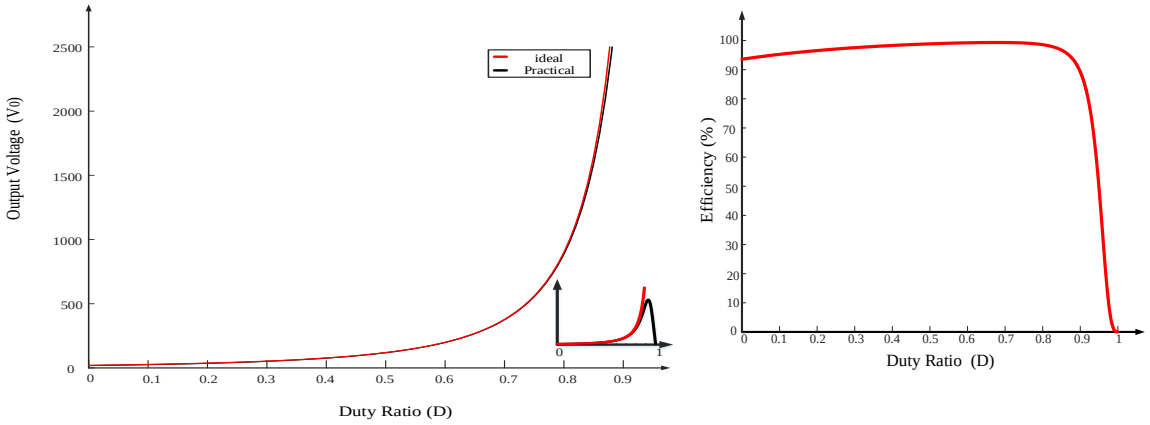


Figure 4.4. Equivalent circuit of ASC-QBC-I converter with element parasitics



(a) (b)

Figure 4.5. Parasitics influence on ASCQBC-I converter (a) output voltage and (b) efficiency

For the operating state 1 (with V_{L1} = -V_{C2}) and 2, the voltage of inductor L_2 in the presence of element parasitics can be expressed as

$$v_{L2}=V_i+V_{C1}+V_{C2}-I_{L2}r_{L2}-I_C(2r_C)-I_{S1}r_S-I_{S2}r_S \quad (4.18)$$

$$v_{L2}=V_i+V_{C2}-I_{L1}r_{L1}-I_{L2}(r_{L2}+r_{D0})-I_{D2}r_{D2}-(V_0+V_{FD0}+V_{FD1}) \quad (4.19)$$

Writing the volt-sec balance for inductor L_2 under the influence of element parasitics, the output voltage is as follows

$$V_0=\frac{V_i\left(\frac{1+D}{(1-D)^2}\right)-V_{FD0}-V_{FD1}}{1+\left(\frac{r_{D0}}{R_0}\right)+a_1\left(\frac{r_C}{R_0}\right)+b_1\left(\frac{r_{L1}}{R_0}\right)+c_1\left(\frac{r_S}{R_0}\right)+d_1\left(\frac{r_{L2}}{R_0}\right)+e_1\left(\frac{r_S}{R_0}\right)+\left(\frac{r_{D2}}{R_0}\right)} \quad (4.20)$$

Where

$$a_1=\frac{2D}{1-D} \quad b_1=\frac{1+D}{(1-D)^2} \quad c_1=\frac{D^2(1+D)}{(1-D)^3} \quad d_1=\frac{1}{(1-D)^2} \quad e_1=\frac{D}{(1-D)^2}$$

The plot of non ideal terminal voltage with the effect of element parasitics is shown in Figure 4.5 (a). Later in the experimental validation, we can observe that this non-ideal voltage gain is in good accord with the experimental voltage gain.

Using (4.20) the efficiency of ASC-QBC-I converter can be evaluated as

$$\eta=\frac{1-(V_{FD0}+V_{FD1})/V_{0\text{-}ideal}}{1+\left(\frac{r_{D0}}{R_0}\right)+a_1\left(\frac{r_C}{R_0}\right)+b_1\left(\frac{r_{L1}}{R_0}\right)+c_1\left(\frac{r_S}{R_0}\right)+d_1\left(\frac{r_{L2}}{R_0}\right)+e_1\left(\frac{r_S}{R_0}\right)+\left(\frac{r_{D2}}{R_0}\right)} \tag{4.21}$$

The schematic representation of efficiency versus duty ratio is shown in Figure.4.5 (b), in which the efficiency for the operating conditions of ASC-QBC-I converter is in good agreement with the experimental validation.

4.4 Analysis of ASCQBC-II Converter

The following discussion on performance indices of ASC-QBC-II is similar to that of ASC-QBC-I converter and the posture of capacitor C_3 is altered to reduce the input current ripple. The ideal operating waveforms of ASC-QBC-II converter are as shown in Figure. 4.6 (a).

4.4.1 Operating State I ($0 \le t \le t_1$; DT_S)

In this duration of time (DT_S), the switches (S_1, S_2) associated with the inductors are conducting as shown in Figure 4.6 (b). The inductors magnetization i.e., the voltage applied across them is similar to that of ASC-QBC-I converter. All the capacitors (C_1-C_4) are discharging except capacitor C_0, which along with load R_0 powered by the capacitor C_4.

The inductor voltage profile for state I is as follows

$$v_{L1}=V_i \tag{4.22}$$
$$v_{L2}=V_{C1}+V_{C3} \tag{4.23}$$

Since

$$V_{C1}=V_{C3}=V_C$$
$$v_{L2}=2V_C \tag{4.24}$$

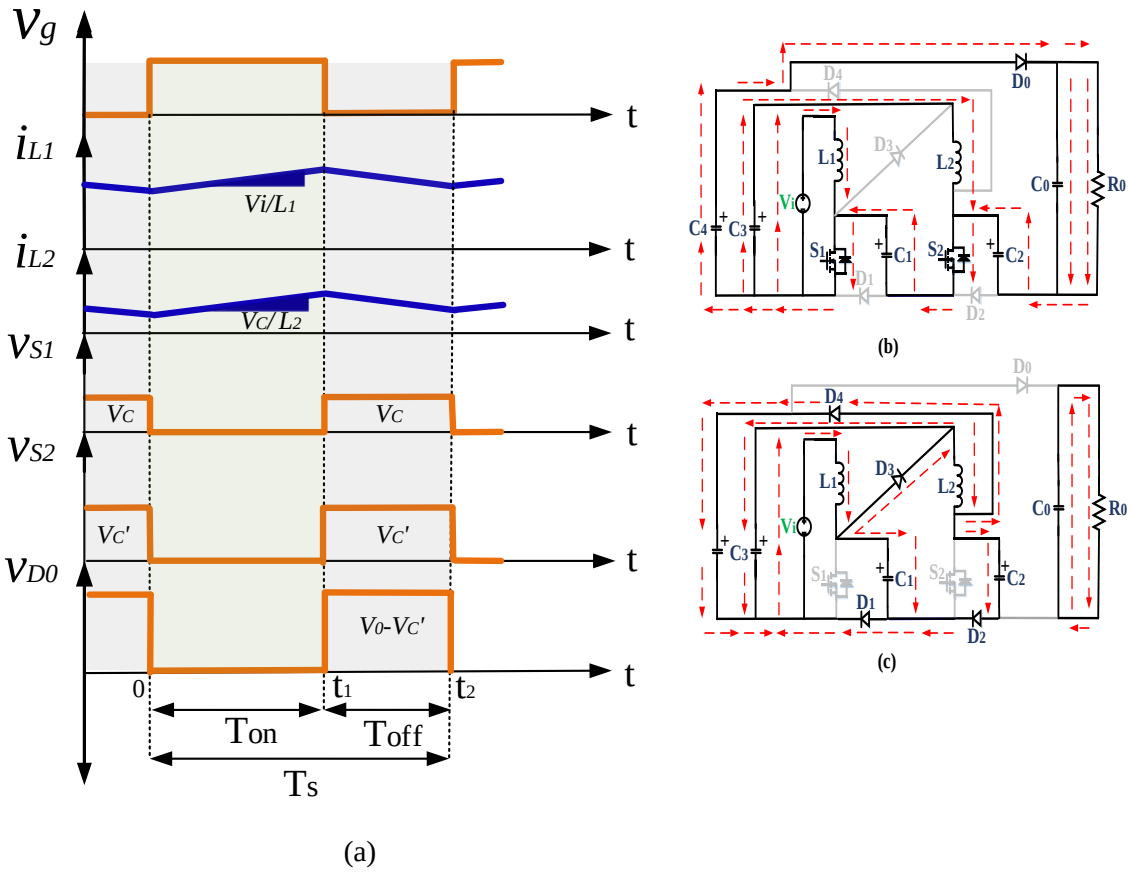


Figure 4.6. ASC-QBC-II converter (a) ideal wave forms (b) and (c) operating modes

4.4.2 Operating State II ($t_1 \le t \le t_2$; $(1\text{-}D)T_S$)

The operating state II corresponds to turn OFF condition of the switches (S_1, S_2) as shown in Figure 4.6 (c). The charging pattern of capacitor C_1 is similar to the previous converter, whereas the capacitor C_3 is charged by the combination of source (V_i) along with inductor L_1. In this stage II, the source (V_i) along with two inductors (L_1, L_2) charge the capacitors C_2 and C_4. Since the load end diode D_0 is reverse biased, capacitor C_0 powers the load (R_0).

The inductor voltages for operating state II are as follows

$$v_{L1} = V_i - V_{C1} \tag{4.25}$$

$$v_{L2} = V_{C3} - V_{C2} \tag{4.26}$$

The capacitors C_3 and C_4 voltages can be written as

$$V_{C3} = V_{C4} = V_C' \tag{4.27}$$

Applying the volt-sec balance for both the inductors L_1 and L_2 within the duration of t_0-t_2

For inductor L_1,

$$\int_{t_0}^{t_1} V_i\, dt + \int_{t_1}^{t_2} (V_i - V_C)\, dt = 0$$

Rewriting the above expression for the voltages of capacitors C_1 and C_3

$$V_{C1}=V_{C3}=V_C=\frac{V_i}{1-D} \tag{4.28}$$

For inductor L_2,

$$\int_{t_0}^{t_1} 2\, V_C\, dt + \int_{t_1}^{t_2} (V_C - V_C')\, dt = 0$$

By using the above expression, the capacitor C_2 and C_4 voltages are as follows

$$V_{C2}=V_{C4}=V_C'=\frac{V_i\,(1+D)}{(1-D)^2} \tag{4.29}$$

The duration t_0-t_1 in which the diode D_0 is conducting, the output voltage is expressed as

$$\begin{aligned} V_0&=V_{C1}+V_{C2}+V_{C2} \\ V_0&=V_C+2V_C' \end{aligned} \tag{4.30}$$

Using (4.28) and (4.29) in (4.30), the output voltage can be evaluated as

$$V_0=\frac{V_i\,(3+D)}{(1-D)^2} \tag{4.31}$$

The CCM voltage gain of ASC-QBC-II converter is as follows

$$G_2\left(\frac{V_0}{V_i}\right)=\frac{(3+D)}{(1-D)^2} \tag{4.32}$$

4.4.3 Diode-Switch Voltage Stress

The voltage stress of different elements in ASC-QBC-II converter can be evaluated by corresponding KVL equations for the suitable loops and as presented in Table 4.3.

Table 4.3 Diode-Switch Voltage Stress of ASCQBC-II Converter

Diodes					switches	
V_{D0}	V_{D1}	V_{D2}	V_{D3}	V_{D4}	V_{S1}	V_{S2}
$\frac{2\,V_i}{(1-D)^2}$	$\frac{V_i}{1-D}$	$\frac{V_i\,(1+D)}{(1-D)^2}$	$\frac{V_i}{1-D}$	$\frac{2\,V_i}{(1-D)^2}$	$\frac{V_i}{1-D}$	$\frac{V_i\,(1+D)}{(1-D)^2}$

4.4.4 Diode-Switch Current Stress

The approach for evaluating different element current stress is similar to that of the previous case and are represented as follows

Table 4.4 Diode-Switch Current Stress of ASCQBC-II Converter

Diodes					switches	
I_{D0}	I_{D1}	I_{D2}	I_{D3}	I_{D4}	I_{S1}	I_{S2}
$\frac{I_0}{D}$	$\frac{2\,I_0}{(1-D)^2}$	$\frac{I_0}{(1-D)}$	$\frac{2\,I_0}{(1-D)^2}$	$\frac{I_0}{(1-D)}$	$\frac{I_0\,(1+3D)}{D\,(1-D)^2}$	$\frac{I_0(1+D)}{D(1-D)}$

4.5 Control Performance

The proposed converters control performance for varying input voltage and load conditions is done by standard state space modelling. Since the ripple voltage and instantaneous current profile of capacitors C_1 and C_2 are identical, hence instead of these two state variables, only one is considered. The small signal model of ASC-QBC-I converter is represented by the following equations

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_C(t)}{dt} \\ \frac{d\hat{v}_{C0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d)}{L_1} & 0 \\ 0 & 0 & \frac{(1+d)}{L_2} & \frac{-(1-d)}{L_2} \\ \frac{(1-d)}{2C} & \frac{-(1+d)}{2C} & 0 & 0 \\ 0 & \frac{(1-d)}{C_0} & 0 & \frac{-1}{R_0 C_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_C(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_i(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} \\ \frac{-1}{2C} & \frac{-1}{2C} & 0 & 0 \\ 0 & \frac{-1}{C_0} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_C \\ V_{C0} \end{bmatrix} \hat{d} \quad (4.33)$$

$$v_0(t) = [0 \quad 0 \quad 0 \quad 1] [\hat{i}_{L1}(t) \quad \hat{i}_{L2}(t) \quad \hat{v}_C(t) \quad \hat{v}_{C0}(t)]^T \quad (4.34)$$

By using (4.33) and (4.34) the open loop control to output transfer function is written as

$$\left(\frac{\hat{v}_0(s)}{\hat{d}(s)} \Big/ \hat{v}_i(s)=0 \right) = \frac{-2.796\times10^{28}\, s^3 + 5.708\times10^{32}\, s^2 - 6.967\times10^{35}\, s + 6.895\times10^{39}}{2.909\times10^{24}\, s^4 + 1.818\times10^{35}\, s^3 + 4.455\times10^{31}\, s^2 + 2.765\times10^{32}\, s + 2.146\times10^{36}} \quad (4.35)$$

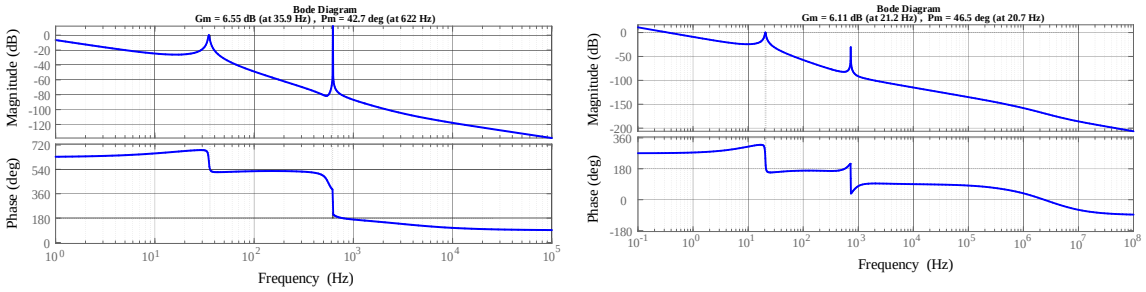
For the above-stated open loop transfer function the stable operation of the converter is achieved by using a single loop output voltage control as specified in (4.36) and bode plot for the corresponding closed-loop ASC-QBC-I converter is shown in Figure 4.7 (a).

$$G_C(s) = K_p + \frac{K_i}{s} \quad (4.36)$$

Where

$$\begin{cases} K_p = 0.0008 \\ K_i = 0.00092 \end{cases}$$

The invalid state variables of a loop that contains all capacitors in ASC-QBC-II converter are avoided by using a small resistance of r (0.01 Ω) in that loop. The small signal modelling of the aforementioned converter is as follows



(a) (b)

Figure 4.7. Bode plot for closed loop (a) ASCQBC-I and (b) ASCQBC-II

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{C1}(t)}{dt} \\ \frac{d\hat{v}_{C2}(t)}{dt} \\ \frac{d\hat{v}_{C3}(t)}{dt} \\ \frac{d\hat{v}_{C0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d)}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-r}{L_2} & \frac{1}{L_2} & \frac{-(1-d)}{L_2} & \frac{d}{L_2} & 0 \\ \frac{(1-d)}{C} & \frac{-1}{C} & \frac{-1}{Cr} & \frac{-2d}{Cr} & \frac{(1-d)}{Cr} & \frac{d(R_0-r)}{CR_0r} \\ 0 & \frac{(1-d)}{2C} & \frac{-d}{Cr} & \frac{-2d}{Cr} & 0 & \frac{d(R_0-r)}{CR_0r} \\ 0 & \frac{-d}{C} & \frac{(1-d)}{Cr} & 0 & \frac{-(1-d)}{Cr} & 0 \\ 0 & 0 & \frac{d}{Cr} & \frac{2d}{Cr} & 0 & -\left(\frac{d(R_0+r)}{CR_0r}+\frac{1-d}{C_0R_0}\right) \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C3}(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_i(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} & 0 \\ \frac{-1}{C} & 0 & 0 & \frac{-2}{Cr} & \frac{-1}{Cr} & \frac{R_0-r}{CR_0r} \\ 0 & \frac{-1}{2C} & \frac{-2}{Cr} & \frac{-2}{Cr} & \frac{-1}{Cr} & \frac{R_0-r}{CR_0r} \\ 0 & \frac{-1}{C} & \frac{-1}{Cr} & 0 & \frac{-1}{Cr} & 0 \\ 0 & 0 & \frac{1}{Cr} & \frac{2}{Cr} & 0 & \frac{-(R_0+r)}{CR_0r}+\frac{1}{C_0R_0} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C0} \end{bmatrix} \hat{d} \quad (4.37)$$

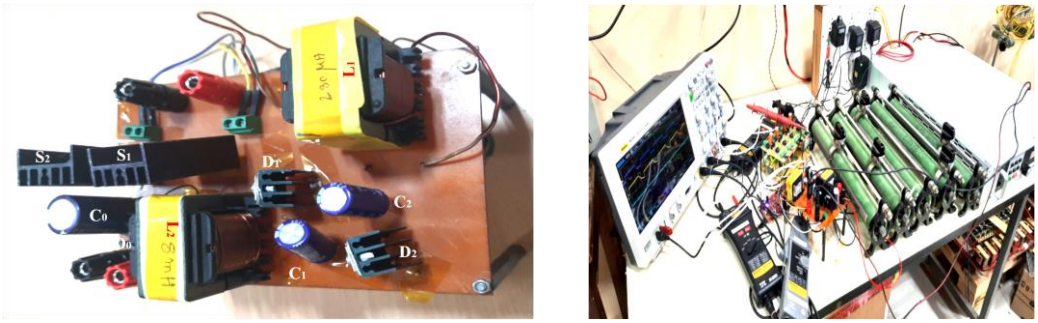
$$v_0(t)=[0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1][\hat{i}_{L1}(t) \quad \hat{i}_{L2}(t) \quad \hat{V}_{C1}(t) \quad \hat{V}_{C2}(t) \quad \hat{V}_{C3}(t) \quad \hat{V}_{C0}(t)]^T \quad (4.38)$$

By using the aforementioned small signal model of the ASC-QBC-II converter the open loop control to output transfer function is written as

$$\left(\frac{\hat{v}_0(s)}{\hat{d}(s)}/\hat{v}_i(s)=0\right)=\frac{2.714\times10^{58}\,s^5-6.416\times10^{65}\,s^4-2.696\times10^{72}\,s^3+4.316\times10^{75}\,s^2-3.298\times10^{79}\,s+2.558\times10^{83}}{1.379\times10^{55}\,s^6+1.652\times10^{62}\,s^5+3.617\times10^{68}\,s^4+6.079\times10^{69}\,s^3+7.652\times10^{75}\,s^2+3.315\times10^{76}\,s+1.278\times10^{80}} \quad (4.39)$$

A suitable PI controller with $K_p=0.00015$ and $K_i=0.0011$ is used to acquire stable output voltage against perturbations in input voltage and output load conditions. The closed loop bode plots for the ASC-QBC converters is shown in Figure 4.7.

4.6 Experimental Validation



(a) (b)

Figure 4.8. ASCQBC-I (a) prototype and (b) experimental setup

The theoretical analysis validation of ASC-QBC-I, II converters is done by fabricating the laboratory prototypes with the specifications mentioned in Table 4.5 and as shown in Figure 4.8 and 4.9. The applied input voltage for both the converters is 20 V for which the output voltages obtained are 391 V and 388 V as shown in Figure. 4.10 (a) and (g), attaining an ultra-

gain of 19.55 and 19.4 respectively. The average input current for both the converters observed to be 5.01 A and 5.05 A making the operating efficiencies 95% and 94% respectively.

(a) (b)

Figure 4.9. ASCQBC-II (a) prototype (b) experimental setup

The inductor currents of the ASC-QBC-I and II converters are as shown in Figure. 4.10 (b) and (h). since both the inductor currents are added in ASC-QBC-I to get the source current, the ripple content is high. Whereas, the source current passes through the inductor L_1 in the ASC-QBC-II converter and hence the ripple content is less. The switch current waveforms are as shown in Figure. 4.10 (c) and (i). The peak current stress for the switches S_1, S_2 in ASC-QBC-I observed to be 6.5 A, 1.5 A and that of ASC-QBC-II are 6.4 A, 1.4 A respectively.

The capacitor voltages of ASC-QBC-I, II are in good agreement with the ideal wave shapes as shown in Figure. 4.10 (d) and (j). The average value of these capacitor voltages is almost near to their ideal case, with a smaller variance in the experimental state.

The voltage stress of diodes (D_0-D_2) and switches (S_1-S_2) in ASC-QBC-I are 391 V for V_{D0}, V_{S2} and 70 V for V_{D1}, V_{D2}, V_{S2} as shown in Figure. 4.10 (e) and (f). Similarly, for the ASC-QBC-II converter the diode-switch voltage stresses are as follows; 220 V for V_{D0}, 45 V for V_{D1}, V_{D3}, 175 V for V_{D2}, 230 V for V_{D4}, Switch S_1 with 45 V and Switch S_2 at 180 V as shown in Fig. 4.10 (k) and (l).

The experimental validation of closed-loop performance is carried out for both the proposed converters at 100 W power rating with the aid of TMS320F28379D processor. The feasibility of stated converters to maintain a stiff output voltage at 400 V against the step variation of input voltage i.e., 20 V-25 V-20 V and 20 V-15 V-20 V is shown in Figures 4.11 (a) and (b) for ASC-QBC-I converter, and for ASC-QBC-II converter it is shown in Figures 4.11 (c) and (d). The perturbations of load are also taken into consideration by varying it from 75% to 100% as shown in Figures 4.11 (e) and (f) for the two converters respectively attaining a steady voltage of 400 V at the output terminals.

The theoretical losses are calculated by using thermal analysis on PSIM platform with the specifications of the selected devices for the proposed topologies. The theoretical and experimental efficiency variations for different load powers are plotted as shown in Figures 4.12 (a) and (b). The maximum efficiencies for both the proposed converters are 95.15 and 94.2% whereas the operating efficiencies for 100 W rating are 95% and 94% respectively. The various types of losses and their distribution at rated power of 100 W for the proposed converters are shown in the following Table 4.6. The loss distribution wheel for ASC-QBC- I, II as shown in Figures 4.13(a) and (b), where in ASC-QBC-I the majority portion of losses is due to switches (58%) and in ASC-QBC-II is due to diodes (49%). Moreover, the ideal findings validation of ASCQBC I and II converters is also demonstrated with the aid of simulated results as shown in Figure 4.14 and 4.15.

Table 4.5 Design Specifications

Specification	ASC-QBC-I	ASC-QBC-II
Power	100 W	100 W
Input voltage	20 V	20 V
Output Voltage	400 V	400 V
Inductors	L_1=280 μH, L_2=8 mH	L_1=400 μH, L_2=4.5 mH
capacitors	C_0=100 μF, C_1-C_2=22 μF	C_0=220 μF,C_1-C_4=22 μF

Table 4.6 Power loss distribution and comparison

Element	Loss	ASC-QBC-I		ASC-QBC-II	
		Theoretical (W)	Practical (W)	Theoretical (W)	Practical (W)
Inductor (ESR)	Conduction	0.67	0.876	1.12	1.388
Capacitor (ESR)	Conduction	0.058	0.038	0.058	0.0615
MOSFET (R_{DS} ON)	Conduction	1.1	1.655	0.485	0.6
MOSFET (Switching)	Switching Loss	1.07	1.27	0.89	1.009
Diodes (Internal Resistance)	Conduction	0.212	0.312	0.502	0.619
Diodes (Forward Drop)	Forward Drop Loss	0.68	0.883	1.785	2.385

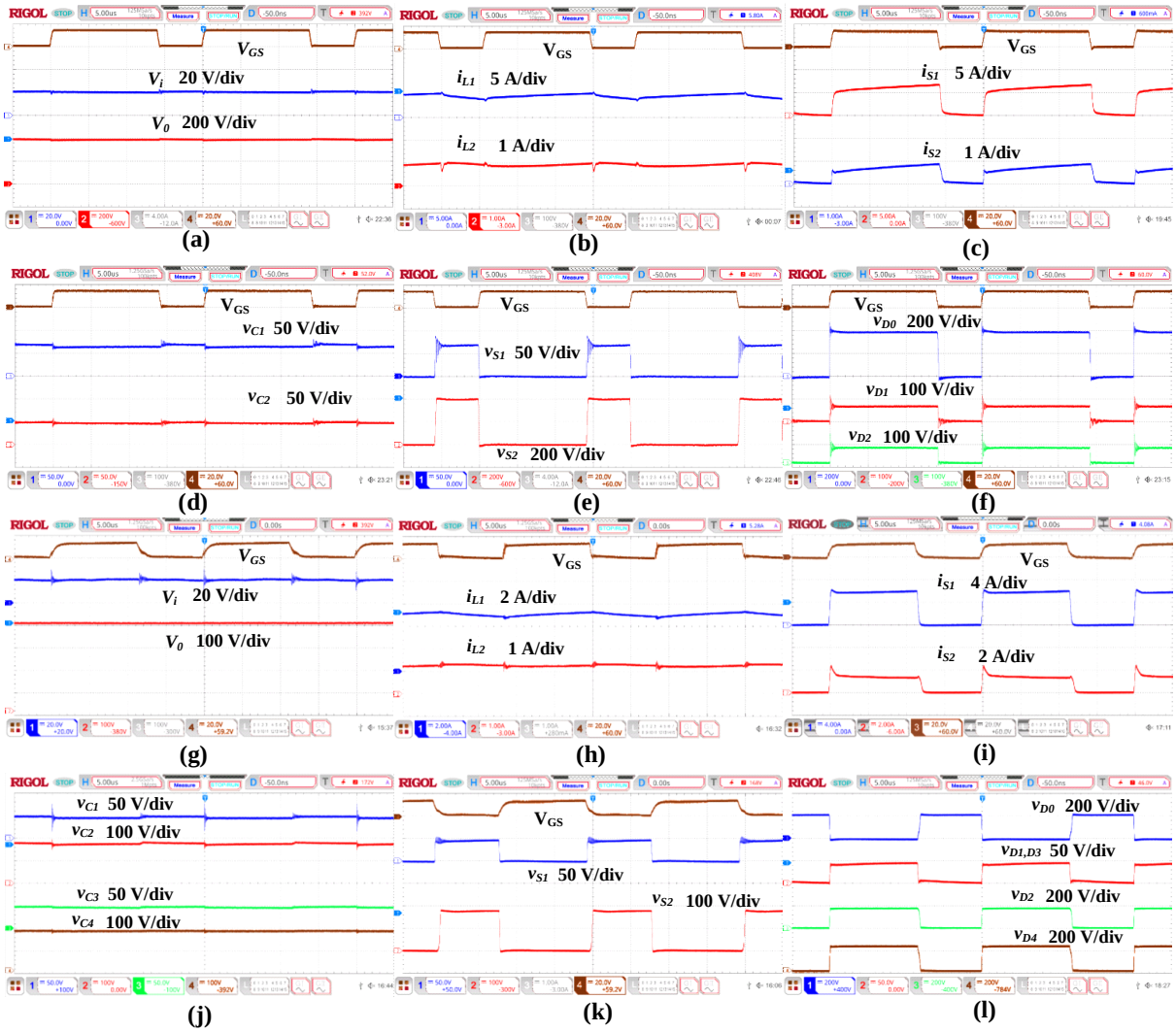
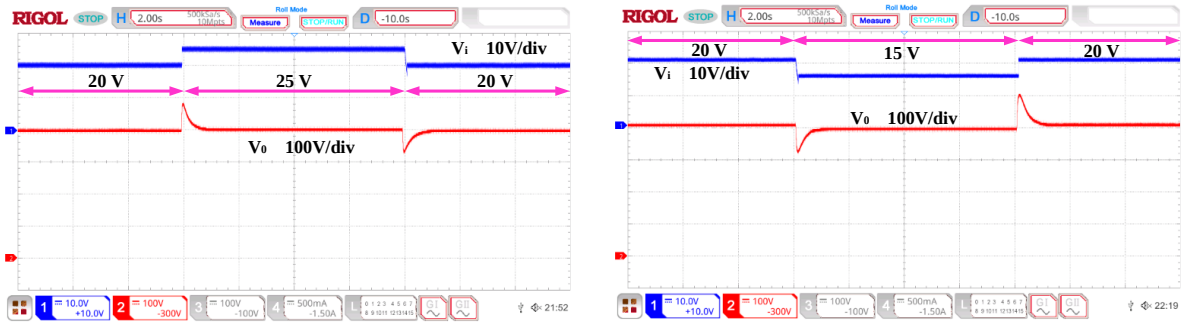


Figure 4.10. (ASC-QBC-I). (a) Input and output voltage (V_i & V_0) (b) Inductor currents (i_{L1} & i_{L2}) (c) Switch Currents (i_{S1} & i_{S2}) (d) Capacitor Voltages (V_{C1} & V_{C2}) (e) Switch Voltages (V_{S1} & V_{S2}) (f) Diode voltages ($V_{D0} – V_{D2}$); **(ASC-QBC-II).** (g) Input and output voltage (V_i & V_0) (h) Inductor currents (i_{L1} & i_{L2}) (i) Switch Currents (i_{S1} & i_{S2}) (j) Capacitor Voltages (V_{C1} - V_{C4}) (k) Switch Voltages (V_{S1} & V_{S2}) (l) Diode voltages ($V_{D0} – V_{D4}$)



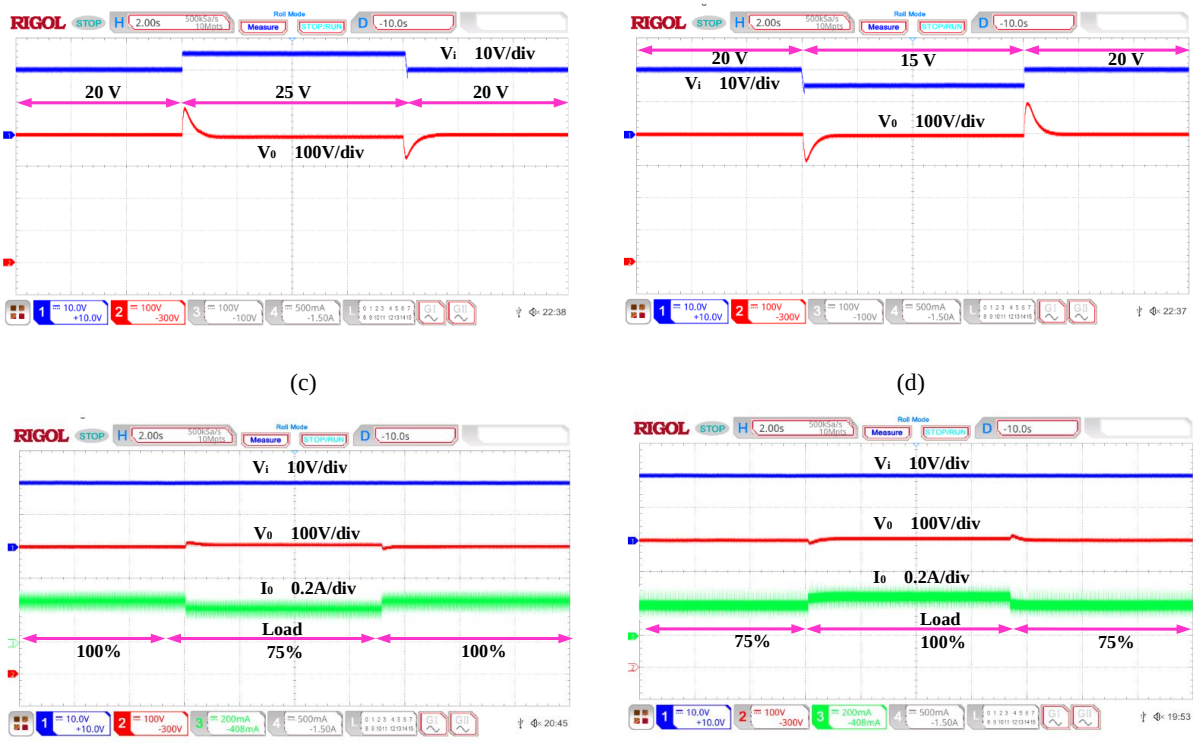


Figure 4.11. Closed loop performance of ASC-QBC-I converter for step variation in input voltage (a) 20 V- 25 V- 20 V (b) 20 V- 15 V- 20 V, ASC-QBC-II converter (c) 20 V- 25 V- 20 V (d) 20 V- 15 V- 20 V, step variations in load (e) ASCQBC-I (f) ASCQBC-II

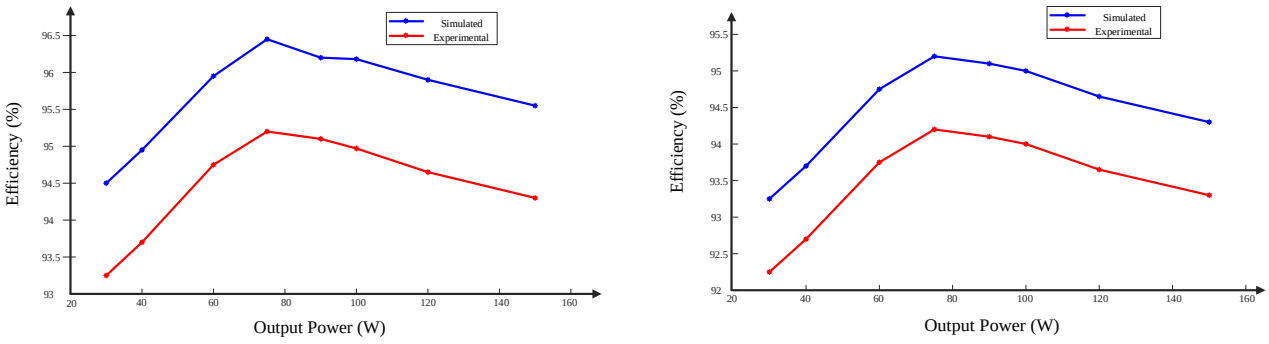


Figure 4.12. Efficiency versus output power (a) ASC-QBC-I and (b) ASCQBC-II

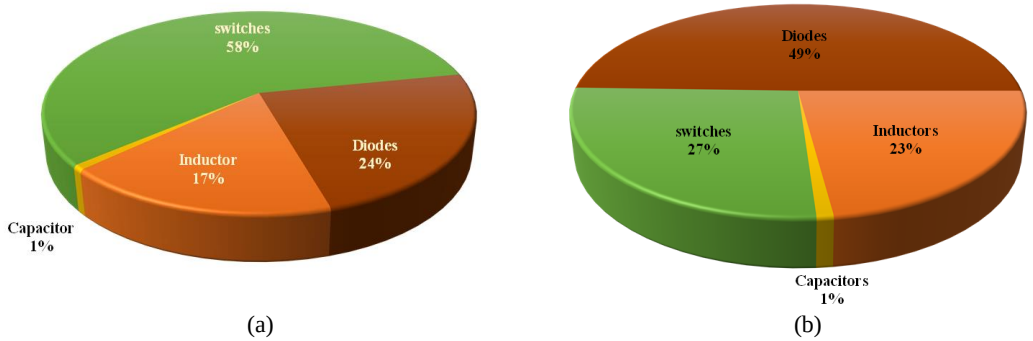


Figure 4.13. Loss distribution of (a) ASC-QBC-I and (b) ASCQBC-II

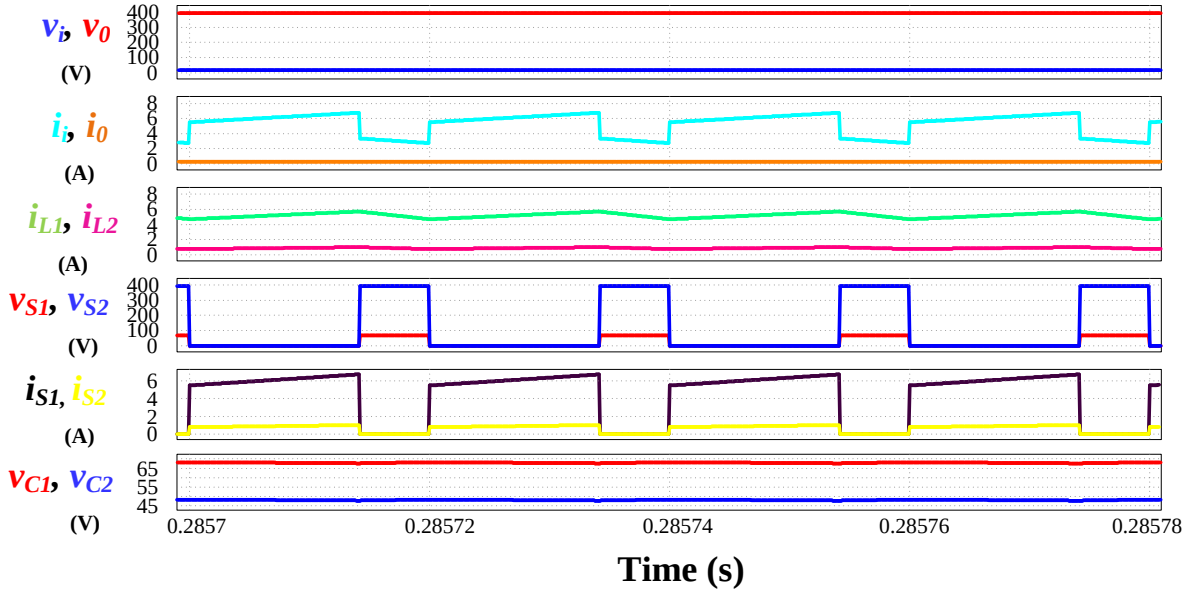


Figure 4.14. Simulated results of ASCQBC-I converter

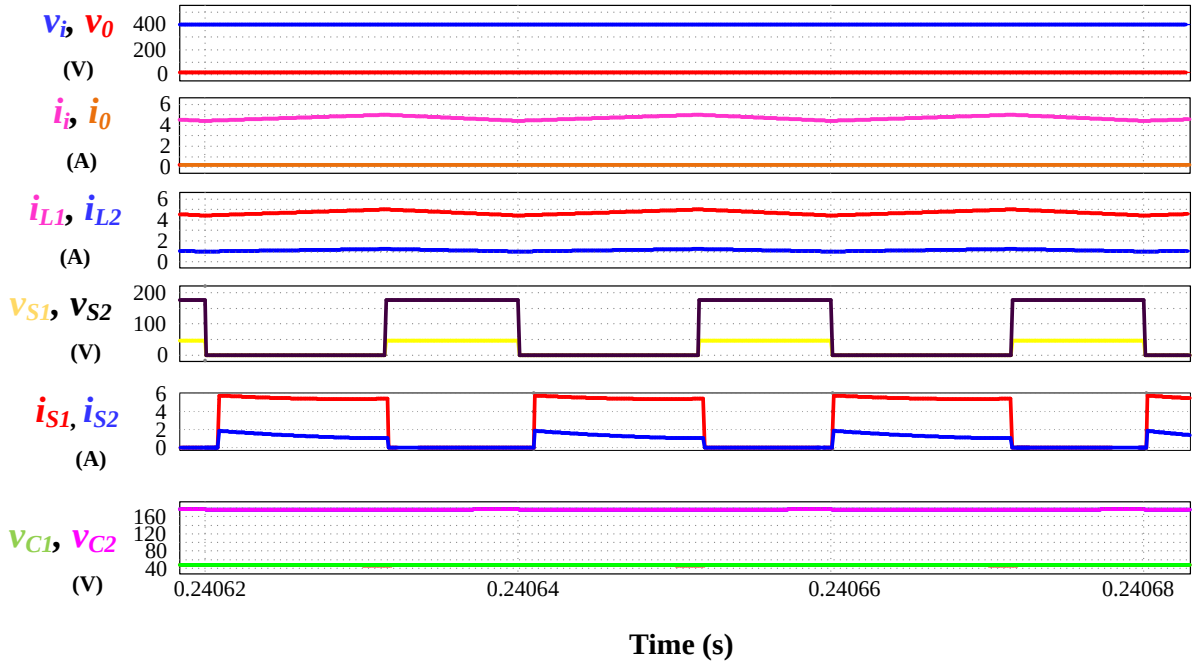


Figure 4.15. Simulated results of ASCQBC-II converter

4.7 Comparison of ASCQBC Converters with High Voltage Gain Converters

The superiority of the proposed converters can be verified by the performance indices i.e., voltage gain, semiconductor individual and total voltage stress, peak current stress on the switches and component count as shown in Table 4.7.

4.7.1 Voltage Gain

The voltage conversion factor is the prominent performance index in DC-DC converters. Hence, the comparison of different converter voltage gain concerning the variation in duty ratio is shown in Figure 4.16 (a). From the plot it is observed that the ASC-QBC-II converter has superior performance to all other converters and ASC-QBC-I voltage gain is slightly less compared to the converters in [89],[96]. The voltage gains of converters in [86],[87],[90],[91]-[94] is far less than with other converters. However, if we consider voltage gain per component count then ASC-QBC- I, II performance is superior to all other converters.

4.7.2 Element Voltage Stress

The element voltage stress is a crucial parameter for semiconductor element selection and inductor-capacitor design. This element voltage stress comparison is demonstrated in three different factors, normalized switch voltage stress (NSVS, $\sum v_S/v_0$), normalized diode voltage stress (NDVS, $\sum v_D/v_0$) and normalized total voltage standing (NTVS).

The NSVS of ASC-QBC-I is moderate as shown in Figure. 4.16 (b). This is because the switch at the load end has to block the entire output voltage. In this regard, the ASC-QBC-II performance is superior, with an NSVS of around 0.5. In comparison to ASC-QBC-II, the remaining converters will have high NSVS expect the converter in [89],[94].

The NDVS for ASC-QBC-I is the lowest among all, whereas ASC-QBC-II performance is moderate by having NDVS factor less than 2 as shown in Figure. 4.16 (c). It is interesting to note that even though the performance in NDVS and NSVS of ASC-QBC-I, II are not very much superior to other converters but when it comes to NTVS the proposed two converters performance is substantially improved from that of other converters, as shown in Figure. 4.16 (d).

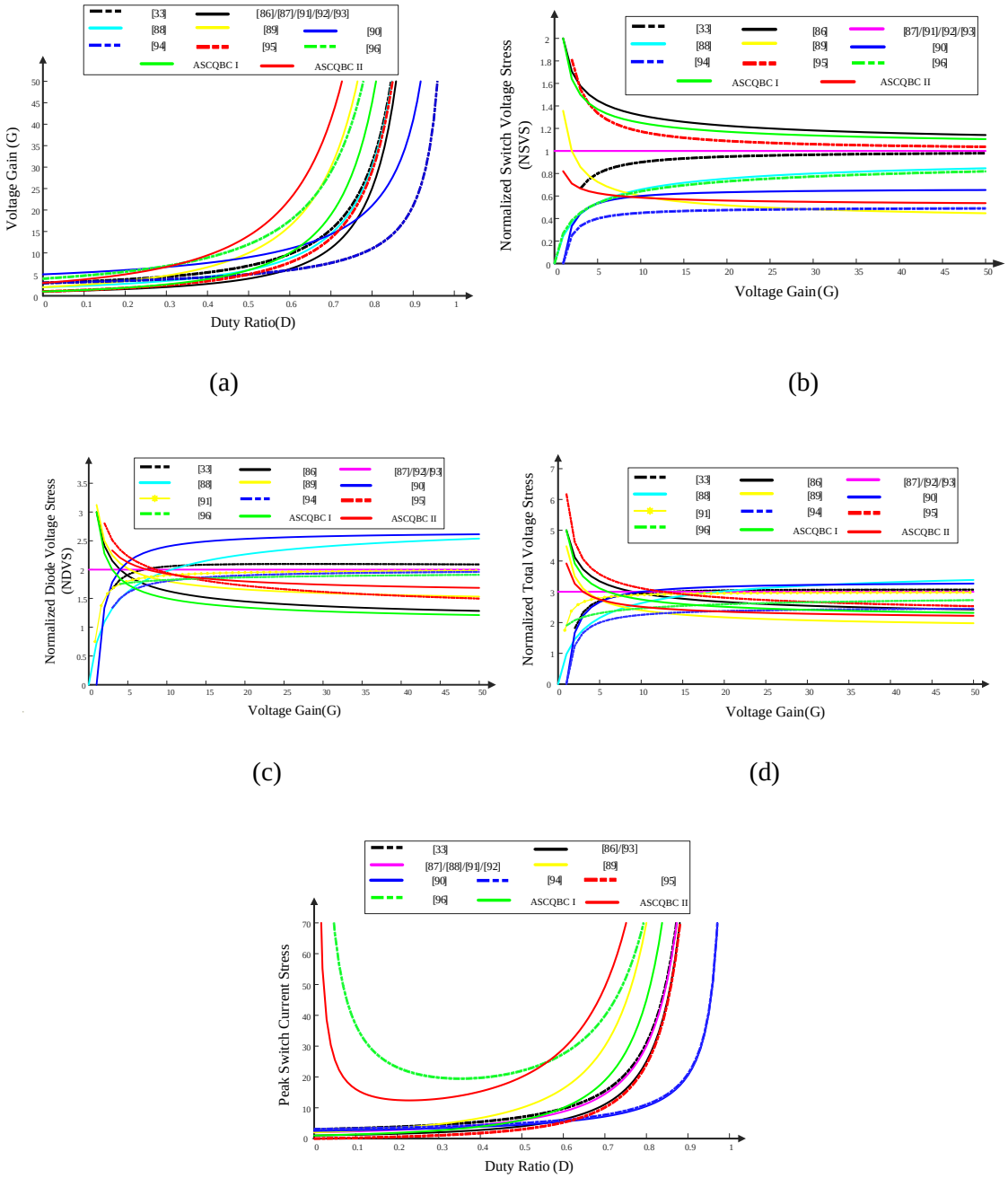


Figure 4.16. Performance comparison indices (a) voltage gain (b) NSVS (c) NDVS (d) NTVS (e) switch current stress

Table 4.7 Performance Comparison of ASCQBC Converters

Topology	Voltage Gain	Normalized Switch Voltage Stress	Normalized Diode Voltage Stress	Normalized Total Voltage Standing	η_{max} or $\eta_{operating}$	Common Ground	Input Current	Switch Current Stress	L/C/S/D (Total)
Ref [33]	$\frac{D^2-3D+3}{(1-D)^2}$	$\frac{2-D}{D^2-3D+3}$	$\frac{5-3D}{D^2-3D+3}$	$\frac{7-4D}{D^2-3D+3}$	96.7%	YES	Pulsating	$\frac{D^2-3D+3}{(1-D)^2}$	2/3/2/3 (10)
			$D=\frac{(2G-3)-\sqrt{4G-3}}{2(G-1)}$						
Ref [86]	$\frac{1}{(1-D)^2}$	$\frac{1+\sqrt{G}}{\sqrt{G}}$	$\frac{2+\sqrt{G}}{\sqrt{G}}$	$\frac{3+2\sqrt{G}}{\sqrt{G}}$	93%	YES	Pulsating	$\frac{1}{(1-D)^2}$	2/2/2/2 (8)
Ref [87]	$\frac{1}{(1-D)^2}$	1	2	3	92.5%	YES	Non Pulsating	$\frac{2-D}{(1-D)^2}$	2/2/1/3 (8)
Ref [88]	$\frac{2-D}{(1-D)^2}$	$\frac{1}{2-D}$	$\frac{3}{2-D}$	$\frac{4}{2-D}$	95%	YES	Pulsating	$\frac{2-D}{(1-D)^2}$	2/3/1/4 (10)
			$D=1-\frac{2}{G}-\sqrt{\frac{1}{4G^2}+\frac{1}{G}}$						
Ref [89]	$\frac{2+D}{(1-D)^2}$	$\frac{2G-1+\sqrt{1+12G}}{6G+1-\sqrt{1+12G}}$	$\frac{8G-1+\sqrt{1+12G}}{6G+1-\sqrt{1+12G}}$	$\frac{2(5G-1+\sqrt{1+12G})}{6G+1-\sqrt{1+12G}}$	95.22%	NO	Non Pulsating	$\frac{2+D}{(1-D)^2}$	3/6/2/5 (16)
Ref [90]	$\frac{5-D}{1-D}$	$\frac{2(G-1)}{3G}$	$\frac{8(G-1)}{3G}$	$\frac{10(G-1)}{3G}$	97.06%	YES	Pulsating	$\frac{5-D}{2(1-D)}$	3/5/2/4 (14)
Ref [91]	$\frac{1}{(1-D)^2}$	1	$2-\frac{1}{G}$	$3-\frac{1}{G}$	93%	YES	Pulsating	$\frac{2-D}{(1-D)^2}$	2/2/1/3 (8)
Ref [92]	$\frac{1}{(1-D)^2}$	1	2	3	93.11%	YES	Pulsating	$\frac{2-D}{(1-D)^2}$	2/2/1/3 (8)
Ref [93]	$\frac{1}{(1-D)^2}$	1	2	3	95.5%	YES	Pulsating	$\frac{1}{(1-D)^2}$	2/2/1/3 (8)
Ref [94]	$\frac{3-D}{1-D}$	$\frac{(G-1)}{2G}$	$\frac{4(G-1)}{2G}$	$\frac{5(G-1)}{2G}$	95.5%	YES	Pulsating	$\frac{3-D}{1-D}$	1/4/1/4 (10)
Ref [95]	$\frac{1+D-D^2}{(1-D)^2}$	$\frac{2-D}{1+D-D^2}$	$\frac{3-2D^2}{1+D-D^2}$	$\frac{5-D-2D^2}{1+D-D^2}$	93.7%	NO	Pulsating	$\frac{2D-D^2}{(1-D)^2}$	2/2/2/2 (8)
			$D=\frac{(2G+1)-\sqrt{8G+5}}{2(G+1)}$						
Ref [96]	$\frac{2(2-D)}{(1-D)^2}$	$\frac{2}{2(2-D)}$	$\frac{7-3D}{2(2-D)}$	$\frac{9-3D}{2(2-D)}$	94.5%	YES	Non Pulsating	$\frac{3-D^2}{D(1-D)^2}$	2/5/2/5 (14)
			$D=\frac{(2G-2)-\sqrt{8G+4}}{2G}$						
ASC-QBC-I	$\frac{1+D}{(1-D)^2}$	$\frac{2}{1+D}$	$\frac{3-D}{1+D}$	$\frac{5-D}{1+D}$	95%	NO	Pulsating	$\frac{1+D}{(1-D)^2}$	2/3/2/3 (10)
			$D=\frac{2G+1-\sqrt{8G+1}}{2G}$						
ASC-QBC-II	$\frac{3+D}{(1-D)^2}$	$\frac{2}{3+D}$	$\frac{7-D}{3+D}$	$\frac{9-D}{3+D}$	94%	NO	Non Pulsating	$\frac{1+3D}{D(1-D)^2}$	2/5/2/5 (14)
			$D=\frac{2G+1-\sqrt{16G+1}}{2G}$						

4.7.3 Element Current Stress

The peak switch current stress $(\hat{I}_s/I_0)$ with respect to output current as shown in Figure. 4.16 (e). For duty ratios greater than 0.6, the ASC-QBC-II converter will experience considerable current stress. This is the reason because of which the ASC-QBC-II converter is operated at a duty ratio of 0.577 in order to maintain a low current stress factor. The ASC-QBC-I converter current stress is moderate (at 20) with respect to the remaining converters.

4.7.4 Miscellaneous Performance Indices

The overall component count (10) is moderate for the converter ASC-QBC-I and for ASC-QBC-II, it is bit higher (14). This elevated component count can be justified by the fact that superiority in voltage gain at a low duty ratio. The only demerit of ASC-QBC-I, II is the lack of common ground between the source and the load. The ASC-QBC-II will have a very small amount of ripple current at the input terminals. The following Table 4.8 differentiates between the ASCQBC-I and II converters simulated and experimental findings.

Table 4.8 Performance comparison of simulation and experimental findings of ASCQBC-I and II

Performance Indices	**ASCQBC-1**		**ASCQBC-2**	
	Simulation	Experimental	Simulation	Experimental
Output voltage (V_0)	400 V	391 V	400 V	388 V
Output current (I_0)	0.25 A	0.23A	0.25 A	0.590 A
Input current (Ii)	4.86 A	5.01 A	5 A	5.05 A
Inductor currents (I_{L1} & I_{L2})	5 A & 0.84 A	6.5 A & 1.5 A	5 A & 1.2 A	6.4 A & 2.4 A
Switch voltage stresses ($\hat{V}_{S1}$ & $\hat{V}_{S2}$)	68 V& 393 V	70 V &391 V	40 V&181 V	45 V &180 V
Switch current stresses ($\hat{I}_{S1}$ & $\hat{I}_{S2}$)	6.4 A & 0.95 A	6.7 A & 0.9 A	6.92 A & 1.5 A	7.2 A & 2.4 A
Capacitor voltage stress	68 V & 48 V (C_1 & C_2)	65 V & 49 V (C_1 & C_2)	43 V & 181 V (C_1/C_3 & C_2/C_4)	45 V & 180 V (C_1/C_3 & C_2/C_4)

4.8 Summary

In this chapter, an active switched capacitor based ultra voltage gain quadratic boost converters have been presented. The theoretical steady-state analysis along with operating modes have been discussed. Moreover, to enlighten the merits of the proposed converters a comparative analysis with similar quadratic boost and other high voltage gain topologies was done. Furthermore, from the experimental validation, it is evident that the ASC-QBC- I and II converters assimilated numerous merits such as ultra-gain, low overall component stress, low input current ripple (ASC-QBC-II) and low current stress for the switches. The control performance of the converters with state space modelling was experimentally validated at a power rating of 100 W against the source voltage and load perturbations. As a proof of concept, a laboratory prototype was fabricated to validate the performance indices of the proposed converters.

Chapter 5

An Ultra High Gain Switched-Capacitor Boost DC-DC converter with Low Rear End Diode Voltage Stress and Reduced Ripple Current

5. An Ultra High Gain Switched-Capacitor Boost DC-DC converter with Low Rear End Diode Voltage Stress and Reduced Ripple Current

5.1 Introduction

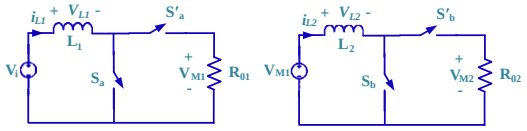
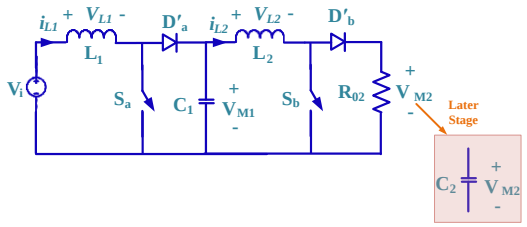
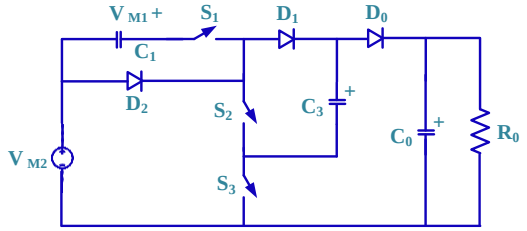
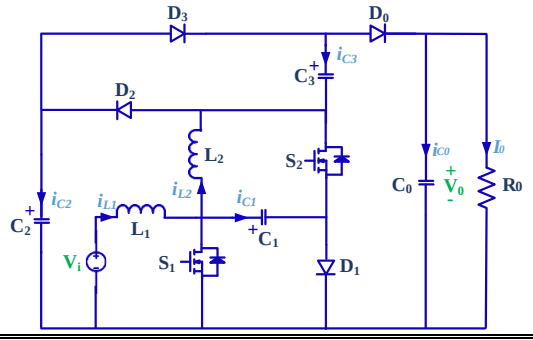
An ultra high gain quadratic boost converter based on switched-capacitor with low rear end diode voltage stress is proposed in this article. The ultra high gain is achieved with a low duty ratio and a wide range of flexibility. The proposed converter provides significantly reduced surface voltage stress and source current ripple. This article presents in detail discussion on the operating principle, continuous conduction mode (CCM) and, discontinuous conduction modes (DCM) and the parasitics effect on the output voltage and efficiency. Also, in this article performance comparison of stated converter with akin quadratic boost dc-dc converters is reported. The performance indices of the stated converter are verified by a prototype of 400 V, 50 kHz, 200 W, subsequently, the converter is also experimented for 800 V output with suitable elements to verify its performance feasibility for ultra voltage gain.

The chapter has the following organization: Section-5.2 comprises topological derivation, Section-5.3 describes of steady state operation and analysis, Section-5.4 presents effect of element parasitics, Section 5.5 emphasizes design aspects. Section-5.6 discusses the control performance, Section-5.7 presents the experimental validation, Section-5.8 gives insight into the comparison with similar converters and the summary is presented in Section 5.9.

5.2 Topological Derivation

A three-stage cascade connection is used to derive the proposed topology i.e., boost stage 1, boost stage 2 and switched capacitor voltage lift stage as shown in Table I. The boost stage 1 and 2 loads are assumed to be R_{01} and R_{02}. Further in cascading these loads are replaced by respective capacitors (C_i) followed by their voltages (V_{Mi}). The third stage i.e., voltage lift stage can be integrated with in stage 1 and stage 2 because it uses internal switches of aforementioned stages in charging process. Here, capacitor C_2 posture in the final derived topology is altered in such a way that the total input current passes through the inductor L_1 as a result its ripple content is low.

Table 5.1 Synthesis of Proposed Switched Capacitor based Quadratic Boost DC-DC Converter (SCQBC)

Step	Methodology	Analysis
1	Preferred voltage gain is restructured in single inductor converters (SIC) and voltage lift stage to create a cascade form	$V_0=\frac{3\text{-}D}{(1\text{-}D)^2}\ V_i=\underbrace{\left\{\frac{1}{1\text{-}D}\right\}\left\{\frac{1}{1\text{-}D}\right\}}_{\frac{1}{f_D'(D)}\rightarrow SIC\ form}\ \underbrace{\{3\text{-}D\}}_{\frac{f_N'(D)}{1}\rightarrow Voltage\ lift\ stage}$ $V_{M1}=\left(\frac{1}{1\text{-}D}\right)V_i \xleftrightarrow{Cascade\ Connection} V_{M2}=\left(\frac{1}{1\text{-}D}\right)V_{M1}$
2	Individual stage voltage gains are decomposed to obtain volt-sec balance equations. There by inductor voltages are obtained in each switching sub interval of operation.	$V_i(DT_s)+((1\text{-}D)T_s)\ (V_i\text{-}V_{M1})=0$ $v_{L1}/DT_s=V_i$ $V_{M1}(DT_s)+((1\text{-}D)T_s)\ (V_{M1}\text{-}V_{M2})=0$ $v_{L2}/DT_s=V_{M1}$
3	Synthesize the equivalent sub-circuits of SIC's as represented in [97] and [98]	 $\begin{Bmatrix} S_a,S_b\rightarrow DT_s \\ S'_a,S'_b\rightarrow (1\text{-}D)T_s \end{Bmatrix}$
4	Merge the individual SIC's voltage loops by considering the previous stage output as input next stage. Here the load $R_{0,1}$ is replaced by a capacitor C_1 and the switches S'_a and S'_b are replaced by diodes.	
5	Synthesize the voltage lift stage i.e., the final stage by considering V_{M1} and V_{M2} as the voltages across the respective capacitors in step-4.	 $\begin{Bmatrix} S_1,S_3 and\ D_1\rightarrow DT_s\rightarrow V_{C3}=V_{M1}+V_{M2} \\ D_0,D_2 and\ S_2\rightarrow (1\text{-}D)T_s\rightarrow V_0=V_{M1}+2V_{M2}=\frac{3\text{-}D}{(1\text{-}D)^2}\ V_i \end{Bmatrix}$
6	Integrate all the individual sub-circuits to construct the overall cascade form. Here $R_{0,2}$ is replaced by a capacitor C_2, and the positions of C_1 and D'_a are interchanged for better synthesis of the proposed topology. The switches and diodes in voltage lift stage are also optimized to get the same outcome as shown in step-5.	

5.3 Steady State CCM Operation and Analysis

The CCM operation comprises two modes i.e., mode 1 and 2 depending on the switching instants (t_0 and t_1) of S_1 and S_2, and the key waveforms are as shown in Figure 5.1 (a).

5.3.1 Mode I of Operation

The SCQBC converter mode 1 of operation is initiated at instant t_0 as shown in Figure 5.1 (b), when a gate pulse is applied to both switches. The applied voltage across inductor L_1 is V_i, that of inductor L_2 and capacitor C_3 is V_{C1}, $V_{C1}+V_{C2}$.

The reverse biased diode D_0 makes the load R_0 to be powered by capacitor C_0. Hence, V_{L1} and V_{L2} are expressed as

$$v_{L1}=V_i \; ; \; v_{L2}=V_{C1} \tag{5.1}$$

5.3.2 Mode II of Operation

This mode of operation is initiated upon the withdrawal of gate pulse for the two switches at instant t_1. The inductor L_1 along with source V_i charges the capacitors C_1. Since the diode D_0 is conducting, the two inductors along with the source and capacitor C_3 powers load R_0 as well as capacitor C_0. The inductor voltage profile is expressed as

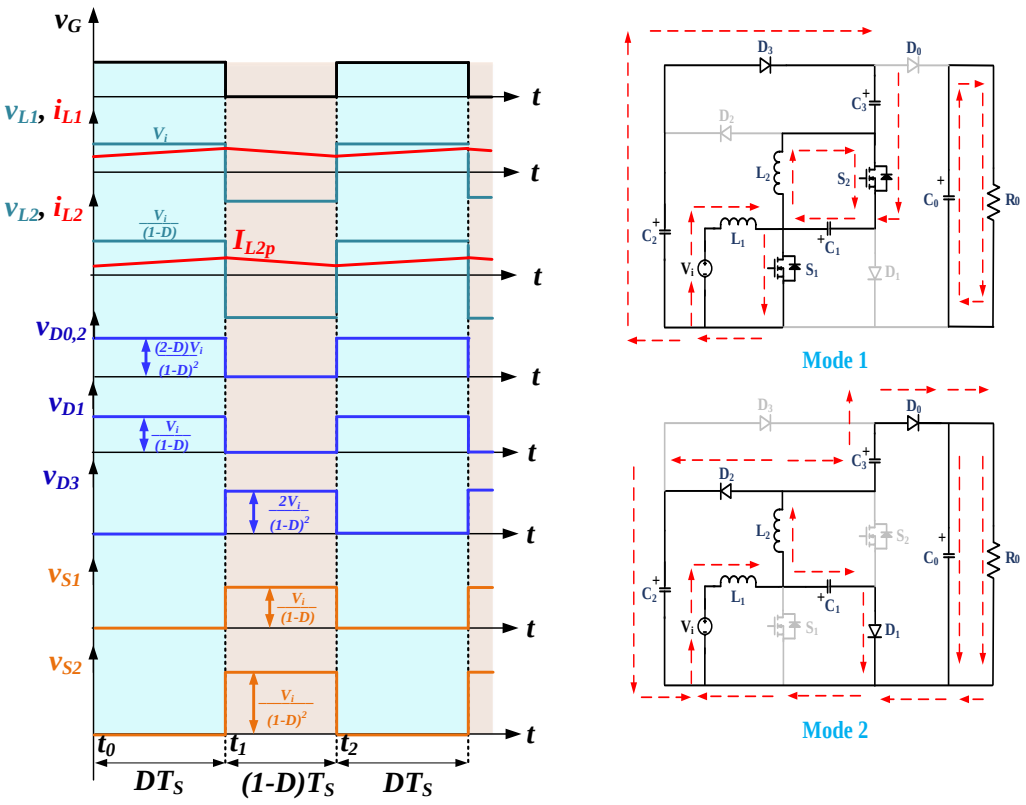
$$v_{L1}=V_i-V_{C1} \; ; \; v_{L2}=V_{C1}+V_{C3}-V_0 \tag{5.2}$$

Using (5.1) and (5.2) for the inductors L_1 and L_2 volt-sec balance, the voltages of three capacitors are as follows

$$V_{C1}=\frac{V_i}{1-D}, \; V_{C2}=\frac{V_i}{(1-D)^2}; \; V_{C3}=\frac{V_i\,(2-D)}{(1-D)^2} \tag{5.3}$$

Using (5.1) to (5.3) the step-up voltage gain is as follows

$$G_{CCM}\left(\frac{V_0}{V_i}\right)=\frac{3-D}{(1-D)^2} \tag{5.4}$$



(a) (b)

Figure 5.1. SCQBC converter's CCM (a) ideal operating waveforms and (b) modes of operation.

5.4 Effect of Element Parasitics

The proposed converter semiconductor and energy storage elements are considered with the respective parasitic parameters i.e., the capacitors and inductors now consist of equivalent series resistance (ESR), diodes have resembled with series connection of forward voltage drop and its internal resistance, and the switches are replaced with its on-state resistance as shown in Figure 5.2 for the following analysis in terms of output voltage and efficiency. To evaluate V_0 of SCQBC converter, a similar analysis as in the case of CCM operation is carried out for the inductor's voltages (with the same operating conditions that are considered for CCM operation), which is as follows

$$V_0=\frac{V_i\left(\frac{3-D}{(1-D)^2}\right)-V_{D1}\left(\frac{3-D}{1-D}\right)}{1+a\left(\frac{r_{L1}}{R_0}\right)+b\left(\frac{r_S}{R_0}\right)+c\left(\frac{r_C+r_{D1}}{R_0}\right)} \tag{5.5}$$

Where

$$a=b=\frac{(3-D)^2}{(1-D)^4} \quad c=\frac{2D\ (3-D)}{(1-D)^3}$$

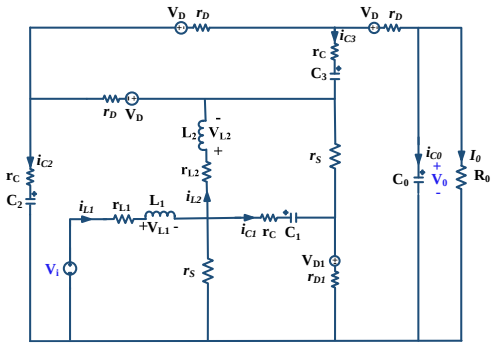


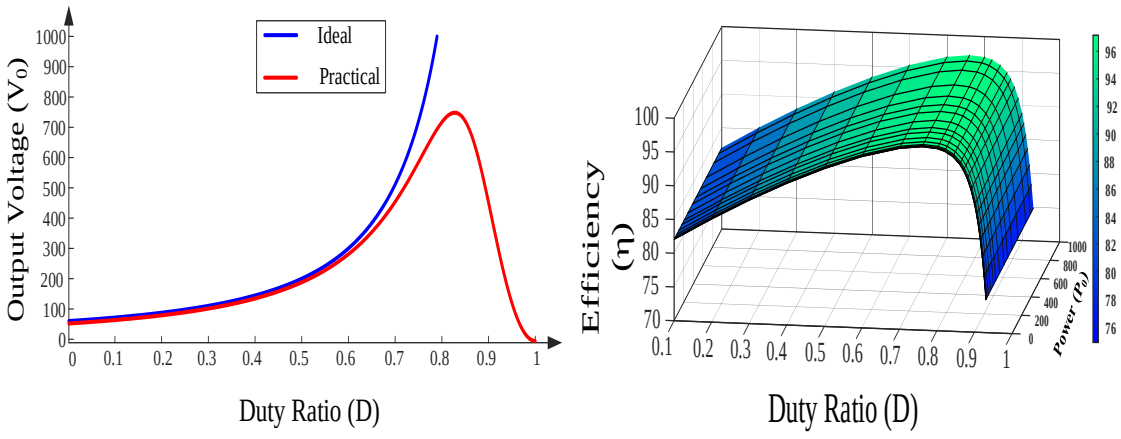
Figure 5.2. SCQBC equivalent circuit with element parasitics.

The plot representing converter terminal voltage V_0 is shown in Figure 5.3 (a) (at V_i=*20 V)*, in which voltage V_0 tends to zero as the duty nears unity.

Using (5.5) the efficiency of SCQBC converter with element parasitics is evaluated as

$$\eta = \frac{1-\frac{V_{D1}}{V_i}(1-D)}{1+a\left(\frac{r_{L1}}{R_0}\right)+b\left(\frac{r_S}{R_0}\right)+c\left(\frac{r_C+r_{D1}}{R_0}\right)} \tag{5.6}$$

The switching losses must be deducted from the above expression to include this portion of losses. The variation of efficiency, output power, versus duty ratio plots are shown in Figure. 5.3 (b).



(a) (b)

Figure 5.3. SCQBC converter (a) V_0 versus D and (b) 3-D plot of efficiency, power versus duty ratio with element parasitics.

5.5 Design Specifications

A ripple content between 20% to 40% of the average currents is opted to design the inductors. The inductor L_2 is designed for an upper limit in the ripple current (40%) so that its size is effectively reduced. Similarly, the design of capacitors is opted a ripple content of less than 5% of their steady-state voltages.

The design constraints for energy storage elements are as stated below.

$$\left.\begin{array}{l} L_1 \geq \dfrac{V_i\, D}{(0.2\, I_{L1}) f_s} \\ L_2 \geq \dfrac{V_{C1}\, D}{(0.4\, I_{L2}) f_s} \end{array}\right\} \quad \left.\begin{array}{l} (C_X) \geq \dfrac{I_{C1off}\, D}{(0.05\, V_{CX}) f_s},\ X=1\text{-}3 \\ C_0 \geq \dfrac{I_0\, D}{(0.05\, V_0) f_s} \end{array}\right\} \tag{5.7}$$

Where

$$I_{L1} = \frac{I_o(3\text{-}D)}{(1\text{-}D)^2}, I_{L2} = \frac{2I_o}{1\text{-}D}, I_{C1off} = I_{L1} - I_{L2} \Bigg\}$$

5.6 Control Performance

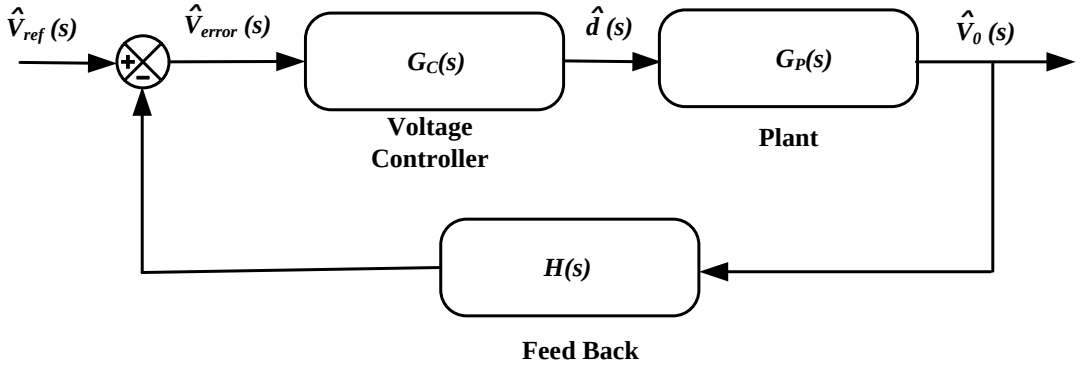


Figure 5.4. Single loop voltage control scheme for SCQBC converter

The proposed converter is designed with a system of single loop voltage control with feedback *H(s)* as shown in Figure. 5.4. It can be observed from the Figure. 5.4 that $G_P(s)$ represents the plant or the proposed converter preceding by a voltage controller $G_C(s)$ to obtain stable output voltage against perturbation in load current and source voltage. The control performance of SCQBC converter is evaluated by standard small signal modeling. The converter voltage variables are $v_i(t)$ and $v_0(t)$, the control variable is $d(t)$, and the state variables for inductors (L_1 and L_2) and capacitors (C_1, C_2, and C_3) are $i_{L1}(t)$, $i_{L2}(t)$, $v_{c1}(t)$, $v_{c2}(t)$ and $v_{c3}(t)$ respectively.

The SCQBC converter state equations for the durations *DTs* and *(1-D)Ts* with the assumption of each capacitor has an ESR are written as

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{Cr} & \frac{-1}{Cr} & \frac{1}{Cr} & 0 \\ 0 & 0 & \frac{1}{Cr} & \frac{1}{Cr} & \frac{-1}{Cr} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_0 C_0} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i(t) \tag{5.8}$$

$$v_{c0}(t) = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1][i_{L1}(t) \quad i_{L2}(t) \quad v_{c1}(t) \quad v_{c2}(t) \quad v_{c3}(t) \quad v_{c0}(t)]^T$$

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ \frac{1}{C} & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & \frac{-1}{Cr} & \frac{-1}{Cr} & \frac{1}{Cr} \\ 0 & 0 & 0 & \frac{-1}{Cr} & \frac{-1}{Cr} & \frac{1}{Cr} \\ 0 & 0 & 0 & \frac{1}{C_0 r} & \frac{1}{C_0 r} & -\left(\frac{R_0+r}{C_0 r R_0}\right) \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i(t) \qquad (5.9)$$

$$v_{c0}(t) = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1][i_{L1}(t) \quad i_{L2}(t) \quad v_{c1}(t) \quad v_{c2}(t) \quad v_{c3}(t) \quad v_{c0}(t)]^T$$

Using (5.8) and (5.9), average state equation of the SCQBC converter is written as

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d(t))}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{-(1-2d(t))}{L_2} & \frac{(1-d(t))}{L_2} & 0 & 0 \\ \frac{1-d(t)}{C} & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-d(t)}{C} & \frac{-d(t)}{Cr} & \frac{-1}{Cr} & \frac{-(1-2d(t))}{Cr} & \frac{(1-d(t))}{Cr} \\ 0 & 0 & \frac{d(t)}{Cr} & \frac{-(1-2d(t))}{Cr} & \frac{-1}{Cr} & \frac{(1-d(t))}{Cr} \\ 0 & 0 & 0 & \frac{(1-d(t))}{C_0 r} & \frac{(1-d(t))}{C_0 r} & \frac{-(1-(1-r)d(t))}{C_0 r R_0} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i(t) \qquad (5.10)$$

$$v_{c0}(t) = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1][i_{L1}(t) \quad i_{L2}(t) \quad v_{c1}(t) \quad v_{c2}(t) \quad v_{c3}(t) \quad v_{c0}(t)]^T$$

Assuming small signal perturbations are applied to the converter and with the aid of steady-state and small signal variables the SCQBC converter small signal model is obtained as in (5.11).

The open loop duty to output voltage (V_0) transfer function of the proposed converter is expressed in (5.12) assuming the perturbations at the input side are zero. The PI controller is used to acquire a stiff voltage V_0 concerning the aforementioned perturbances. The SCQBC converter bode plot with stable closed loop operation is shown in Figure 5.5.

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{c1}(t)}{dt} \\ \frac{d\hat{v}_{c2}(t)}{dt} \\ \frac{d\hat{v}_{c3}(t)}{dt} \\ \frac{d\hat{v}_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d)}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{-(1-2d)}{L_2} & \frac{(1-d)}{L_2} & 0 & 0 \\ \frac{1-d}{C} & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-d}{C} & \frac{-d}{Cr} & \frac{-1}{Cr} & \frac{-(1-2d)}{Cr} & \frac{(1-d)}{Cr} \\ 0 & 0 & \frac{d}{Cr} & \frac{-(1-2d)}{Cr} & \frac{-1}{Cr} & \frac{(1-d)}{Cr} \\ 0 & 0 & 0 & \frac{(1-d)}{C_0 r} & \frac{(1-d)}{C_0 r} & \frac{-(1-(1-r)d)}{C_0 r R_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{c1}(t) \\ \hat{v}_{c2}(t) \\ \hat{v}_{c3}(t) \\ \hat{v}_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_i(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{2}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ \frac{-1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C} & \frac{-1}{Cr} & 0 & \frac{2}{Cr} & \frac{-1}{Cr} \\ 0 & 0 & \frac{1}{Cr} & \frac{2}{Cr} & 0 & \frac{-1}{Cr} \\ 0 & 0 & 0 & \frac{-1}{C_0 r} & \frac{-1}{C_0 r} & \frac{-1}{R_0 C_0} + \left(\frac{R_0+r}{C_0 r R_0}\right) \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C0} \end{bmatrix} \hat{d}(t) \qquad (5.11)$$

$$\left(\frac{\hat{v}_0(s)}{\hat{d}(s)} \Big/ \hat{v}_i(s)=0 \right) = \frac{-4.983\times10^{56}\, s^5 - 4.53\times10^{63}\, s^4 - 9.224\times10^{69}\, s^3 + 2.639\times10^{74}\, s^2 - 1.785\times10^{78}\, s + 2.348\times10^{82}}{3.405\times10^{52}\, s^6 + 3.212\times10^{59}\, s^5 + 7.209\times10^{65}\, s^4 + 4.543\times10^{67}\, s^3 + 8.245\times10^{73}\, s^2 + 9.772\times10^{74}\, s + 1.802\times10^{79}} \qquad (5.12)$$

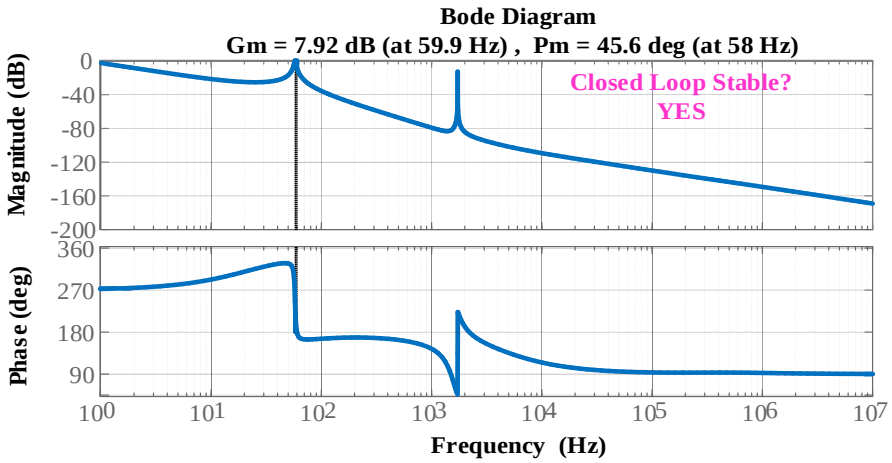


Figure 5.5. Closed loop bode plot of SCQBC converter.

5.7 Simulation and Experimental Results

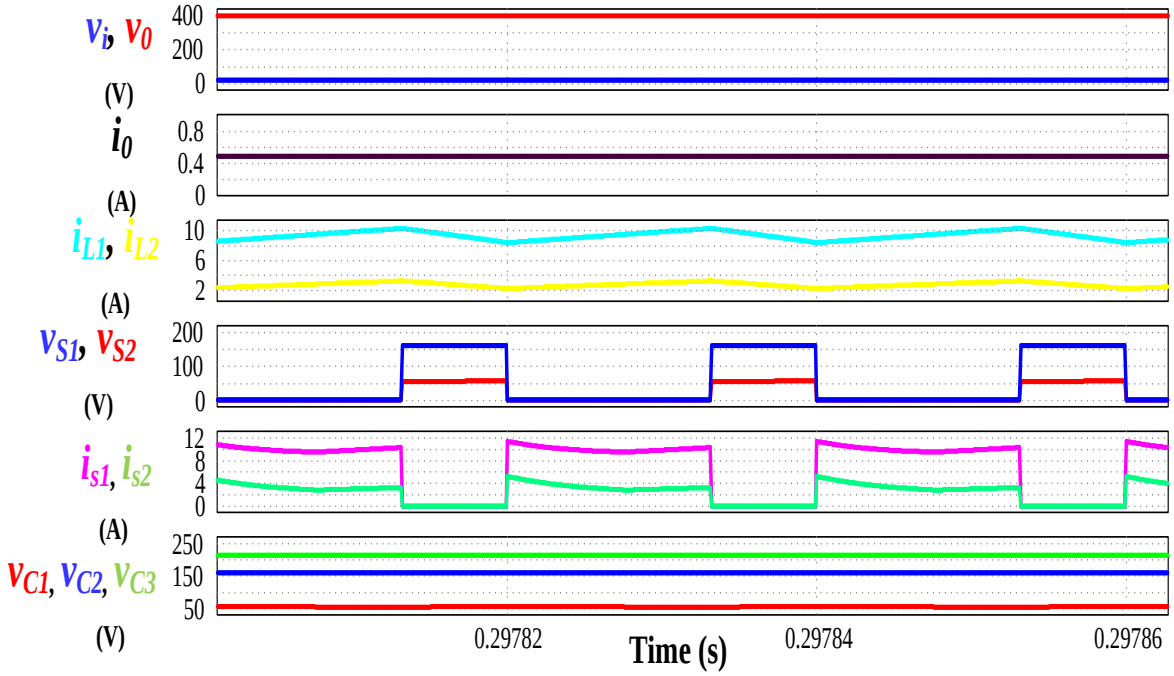
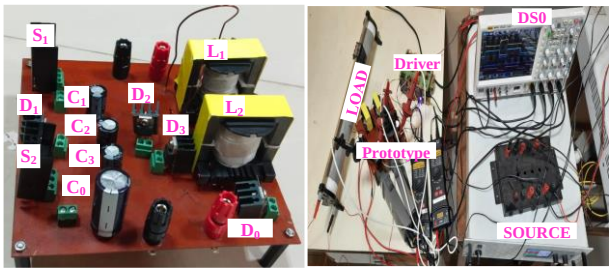


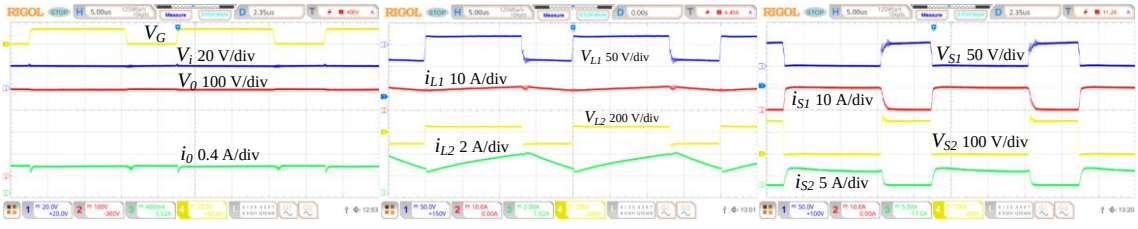
Figure 5.6. Simulated results of SCQBC converter

Prior to experimental validation the proposed SCQBC converter ideal characteristics are validated with the aid of simulation results and are as shown in Figure 5.6. Since the semiconductor voltage stresses are directly depending on the intermediate capacitor voltage stresses and the current stresses are related to switched inductor currents, these two performance indices are majorly reflected in the Figure 5.6. In addition, the input and output port parameters and switch voltage-current stresses are also reported in Figure 5.6.

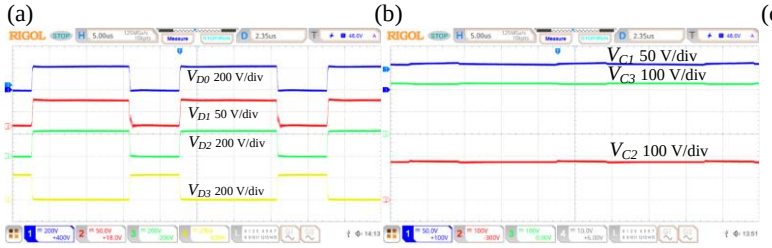


(a) (b)

Figure 5.7. SCQBC converter (a) prototype and (b) Experimental setup

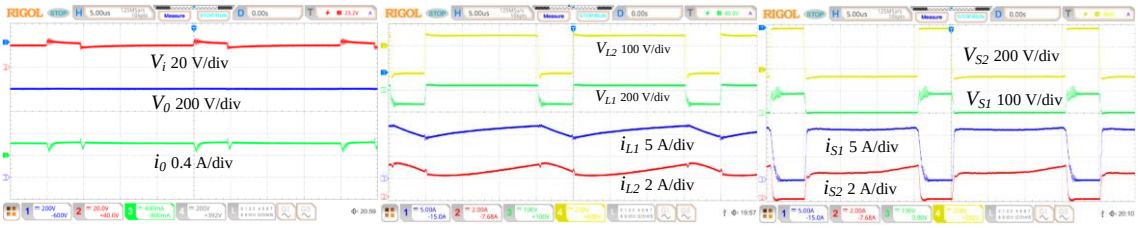


(a) (b) (c)

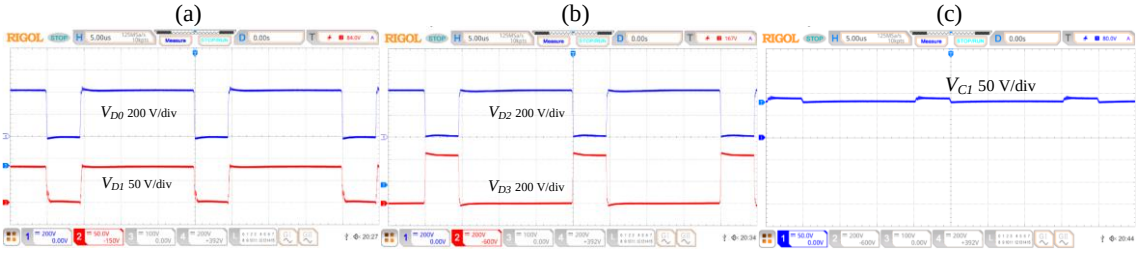


(d) (e)

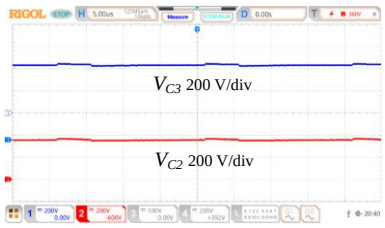
Figure 5.8. Experimental results of SCQBC converter for 400 V output (a) input and output voltages v_i and v_0, load current i_0 (b) inductor voltages (v_{L1} and v_{L2}) and currents (i_{L1} and i_{L2}) (c) switch voltages (v_{S1} and v_{S2}) and currents (i_{S1} and i_{S2}) (d) diode voltages (V_{D0}–V_{D3}) and (e) capacitor Voltages (V_{C1}–V_{C3}).



(a) (b) (c)

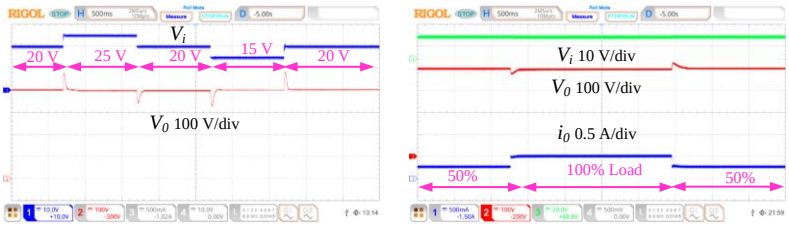


(d) (e) (f)



(g)

Figure 5.9 Experimental results of SCQBC converter for 800 V output (a) input and output voltages v_i and v_0, load current i_0 (b) inductor voltages (v_{L1} and v_{L2}) and currents (i_{L1} and i_{L2}) (c) switch voltages (v_{S1} and v_{S2}) and currents (i_{S1} and i_{S2}) (d) diode voltages (V_{D0}–V_{D1}) (e) diode voltages (V_{D2}–V_{D3}) (f) capacitor Voltage (V_{C1}) and (g) capacitor Voltages (V_{C2}–V_{C3})



(a) (b)

Figure 5.10. Closed loop performance of SCQBC converter for (a) stepped V_i and (b) stepped load

The experimental validation of the proposed SCQBC converter performance indices for a power rating of 200 W is shown in Figure 5.7, with the prototype specifications as in Table 5.2. The proposed converter attains an output voltage of 391 V at a load current of 489 mA for an applied voltage of 20 V as shown in Figure 5.8 (a). The inductor voltages and currents are resembling their ideal wave shapes and are as shown in Figure 5.8 (b). Since the entire input current passes through the inductor L_1, its ripple content will be low. The input current of the SCQBC converter is observed to be 10.08 A, making the converter's operating efficiency 94.84%.

The blocking voltage of switch S_1 is low and it is equal to the voltage stress of V_{C1}. The voltage stress on switch S_2 is greatly reduced and it is 43% of V_0 as shown in Figure. 5.8 (c). The diode D_1 blocking voltage is equal to switch S_1, and that of diodes D_0, D_2, and D_3 are at a voltage of $\frac{(2-D)V_0}{3-D}$, making the diode operating voltage stress 15% and 57% of V_0 as shown in Figure 5.8 (d). It is evident from the aforementioned discussion that diodes and switches peak voltage stresses are always less than V_0. The capacitor voltage stresses (V_{C1}-V_{C3}) are as shown in Figure 5.8 (e), in which as discussed earlier capacitors C_1, C_2, and C_3 are having a voltage stress of $\frac{V_0(1-D)}{(3-D)}$, $\frac{V_0}{(3-D)}$, and $\frac{V_0(2-D)}{(3-D)}$ i.e., the capacitors C_1, C_2 and C_3 are at a voltage stress of 15%, 43% and 57% of output voltage.

The stated SCQBC converter performance feasibility is also validated for an ultra voltage gain of 40 i.e., the input voltage V_i is fixed at 20 V with the same inductors L_1 and L_2, now the output voltage V_0 is raised up to 800 V at a duty ratio of 76.4%. Here the same capacitor values

are used as in the previous case but with an increased voltage rating as per the new V_0 requirement. For the aforementioned operating conditions, the experimental output voltage is observed to be 777 V as shown in Figure 5.9 (a). Subsequently, all the aforementioned performance indices like inductor voltages and currents as shown in Figure 5.9 (b), switch voltage and currents as in Figure 5.9 (c), and diode voltages and currents as shown in Figure 5.9 (d) and (e) are experimentally validated at 200 W, 50 kHz operating conditions. The average capacitor voltages are in good accord with their ideal values as shown in Figure 5.9 (f) and (g).

The open loop control to output transfer function [33], [34] of the SCQBC converter preceded by a PI controller of K_P=0.000015 and K_I=0.004 acquired a stable output voltage against source voltage and load current perturbations. The control performance of the SCQBC converter for a stepped voltage V_i from 15 V- 20 V- 25 V at a stable V_0 of 400 V is shown in Figure 5.10 (a). In addition to the step changes in input voltage, a 50% step change in load is also considered to verify the SCQBC control performance as shown in Figure 5.10 (b). The theoretical and experimental efficiency variation concerning to load power is as shown in Figure 5.11 and the power loss distribution wheel at rated power of 200 W of various elements for both theoretical and experimental cases is as shown in Figure 5.12 (a) and (b).

Table 5.2. Design Specifications

Specification	Rating
Input voltage	20 V
Output Voltage	400 V
Power	200 W
Inductors	L_1=130 µH, L_2=700 µH
capacitors	C_0=100 µF, C_1-C_3=22 µF
Diodes	D_0, D_1, D_3 (STPSC10H065) D_1 (MBR10100)
Switches	S_1 (FDPF3860T) S_2 (STW28N65M2)

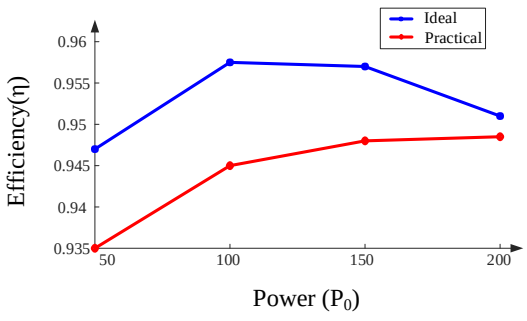
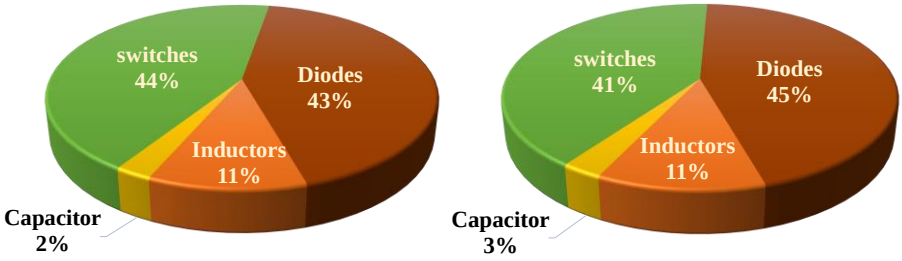


Figure 5.11. SCQBC converter efficiency versus output power.



(a) (b)

Figure 5.12. SCQBC converter loss distribution among various elements (a) ideal (b) experimental.

5.8 Performance Comparison

The performance comparison of similar quadratic boost topologies with the proposed converter in terms of voltage gain, normalized voltage stress, component count, and ripple content in the input current is reported in Table 5.3. Figure 5.13 (a) presents the voltage gain comparison, in which among all the converters only the converters in [104]-[106] and [110] ASCQBC-II performance is superior to SCQBC but these converters have an overall component count of 16 and 14 respectively, thereby making the energy storage element count high. The SCQBC converter attains an output voltage of 400 V operating at a duty ratio of 0.658 featuring a superior voltage gain of 20 whereas the converter in [100] is operating at a dc static gain near 14 and that of converter [99], [88] and [101] are operating at a voltage gain about 10-12. Among all the stated converters, the converters in [102], [91] are observed to be providing the least voltage gain of 8.5 for the aforementioned duty ratio. In order to bring the uniformity between the topologies chosen for comparison a parameter known as effectiveness index (EI) is selected such that it will indicate the voltage gain per component at the given duty ratio. Thus, effectively connecting the respective voltage gain with the overall component count. Though the converters in [105], [106] and [110] ASCQBC-I are having high EI value of 2.2 at 0.658 duty ratio but the proposed SCQBC converter also has improved EI at 1.62 as depicted in Figure. 5.13 (b), which concludes that the SCQBC is still in par with the aforementioned topologies concerning to G_{CCM} and EI comparison.

Table 5.3. Comparison of SCQBC Converter with other Quadratic Boost Converters

Topology	Voltage Gain	NDVS ($\sum V_D/V_0$)	NSVS ($\sum V_S/V_0$)	NTVS	Common Ground	Pulsating Input Current	S/C/L/D (Total)	Power Density
Ref [99]	$\frac{2-D}{(1-D)^2}$	$\frac{4-2D}{2-D}$	1	$\frac{6-4D}{2-D}$	Yes	No	2/3/2/3 (10)	Moderate
Ref [100]	$\frac{1+D}{(1-D)^2}$	$\frac{3}{1+D}$	$\frac{1}{1+D}$	$\frac{4}{1+D}$	No	No	1/4/3/4 (12)	Low
Ref [88]	$\frac{2-D}{(1-D)^2}$	$\frac{3}{2-D}$	$\frac{1}{2-D}$	$\frac{4}{2-D}$	Yes	Yes	1/3/2/4 (10)	Moderate
Ref [101]	$\frac{1+D-D^2}{(1-D)^2}$	1	$\frac{2-D}{1+D-D^2}$	$\frac{3-D^2}{1+D-D^2}$	No	Yes	2/2/2/2 (8)	High
Ref [102]	$\frac{1}{(1-D)^2}$	$\frac{1+2(1+\sqrt{G})}{G}$	$\frac{1+2(1+\sqrt{G})}{G}$	$\frac{2(1+2(1+\sqrt{G}))}{G}$	Yes	Yes	2/2/2/2 (8)	High
Ref [91]	$\frac{1}{(1-D)^2}$	$2-\frac{1}{G}$	1	$3-\frac{1}{G}$	Yes	No	1/2/2/3 (8)	High
Ref [103]	$\frac{3-D}{(1-D)^2}$	$\frac{6-D}{3-D}$	$\frac{1}{3-D}$	$\frac{7-D}{3-D}$	Yes	Yes	1/6/3/6 (16)	Low
Ref [104]	$\frac{3}{(1-D)^2}$	$\frac{10-3D-2D^2}{3}$	$\frac{2}{3}$	$\frac{12-3D-2D^2}{3}$	Yes	No	1/5/3/7 (16)	Low
Ref [105], [106]	$\frac{3+D}{(1-D)^2}$	$\frac{8-2D}{3+D}$	$\frac{2}{3+D}$	$\frac{10-2D}{3+D}$	Yes	No	2/5/2/5 (14)	Moderate
Ref [107]	$\frac{3-D^2}{(1-D)^2}$	$\frac{10-6D}{3-D^2}$	$\frac{4-2D}{3-D^2}$	$\frac{14-8D}{3-D^2}$	No	Yes	2/3/3/4 (12)	Low
Ref [108] (Synchronous Mode)	$\frac{2}{(1-D)^2}$	$\frac{5-2D}{2}$	$\frac{2-D}{2}$	$\frac{7-3D}{2}$	Yes	Yes	2/4/2/4 (12)	Moderate
Ref [109]	$\frac{2}{(1-D)^2}$	$\frac{4-D}{2}$	$\frac{1}{2}$	$\frac{5-D}{2}$	Yes	No	2/4/2/4 (12)	Moderate
Ref [110] ASCQBC-I	$\frac{1+D}{(1-D)^2}$	$\frac{3-D}{1+D}$	$\frac{2}{1+D}$	$\frac{5-D}{1+D}$	No	Yes	2/3/2/3 (10)	Moderate
Ref [110] ASCQBC-II	$\frac{3+D}{(1-D)^2}$	$\frac{7-D}{3+D}$	$\frac{2}{3+D}$	$\frac{9-D}{1+D}$	No	No	2/5/2/5 (14)	Moderate
SCQBC	$\frac{3-D}{(1-D)^2}$	$\frac{7-4D}{3-D}$	$\frac{2-D}{3-D}$	$\frac{9-5D}{3-D}$	Yes	No	2/4/2/4 (12)	Moderate

The semiconductor voltage stress is also one of the prominent features to evaluate the performance of any dc-dc converter. To understand the semiconductor voltage stress comparison, the particular type of the semiconducting element voltage stress is added and the cumulative is normalized with respect to the output voltage as expressed by the following NDVS, NSVS, and NTVS (Total surface voltage stress) equations.

$$\left.\begin{aligned} \text{Normalized Diode Voltage Stress } (NDVS) &= \frac{V_{D1}+V_{D2}+\ldots+V_{Dn}}{V_0} = \frac{\sum V_{Dx}}{V_0} \\ \text{Normalized Switch Voltage Stress } (NSVS) &= \frac{V_{S1}+V_{S2}+\ldots+V_{Sn}}{V_0} = \frac{\sum V_{Sx}}{V_0} \\ \text{Normalized Total Voltage Standing } (NTVS) &= NDVS+NSVS \end{aligned}\right\}$$

Table 5.4. Performance Comparison of Per Unit Ripple Current and Peak Semiconductor Stresses

Topology	Per Unit Ripple current $\left(\Delta I_i / I_i\right)$	Ripple current (ΔI_i)	Peak Switch Voltage Stress $\left(\hat{V}_S / V_0\right)$	Peak Switch Current Stress $\left(\hat{I}_S / I_0\right)$	Peak Diode Voltage Stress $\left(\hat{V}_D / V_0\right)$
Ref [99]	$\left(\frac{R_0}{L_1 f_s}\right)\frac{D(1-D)^4}{(1-D)^2}$	Low	$\frac{1}{2-D}$	$\frac{D\left(\frac{2-D}{1-D}\right)+1}{D^2(1-D)}$	$\frac{1-D}{2-D}$
Ref [100]	$\left(\frac{R_0}{L_1 f_s}\right)\frac{D(1-D)^4}{(1+D)^2}$	Low	$\frac{1}{1+D}$	$\frac{2D+D^2+D^3}{(1-D)^2}$	$\frac{1}{1+D}$
Ref [88]	1	High	$\frac{1}{2-D}$	$\frac{2-D}{(1-D)^2}$	$\frac{D}{2-D}$
Ref [101]	$\frac{1-D}{2-D}$	High	$\frac{1}{1+D-D^2}$	$\frac{2-D}{(1-D)^2}$	$\frac{2D-D^2}{1+D-D^2}$
Ref [102]	$1-D$	High	$3-3D+D^2$	$\frac{1}{(1-D)^2}$	$3-3D+D^2$
Ref [91]	$\left(\frac{R_0}{L_1 f_s}\right)D(1-D)^4$	Low	1	$\frac{2-D}{(1-D)^2}$	1
Ref [103]	$\left(\frac{R_0}{L_1 f_s}\right)\frac{D(1-D)^4}{(3-D)^2}$	Low	$\frac{1}{3-D}$	$\frac{2+D-D^2}{D(1-D)^2}$	$\frac{1}{3-D}$
Ref [104]	$\left(\frac{R_0}{L_1 f_s}\right)\frac{D(1-D)^4}{9}$	Low	$\frac{2}{3}$	$\frac{2+D+2D^2}{D(1-D)^2}$	$\frac{2}{3}$
Ref [105], [106]	$\left(\frac{R_0}{L_1 f_s}\right)\frac{D(1-D)^4}{(3+D)^2}$	Low	$\frac{1+D}{3+D}$	$\frac{1+3D-D^2-D^3}{D(1-D)^2}$	$\frac{2}{3+D}$
Ref [107]	$\frac{1+2D-D^3}{D(1+D)(3-D^2)}$	High	$\frac{3-D}{3-D^2}$	$\frac{1+2D-D^3}{D(1+D)(1-D)^2}$	$\frac{4(1-D)}{3-D^2}$
Ref [108] (Synchronous Mode)	$\left(\frac{R_0}{2 f_s}\right)D(1-D)^3\left(\frac{1-D}{L_1}+\frac{D}{L_2}\right.$	High	$\frac{1}{2}$	$\frac{2}{(1-D)^2}$	$\frac{2-D}{2}$
Ref [109]	$\left(\frac{R_0}{4 L_1 f_s}\right)D(1-D)^4$	Low	$\frac{D}{2}$	$\frac{1+2D-D^2}{D(1-D)^2}$	$\frac{1}{2}$
Ref [110] ASCQBC-I	$\frac{1}{(1+D)}$	High	1	$\frac{2}{(1-D)^2}$	1
Ref [110] ASCQBC-II	$\left(\frac{R_0}{L_1 f_s}\right)\frac{D(1-D)^4}{(3+D)^2}$	Low	$\frac{1+D}{3+D}$	$\frac{1+3D}{D(1-D)^2}$	$\frac{2}{3+D}$
SCQBC	$\left(\frac{R_0}{L_1 f_s}\right)\frac{D(1-D)^4}{(3-D)^2}$	Low	$\frac{1+D}{3-D}$	$\frac{3-D}{(1-D)^2}$	$\frac{2}{3-D}$

The NDVS of SCQBC converter is at 1.87 for a voltage gain of 20, which is observed to be moderate from Figure. 5.13 (c). Here in this aspect of NDVS, the converter in [102] performance is superior at an NDVS of 0.6 but the dc voltage gain attained is low. The converters in [88], [103] are having high NDVS thereby high diode voltage stress compared to all other converters. The succeeding parameter of discussion is NSVS and it is observed to be 0.57 for the SCQBC converter from Figure. 5.13 (d), this NSVS is lowest among all other converters with superior EI. The converters in [100], [102] are having the same NSVS of 0.6, the converter in [100] has a voltage gain that is similarly comparable to the SCQBC converter, and for the converter in [102] source current ripple content is large. The NTVS of the stated SCQBC converter is observed to be 2.44 from Figure. 5.13 (e). Except for the converter in [102] remaining all converters NTVS is high, for which the voltage gain is very low (8.5), and hence its performance evaluation in this aspect is not relatable to the SCQBC converter.

Although the NDVS and NSVS of the proposed converter are moderate in the end the NTVS is substantially improved. This NTVS for the converters whose voltage gain is near the SCQBC is also crucial for comparison because it indicates the effective surface voltage stress. In this regard, the converters in [91], [103] performances are not superior but the converters in [104]-[106] are having a NTVS which is closer to the stated SCQBC converter. The SCQBC converter also has the features like moderate component count, low ripple content in input current and common ground for source and load, and minimum components in the forward path.

The low source current ripple content of the SCQBC converter is validated by a thorough comparison as mentioned in Table 5.4 and as shown in Figure 5.14 (a). The topologies reported in [88], [101], [102], [107], [108], [110] ASCQBC-I are having pulsating input current at the input port. Therefore, the ripple content of these converters is high in comparison with the remaining topologies reported. The topologies of [103], [104], [105] and [110] ASCQBC-II per unit current ripple content is in par with the proposed SCQBC converter as shown in Figure. 5.14 (a). The converters in [100], [106], and [109] have superior performance in ripple current aspects, but the voltage gain of these converters is low except for the converter in [106]. Though the converter in [106] has the merit of improved ripple content performance its inductor design and selections are over-compensated i.e. ΔI_{LI} is considered as 10% of its average input current whereas in the proposed converter the same is considered to be 20%. In this regard, one can conclude that among all the converters the proposed SCQBC converter per unit ripple current performance is superior with elevated ultra voltage gains. The peak voltage stress on semiconducting elements of the stated topologies is reported in Table 5.4 and presented in Figure. 5.14 (b) and (c). From this comparison, it is evident that except for the converter in [102] the remaining converters have a peak switch voltage stress equal and or less than the output voltage. The converter in [99], [88], [101] and [104] along with the SCQBC converter have moderate peak switch voltage stress against the converters in [103], [105], [106], [109], and [110] ASCQBC-II which are having superior performance in this aspect. However, the converter in [109] is having a poor outcome in terms of voltage gain and the remaining converters of low peak switch voltage stress have high element count. It is interesting to note that the peak diode voltage stress of SCQBC converter along with the converters of superior voltage gain reported in [104]-[106] and [110] ASCQBC-II is also less than the output voltage as shown in Figure. 5.14 (c). Another key parameter of comparison would be peak switch current stress formulated in Table 5.3 and as shown in Figure. 5.14 (d). From this, it is evident that the proposed converter is having significant improvement in this aspect along with the converters in [100], [107], [108] and [110] ASCQBC-I. Though the converters in [88], [101] and [91] are having superiority in this peak switch current aspects but

they lack key features such as voltage gain and effectiveness index. The simulated and experimental results comparison is also accounted for comparison and reflected in Table 5.5.

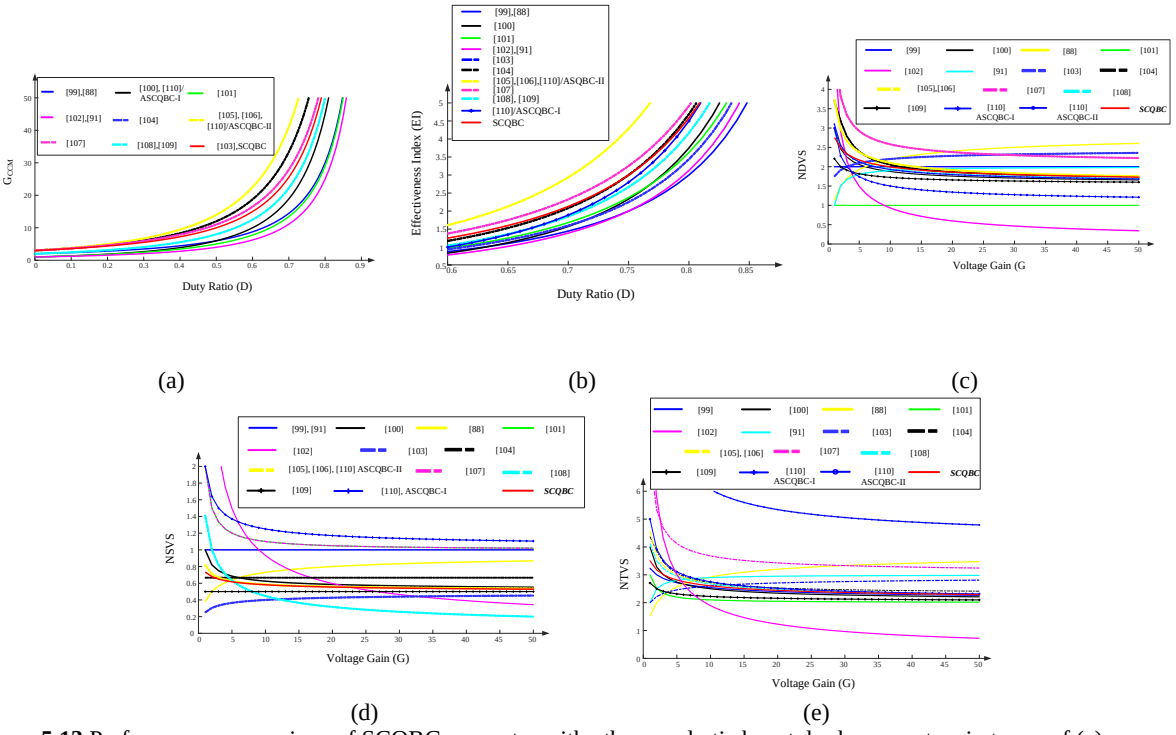


Figure 5.13 Performance comparison of SCQBC converter with other quadratic boost dc-dc converters in terms of (a) voltage gai n (b) EI (b) NDVS (c) NSVS and (d) NTVS.

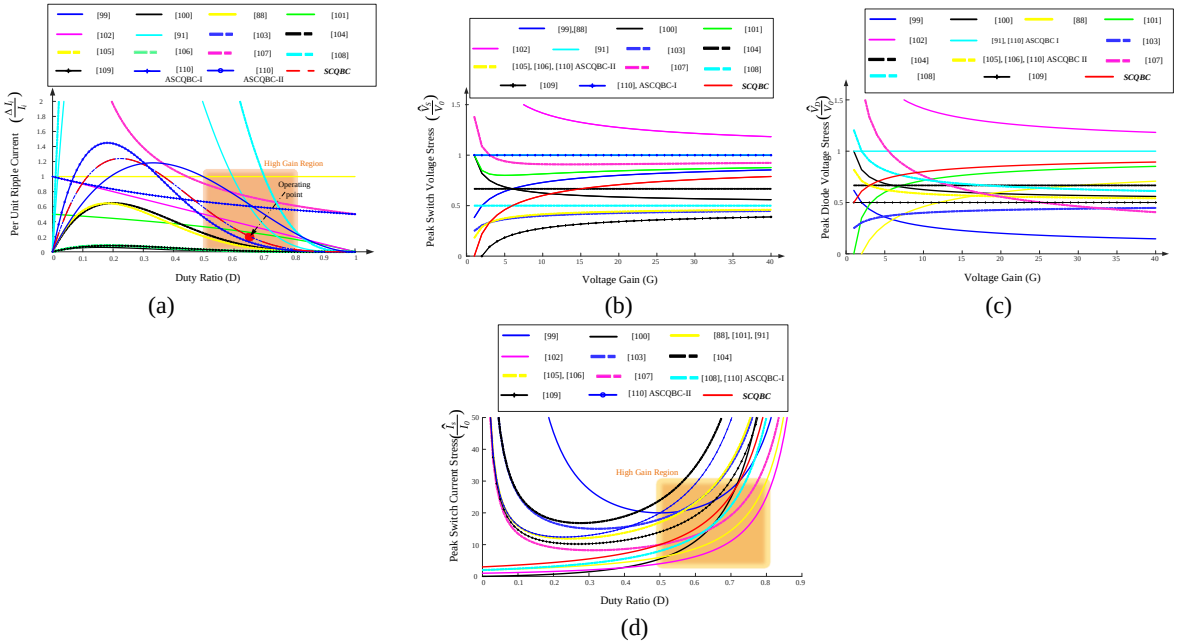


Figure 5.14. Comparison of (a) Per unit ripple current (b) switches (c) diodes peak voltage stress and (d) switch peak current stress

Table 5.5 Performance comparison of simulation and experimental findings of SCQBC converter

Performance Indices	Simulation	Experimental
Output voltage (V_0)	400 V	391 V
Output current (I_0)	0.5 A	0.489 A
Input current (I_i)	10 A	10.1 A
Inductor currents (I_{L1} & I_{L2})	10 A & 2.94 A	10.1 A & 2.45 A
Switch voltage stresses ($\hat{V}_{s1}$ & $\hat{V}_{s2}$)	59 V & 170 V	60 V & 180 V
Switch current stresses ($\hat{I}_{s1}$ & $\hat{I}_{s2}$)	12.4A & 5.5 A	10 A & 3.8 A
Capacitor voltage stress	57.3 V, 168.7 V & 223 V (C_1, C_2 & C_3)	55 V, 165 V & 225.5 V (C_1, C_2 & C_3)

5.9 Summary

In this chapter, A switched-capacitor-based quadratic boost converter with low voltage stress on rear end diode is presented in this article. The features of proposed SCQBC converter are ultrahigh step-up gain at a moderate duty cycle, low surface voltage stress, reduced ripple content in the input current, and minimum components in the forward path. The operating principle of SCQBC converter with CCM and DCM analyses is presented in this article. The proposed converter performance indices comparison with other similar quadratic boost converters is also presented in this article. Furthermore, to demonstrate the feasibility of the SCQBC converter a scaled laboratory prototype of 200 W, 400 V, 50 kHz operating with a peak efficiency of 95.4% is developed. The proposed converter feasibility for its performance indices under DCM mode of operation is also demonstrated. To comply with ultra voltage gain applications the SCQBC converter is also experimented for 800 V, 200 W, 50 kHz operation.

Chapter 6

A Wide Voltage Range Bidirectional High Voltage Transfer Ratio Quadratic Boost DC-DC converter for EVs with Hybrid Energy Sources

6. A Wide Voltage Range Bidirectional High Voltage Transfer Ratio Quadratic Boost DC-DC converter for EVs with Hybrid Energy Sources

6.1 Introduction

The clean sustainable energy-based propulsion systems are often high in demand owing to their zero-carbon emission. However, majority of these sources which are often termed as green energy micro sources persists low terminal DC voltage, henceforth requires a power conditioning circuits especially having the feature of high voltage gain. The converter offering the high voltage gain along with buck capability in reverse power flow direction is also prominent in electric propulsion systems. This kind of requirements is highly adopted in modern electric vehicles (EVs) integrated with hybrid energy sources. In this regard, a wide range bidirectional dc-dc converter with quadratic boost voltage gain is proposed in this chapter for hybrid energy source driven electric vehicles. The proposed converter is restructured such that in the forward path of buck and boost mode there exists only one semiconducting device. The benefits of stated converter are wide-voltage-range and absolute common ground. The steady state operation, voltage stress of semiconducting elements, comparison with other similar quadratic boost converters and closed loop control are presented in this article. A 200 W, 25 KHz, low voltage (V_{LV}) input of 40~120 V prototype is developed to validate the performance indices.

This chapter reports a novel bidirectional DC-DC converter (BDC) with quadratic buck-boost voltage transformation ratio (VTR) for hybrid energy source driven EVs as shown in Figure 1. In the proposed converter the posture of inductor L_2 and switch S_2 is altered to attain higher efficiency and VTRs along with the following features

- Simple structure.
- Lower input current ripple.
- Capable of operating for a wide range of input voltage thereby attaining a wide range of VTR.
- The forward path in buck and boost mode contains only one semiconducting element.
- Absolute common ground between the source and sink.

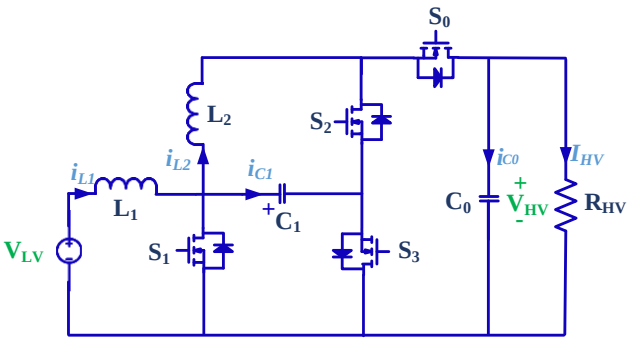


Figure 6.1. Proposed bidirectional quadratic boost dc-dc converter.

The chapter has the following organization: Section-6.2 emphasizes the boost mode operation and analysis, Section-6.3 presents buck mode of operation, Section 6.4 details about the design and control aspects. Section-6.5 discusses the experimental validation, Section-6.6 presents the comparative study and the summary is presented in 6.7.

6.2 Boost Mode of Operation and Analysis

In the boost operating state, the switching action is performed between S_1 and S_2 while the switches S_0 and S_3 are replaced by their internal diodes (D_0 and D_3) as shown in Figure 6.2 (b). The ideal operating waveforms of the proposed converter in this mode are as shown in Figure 6.2 (a).

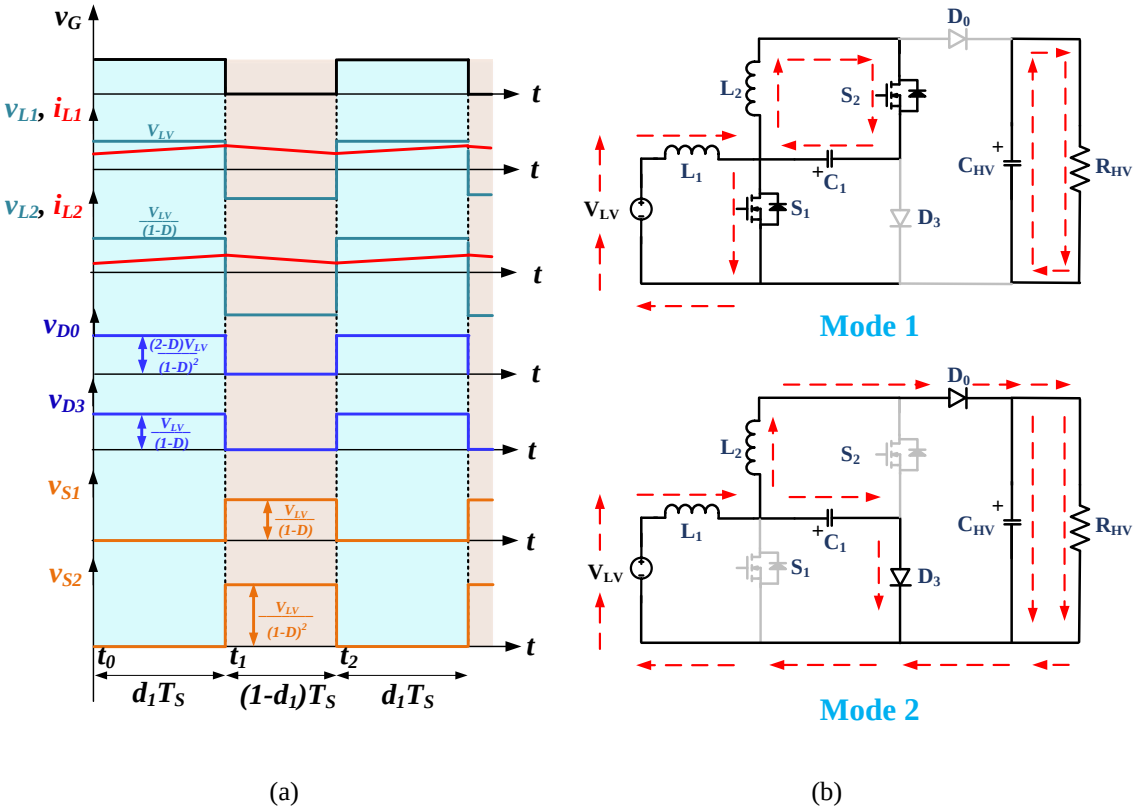


Figure 6.2. Boost mode (a) ideal operating waveforms (b) operating modes.

6.2.1 Operating State I: [t_0-t_1]

The switching pattern for this operating state is $D_0S_1S_2D_3=0110$ and current conducting paths are as shown in Figure 6.2 (b). The inductors L_1 and L_2 are charging with an applied voltage V_{LV} and V_{C1} i.e., the capacitor C_1 is discharging during this state. The reverse biased diode D_0 causes the capacitor C_{HV} to power the load R_{HV} as shown in the operating waveforms Figure 6.2 (a). The voltage and current profiles for the energy storage elements are written as follows

$$\begin{matrix} v_{L1}=V_{LV}, v_{L2}=V_{C1} \\ i_{C1}=-i_{L2}, i_{CHV}=-I_{HV} \end{matrix} \tag{6.1}$$

6.2.2 Operating State II: [t_1-t_2]

The conducting paths for this operating state are as shown in Figure 6.2 (b) with the corresponding switching pattern as $D_0S_1S_2D_3=1001$. The two capacitors C_{HV} and C_1 are charging in this state while the inductors L_1 and L_2 are discharging as shown in the operating waveforms Figure 6.2 (a). The inductor and capacitor voltage profile are as follows

$$\begin{matrix} v_{L1}=V_{LV}-V_{C1}, v_{L2}=V_{C1}-V_{HV} \\ i_{C1}=i_{L1}-i_{L2}, i_{CHV}=i_{L2}-I_{HV} \end{matrix} \tag{6.2}$$

Considering the duty ratio as d_1 for boost mode and writing the volt-sec balance for L_1 and L_2 The CCM voltage gain and voltage stress on capacitor (C_1) is written as

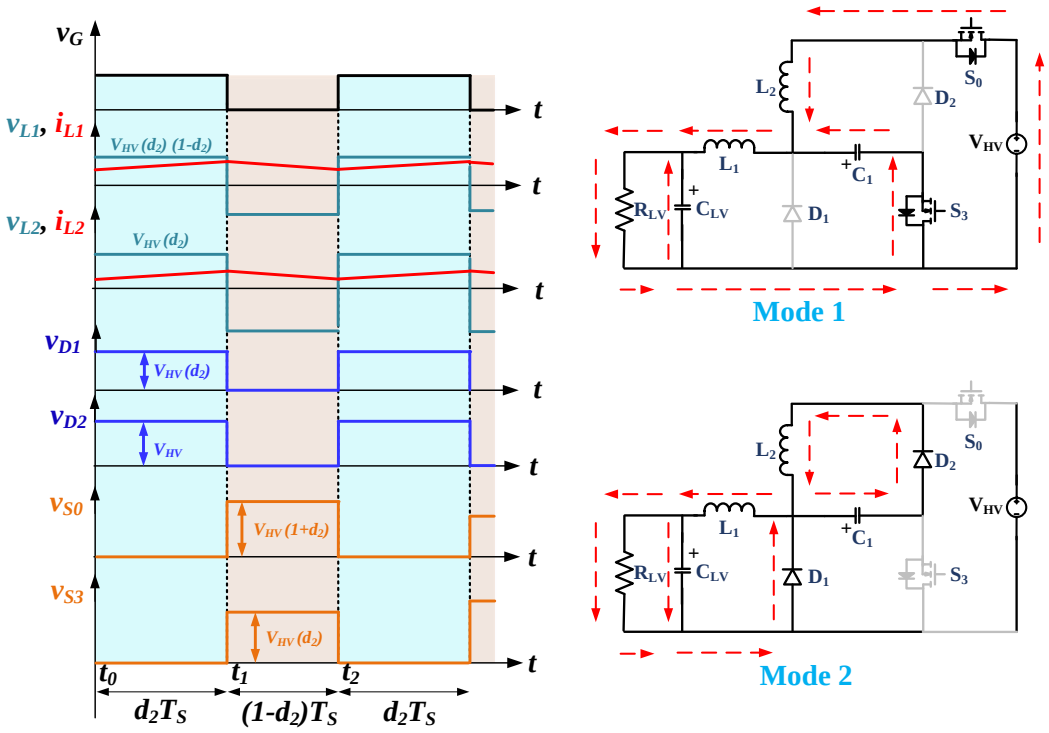
$$\begin{matrix} G_{Boost}\left(\frac{V_{HV}}{V_{LV}}\right)=\frac{1}{(1-d_1)^2} \\ V_{C1}=\frac{V_{LV}}{(1-d_1)} \end{matrix} \tag{6.3}$$

Similarly applying the amp-sec balance for capacitor C_{HV} and C_1, the steady state inductor currents are written as

$$\begin{matrix} I_{L1}=\frac{I_{HV}}{(1-d_1)^2} \\ I_{L2}=\frac{I_{HV}}{(1-d_1)} \end{matrix} \tag{6.4}$$

6.3 Buck Mode of Operation and Analysis

On the contrary to boost mode, the switching action in buck mode is between S_0 and S_3 while the switches S_1 and S_2 are replaced by their internal diodes D_1 and D_2 as shown in Figure 6.3 (b) The steady-state operating waveforms for this buck mode are as shown in Figure 6.3 (a).



(a) (b)

Figure 6.3. Buck mode (a) ideal operating waveforms (b) operating modes.

6.3.1 Operating State I: [t_0-t_1]

The corresponding switching pattern for this operating state is $S_0D_1D_2S_3=1001$ with conducting paths as shown in Figure 6.3 (b). The charge and or discharge pattern is similar to boost mode i.e., in this case, both the inductors (L_1 and L_2) are charging and the capacitor C_1 is discharging. The voltage and current profile of various energy storage elements are written as follows

$$v_{L1}=V_{C1}-V_{LV}, v_{L2}=V_{HV}-V_{C1} \\ i_{C1}=i_{L2}-i_{L1}, i_{CLV}=i_{L1}-I_{LV} \quad (6.5)$$

6.3.2 Operating State II: [t_1-t_2]

The inductors L_1 and L_2 are discharging in this operating state with switching pattern $S_0D_1D_2S_3=0110$ as shown in Figure 6.3 (b). The capacitor C_1 is charging with the aid of inductor L_2. The voltages and currents of various elements are written as

$$v_{L1}=-V_{LV}, v_{L2}=-V_{C1} \\ i_{C1}=i_{L2}, i_{CLV}=i_{L1}-I_{LV} \quad (6.6)$$

Writing the volt-sec balance for inductors L_1 and L_2 upon considering the duty ratio for buck mode of operation as d_2.

$$G_{Buck}\left(\frac{V_{LV}}{V_{HV}}\right)=(d_2)^2 \\ V_{C1}=V_{HV}(d_2) \quad (6.7)$$

Writing the amp-sec balance for capacitors C_{LV} and C_1 then inductor currents are written as

$$\begin{matrix} I_{L1}=I_{LV} \\ I_{L2}=I_{LV}(d_2) \end{matrix} \tag{6.8}$$

6.4 Parameter Design and Control Performance

6.4.1 Semiconductor Voltage Stress

Assuming all the semiconducting elements as ideal and applying the KVL equations for the selected loops of Figure 6.2 (b) and 6.3 (b), The voltage stress of various elements is written as

$$\begin{matrix} \xrightarrow{Boost\ Mode} \begin{cases} V_{S1}=V_{D3}=V_{C1}=V_{HV}(1-d_1) \\ V_{S2}=V_{HV} \\ V_{D0}=V_{HV}(2-d_1) \end{cases} \\ \xrightarrow{Buck\ Mode} \begin{cases} V_{S0}=V_{HV}(1+d_2) \\ V_{S3}=V_{D1}=V_{HV}(d_2) \\ V_{D2}=V_{HV} \end{cases} \end{matrix} \tag{6.9}$$

6.4.2 Semiconductor Current Stress

The aforementioned conducting paths from Figure 6.2 (b) and 6.3 (b) are used to write and validate the KCL equations, there by the following average current stresses of various elements are obtained

$$\left.\begin{matrix} I_{S1}=\left(\dfrac{d_1}{(1-d_1)^2}\right)I_{HV} \\ I_{S2}=\left(\dfrac{d_1}{(1-d_1)}\right)I_{HV} \end{matrix}\right\} \xleftarrow{Boost\ Mode} \xrightarrow{Buck\ Mode} \left\{\begin{matrix} I_{S0}=I_{LV}(d_2)^2 \\ I_{S3}=I_{LV}(d_2)(1-d_2) \end{matrix}\right\} \tag{6.10}$$

6.4.3 Inductor Design

The inductors are designed by assuming a ripple current of 20% to 40% (%x) of their average values. The following expressions are used to design the inductors

$$\left.\begin{matrix} L_1 \geq \dfrac{V_{LV}\, d_1(1-d_1)^2}{f_S\,(\%X)\, I_{HV}} \geq \dfrac{40\times 0.592\times(1-0.592)^2}{50\times 10^3\times 0.2\times 0.833} \geq 473\mu H \\ L_2 \geq \dfrac{V_{LV}\, d_1}{f_S\,(\%X)\, I_{HV}} \geq \dfrac{40\times 0.592}{50\times 10^3\times 0.2\times 0.833} \geq 2.84\ mH \end{matrix}\right\} \tag{6.11}$$

6.4.4 Capacitor Design

Similarly, the capacitors are designed by assuming a ripple voltage of 1% to 5% (%x) of their average values. The design considerations for capacitors are as follows

$$\left.\begin{matrix} C_{HV} \geq \dfrac{I_{HV}\,(d_1)^2}{f_S\,(\%X)\, V_{HV}} \geq \dfrac{0.833\times 0.592^2}{50\times 10^3\times 0.01\times 240} \geq 2.4\ \mu F \\ C_1 \geq \dfrac{I_{HV}\,(d_1)^2}{(1-d_1) f_S\,(\%X)\, V_{HV}} \geq \dfrac{0.833\times 0.592^2}{(1-0.592)\times 50\times 10^3\times 0.01\times 240} \geq 6\ \mu F \end{matrix}\right\} \tag{6.12}$$

6.4.5 Control Performance

The control feasibility of the proposed converter is analysed with the aid of state space

averaging method (SSA). As presented in the steady state analysis of the proposed converter, it is having two operating modes in both boost and buck power stages i.e., we can form two sets of differential equations based on these modes of operation in each power stage. Since the converter has two inductors and two capacitors there exist four state variables based on the inductor currents and capacitor voltages.

The following expressions are derived based on the operating modes in which, boost mode 1 and 2 are represented by equations (6.13) and (6.14), and the remaining equations (6.15) and (6.16) will represent the buck modes operation of the proposed QBDC. The proposed converter performance in single loop voltage control with the aid of a PI controller is carried out by standard small signal modeling. The overall small signal model is represented in (6.17) and (6.18), and the respective control to output voltage transfer function of a compensated plant with PI controller is represented in (6.19) and (6.20) for the respective boost and buck modes of operations. The stability of the system is also verified through bode plots for compensated plant in both boost and buck modes of operation as shown in Figure 6.4 (a) and (b).

$$\left.\begin{aligned} \frac{di_{L1}(t)}{dt} &= \frac{v_{LV}(t)}{L_1} \\ \frac{di_{L2}(t)}{dt} &= \frac{v_{C1}(t)}{L_2} \\ \frac{dv_{C1}(t)}{dt} &= \frac{-i_{L2}(t)}{C_1} \\ \frac{dV_{CHV}(t)}{dt} &= \frac{-i_{HV}(t)}{C_{HV}} = \frac{-V_{CHV}(t)}{R_{HV}C_{HV}} \end{aligned}\right\} \rightarrow d_1 T_S \tag{6.13}$$

$$\left.\begin{aligned} \frac{di_{L1}(t)}{dt} &= \frac{v_{LV}(t)-v_{C1}(t)}{L_1} \\ \frac{di_{L2}(t)}{dt} &= \frac{v_{C1}(t)-v_{CHV}(t)}{L_2} \\ \frac{dv_{C1}(t)}{dt} &= \frac{i_{L1}(t)-i_{L2}(t)}{C_1} \\ \frac{dV_{CHV}(t)}{dt} &= \frac{i_{L2}(t)}{C_{HV}} - \frac{V_{CHV}(t)}{R_{HV}C_{HV}} \end{aligned}\right\} \rightarrow (1-d_1) T_S \tag{6.14}$$

$$\left.\begin{aligned} \frac{di_{L1}(t)}{dt} &= \frac{v_{C1}(t)-v_{CLV}(t)}{L_1} \\ \frac{di_{L2}(t)}{dt} &= \frac{v_{CHV}(t) - v_{C1}(t)}{L_2} \\ \frac{dv_{C1}(t)}{dt} &= \frac{-i_{L1}(t)+i_{L2}(t)}{C_1} \\ \frac{dV_{CLV}(t)}{dt} &= \frac{i_{LV}(t)}{C_{LV}} - \frac{V_{CLV}(t)}{R_{LV}C_{LV}} \end{aligned}\right\} \rightarrow d_2 T_S \tag{6.15}$$

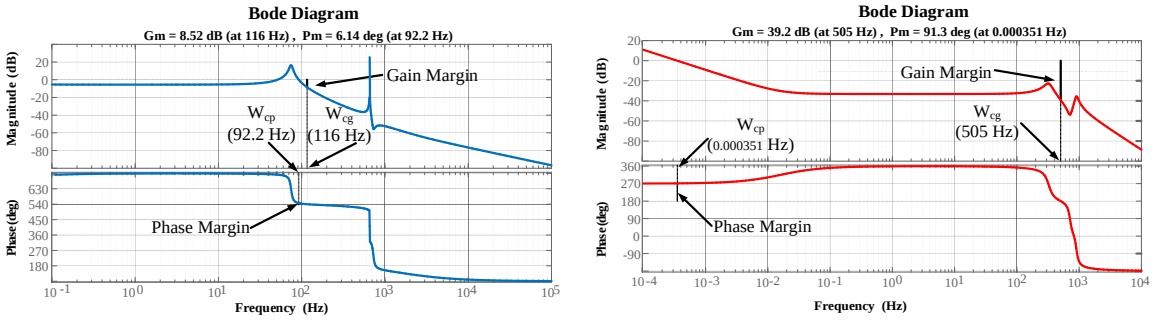
$$\left.\begin{aligned} \frac{di_{L1}(t)}{dt} &= \frac{-v_{CLV}(t)}{L_1} \\ \frac{di_{L2}(t)}{dt} &= \frac{-v_{C1}(t)}{L_2} \\ \frac{dv_{C1}(t)}{dt} &= \frac{i_{L2}(t)}{C_1} \\ \frac{dV_{CLV}(t)}{dt} &= \frac{i_{LV}(t)}{C_{LV}} - \frac{V_{CLV}(t)}{R_{LV}C_{LV}} \end{aligned}\right\} \rightarrow (1-d_2) T_S \tag{6.16}$$

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{C1}(t)}{dt} \\ \frac{d\hat{v}_{CHV}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d_1)}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-(1-d_1)}{L_2} \\ \frac{1-d_1}{C_1} & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{(1-d_1)}{C_{HV}} & 0 & \frac{-1}{R_{HV}C_{HV}} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{c1}(t) \\ \hat{v}_{CHV}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{LV}(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} \\ \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{-1}{C_{HV}} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{CHV} \end{bmatrix} \hat{d}_1(t) \tag{6.17}$$

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{C1}(t)}{dt} \\ \frac{d\hat{v}_{CLV}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d_2}{L_1} & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_2} & 0 \\ \frac{-d_2}{C_1} & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_{LV}} & 0 & 0 & \frac{-1}{R_{LV}C_{LV}} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{c1}(t) \\ \hat{v}_{CLV}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{d_2}{L_1} \\ 0 \\ 0 \end{bmatrix} \hat{v}_{HV}(t) + \begin{bmatrix} \frac{V_{C1}}{L_1} \\ \frac{V_{LV}}{L_2} \\ \frac{-I_{L1}}{C_1} \\ 0 \end{bmatrix} \hat{d}_2(t) \tag{6.18}$$

$$\left(\frac{\hat{v}_{HV}(s)}{\hat{d}_1(s)} \Big/ \hat{v}_{LV}(s)=0 \right) = \frac{-4.4\times10^{23}\, s^4 + 4.688\times10^{27}\, s^3 - 1.036\times10^{31}\, s^2 + 9.458\times10^{34}\, s + 9.458\times10^{33}}{4.781\times10^{22}\, s^5 + 1.66\times10^{24}\, s^4 + 8.22\times10^{29}\, s^3 + 2.793\times31\, s^2 + 1.784\times10^{35}\, s} \tag{6.19}$$

$$\left(\frac{\hat{v}_{LV}(s)}{\hat{d}_2(s)} \Big/ \hat{v}_{HV}(s)=0 \right) = \frac{4.542\times10^{16}\, s^3 - 2.864\times10^{19}\, s^2 + 9.176\times10^{23}\, s + 9.176\times10^{22}}{3.092\times10^{11}\, s^5 + 3.865\times10^{14}\, s^4 + 1.139\times10^{19}\, s^3 + 6.503\times10^{21}\, s^2 + 4.165\times10^{25}\, s} \tag{6.20}$$



(a) (b)

Figure 6.4. Bode plots of compensated (PI) proposed converter (a) boost mode (b) buck mode.

6.5 Experimental Results

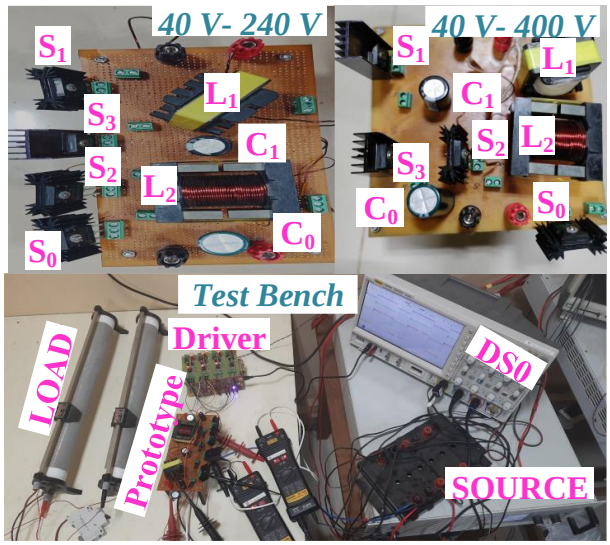


Figure 6.5. Prototypes and experimental setup.

The proposed converter performance indices are experimentally demonstrated for a power rating of 200 W as shown in Figure 6.5 and the prototype specifications are provided in Table 6.1. The mosfets are hard switched at 25 kHz for both buck and boost operations.

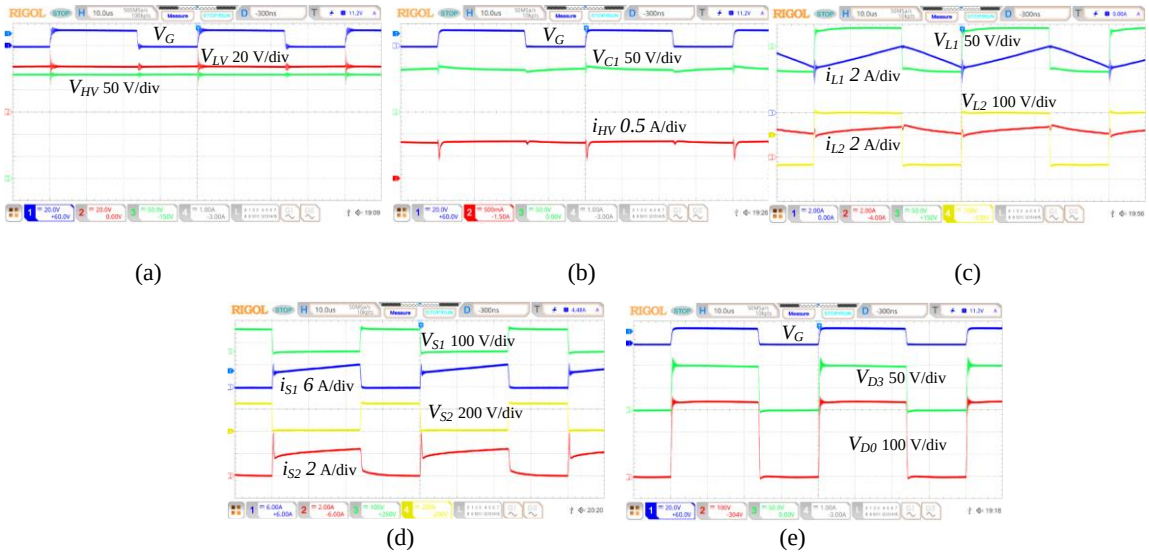


Figure 6.6. Boost mode experimental results 40-240 V, 200 W (a) input and output voltages (v_{LV} and v_{HV})(b) intermediate capacitor C_1 voltage and HV side current (v_{C1} and i_{HV}) (c) inductor voltages and currents (v_L and i_L) (d) switch voltages and currents (v_S and i_S) (e) diode voltages (v_{D0} and v_{D3}).

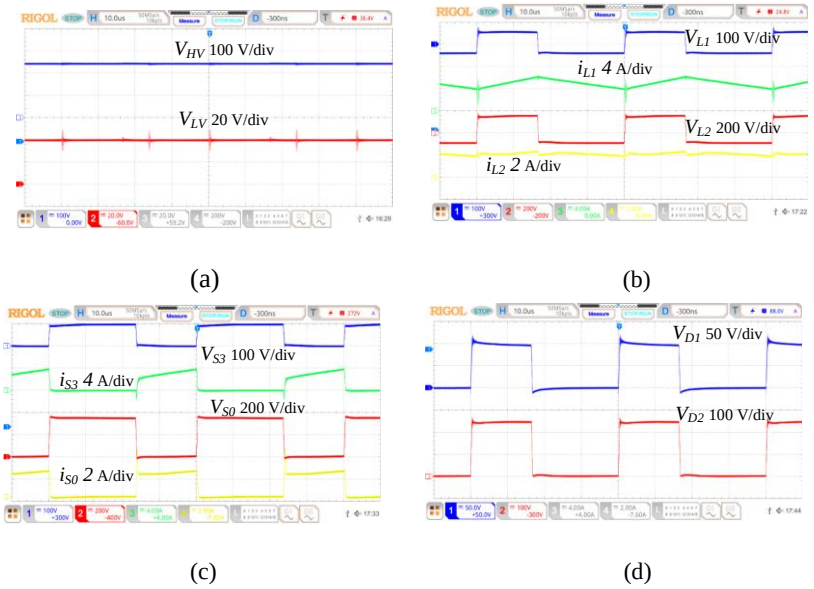
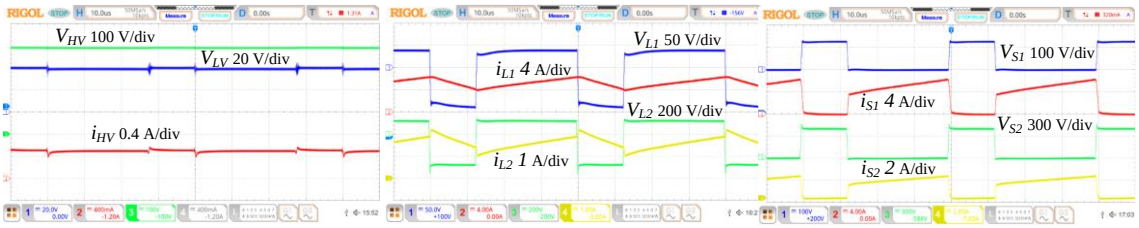


Figure 6.7. Buck mode experimental results 240-40 V, 200 W (a) input and output voltages (v_{LV} and v_{HV}) (b) inductor voltages and currents (v_L and i_L) (c) switch voltages and currents (v_S and i_S) (d) diode voltages (v_{D1} and v_{D2}).

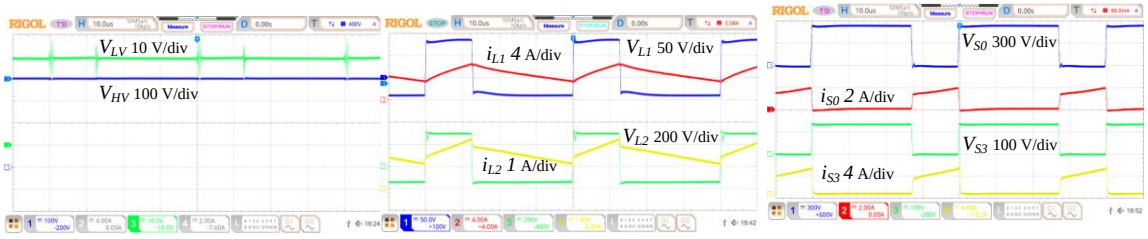
(a) (b) (c)

Figure 6.8. Closed loop validation of 40-240 V, 200 W (a) boost mode step change in v_{LV} (b) buck mode ramped output v_{LV} (c) boost mode step change in load 50% to 100%.



(a) (b) (c)

Figure 6.9. Boost mode experimental results 40-400 V, 200 W (a) input and output voltages (v_{LV} and v_{HV}), and HV side current (i_{HV}) (b) inductor voltages and currents (v_L and i_L) (c) switch voltages and currents (v_S and i_S).



(a) (b) (c)

Figure 6.10. Buck mode experimental results 400-40 V, 200 W (a) input and output voltages (v_{LV} and v_{HV}) (b) inductor voltages and currents (v_L and i_L) (c) switch voltages and currents (v_S and i_S).

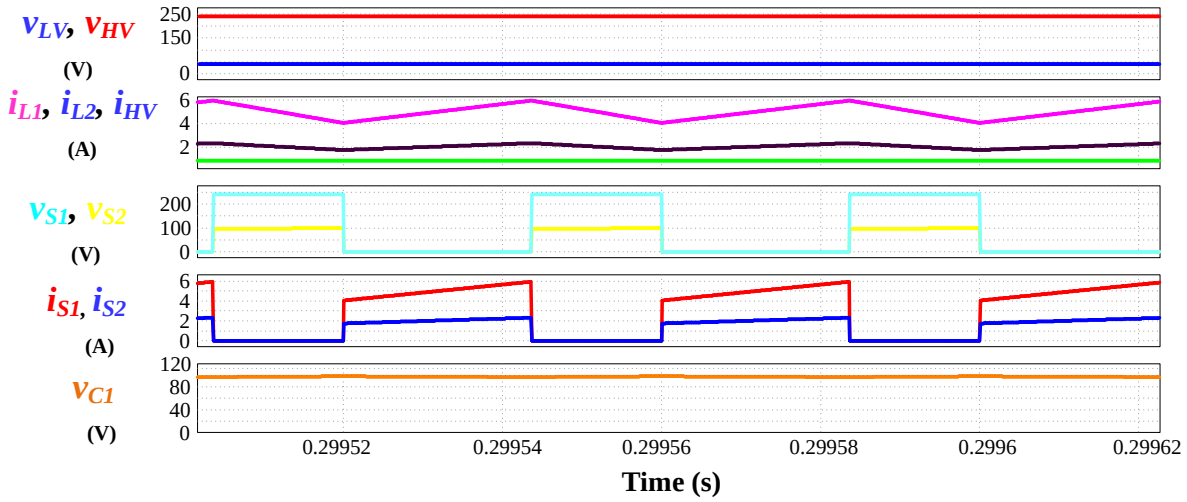


Figure 6.11. Boost mode simulated results for 40-240 V

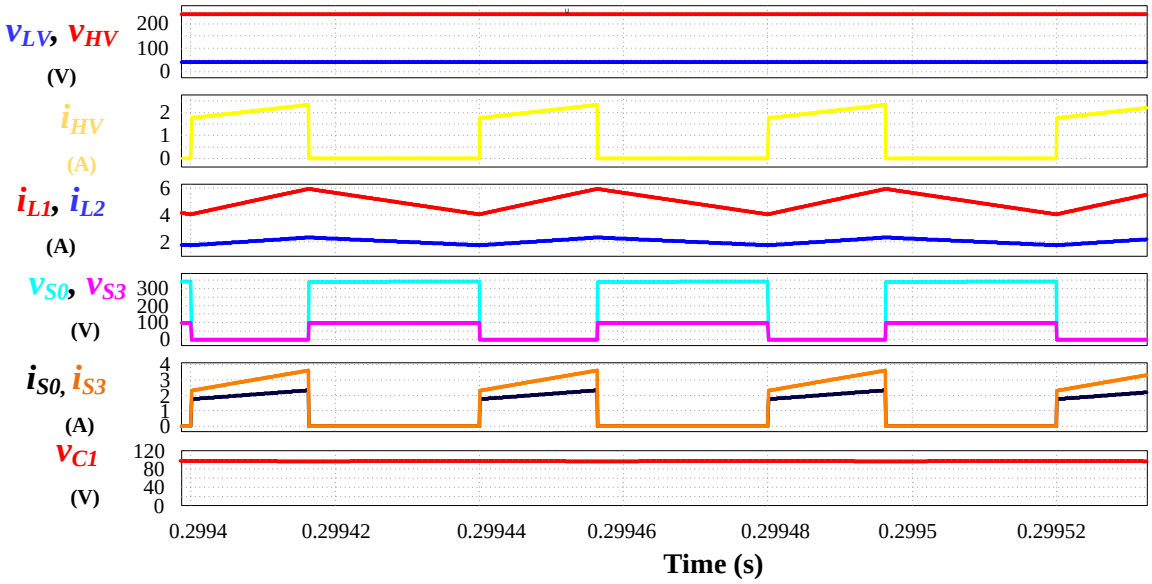
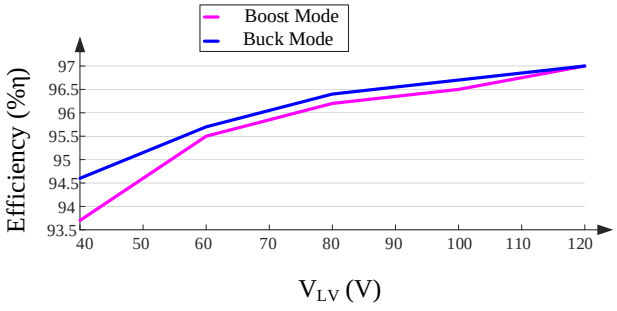


Figure 6.12. Buck mode simulated results for 240-40 V

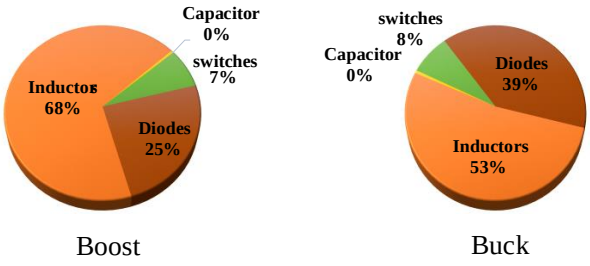
The experimental results for the boost mode of operation are provided in Figure 6.6. The LV side voltage is 40 V and the duty for switches S_1 and S_2 is 0.592 with a load resistance of 288 Ω. The converter is operating at an efficiency of 93.7% with an average input current of 5.01 A. The HV side voltage and currents are observed to be 235 V and 0.799 A as shown in Figure 6.6 (a) and (b). The voltage stress of capacitor C_1 is near to $V_{HV}(1-d_1)$ i.e., 96.8 V as shown in Figure 6.6 (b). Both the inductor currents and voltages are in good accord with their ideal wave shapes and have a peak current of 6 A and 2.4 A respectively as shown in Figure 6.6 (c). The peak voltage stress of switches S_1 and S_2 matches with the $V_{HV}(1-d_1)$ and V_{HV} as shown in Figure 6.6 (d). The body diode voltages (V_{D0} and V_{D3}) are at 340 V and 100 V as shown in Figure 6.6 (e).

The bidirectional power flow is validated by allowing the proposed converter to be operated in buck mode with a V_{HV} of 240 V and I_{HV} of 0.806 A. The converter is operated at a duty ratio of 0.408 for which the observed V_{LV} is 39.4 V at an average output current I_{LV} of 4.68 A as shown in Figure 6.7 (a) and (b). For the aforementioned conditions, the proposed converter buck mode operating efficiency is 95.3%. The voltage stress of switches S_0 is at $V_{HV}(1+d_2)$ and S_3 is at $V_{HV}(d_2)$, Similarly, the voltage stress of diodes D_1 and D_3 are also in par with their ideal magnitudes of $V_{HV}(d_2)$ and V_{HV} as shown in Figure 6.7 (c) and (d). The control performance of the proposed converter for a sudden change of input LV voltage from 40 – 45 V and 40 – 35 V cases, for which the observed output HV voltage is 240 V in boost mode and a ramp LV output voltage of 40 – 120 V (V_{LV}) for a HV input voltage of 240 V in buck mode are shown in Figure 6.8 (a), and (b). The closed loop validation is also carried out for 50% sudden change in load condition as shown in Figure 6.8 (c).

To further enhance the proposed QBDC operating range to match with precise applications where in which a HV terminal voltage of 400 V is required, a case study of 40-400 V bidirectional power transfer is considered and performance indices are experimentally validated at 200 W, 25 kHz as shown in Figure 6.9 and 6.10. All the semiconductor and energy storage element voltage and current are in good accord with their ideal operating conditions. The proposed QBDC is observed to be operating at an efficiency of 94.7% and 95.1% for boost and buck operating states. The ideal operating conditions validation with the aid of simulated results for boost and buck modes at 40-240 V range are reported in Figure 6.11 and 6.12. The experimented efficiencies for different voltage levels within the 40-120 V range is carried out and are shown Figure 6.13 (a) and their respective standard loss distribution at 40 V and 200 W (rated power) is shown in Figure 6.13 (b).



(a)



(b)

Figure 6.13. (a) Efficiency variation of the proposed converter with wide range of V_{LV}, 40~120 V (b) loss distribution for boost (V_{LV} = 40 V, 200 W) and buck (V_{HV} = 240 V) modes.

Table 6.1 Design Specifications

Specification	Rating
Input voltage	40~120 V
Output Voltage	240 V
Power	200 W
Inductors	L_1=500 µH, L_2=4.5 mH
capacitors	C_{HV} = C_{LV} =100 µF, C_1 =33 µF
Switches	S_0, S_2 (IPW65R060CFD7) S_1, S_3 (IRF300P226)

6.6 Comparison with similar Quadratic BDC

The proposed converter comparison with other QBDCs is carried out regarding numerous performance indices like; component count, buck and boost voltage gains, power rating, efficiency, existence of continuous current at LV and HV ports, switching frequency and normalized total voltage stress (NTVS) [30] of the converters as shown in Table 6.2.

The converters in [20-22],[24] and the proposed converter are similar in terms of voltage gains as shown in Figure 6.14 (a) and (b). The converter in [22] has a high component count i.e., its effectiveness index (EI, as defined in [29]) is less in comparison with the converters in [20],[21],[24] and the proposed converter as shown in Figure 6.14 (c). Though the maximum switch voltage stress is moderate, its overall NTVS is high as shown in Figure 6.15 (a) and (b). Another prominent demerit of the converter in [22] is that the switch T_1 has higher conducting interval i.e., it remains completely turned on for the entire boost operation and in the buck mode of operation, its body diode is turned on for d_2T_S period. The performance of converters in [20],[21],[24] in terms of EI is similar to the proposed converter. The NTVS of the proposed converter and [21] is moderate in comparison with the converters in [20], [24] as shown in Figure 6.15 (b).

The converter in [23] has better voltage gain in buck and boost modes but its overall component count is high. This converter has no common ground there by its feasibility towards many applications is limited. The maximum voltage stress on the switch and NTVS of the converter in [23] has improved in comparison with other converters. In [25], a BDC converter is described with identical buck and boost VTRs. This converter has LC filters at each port to provide continuous currents at the LV and HV ports. These filters make the overall converter bulky and power density to be low. Regarding the voltage stress, this converter has poor performance as shown in Figure 6.15 (a) and (b). The voltage gains and EI of the converter in [26] is better in comparison with the other converter except the converter in [23]. Though the voltage stress of this converter is moderate, its overall component count is still high.

The plot for per unit current ripple concerning to the variation in duty ratio is shown in Figure 6.15 (c). To have uniformity in comparison among the stated converters the operating conditions are assumed to be identical to the proposed QBDC. The per unit input current ripple for the converters in [20] is 0.026, the proposed BDC and the converter in [26] are at 0.055, in addition the converter in [23] is having this ripple at 0.27 and the remaining converters possess per unit input current ripple more than unity. The aforementioned discussion emphasizes that the QBDC converter along with the converters in [20] and [26] is having the least input current ripple.

Table 6.2 Performance comparison

Topology	Ref [61]	Ref [62]	Ref [111]	Ref [112]	Ref [113]	Ref [63]	Ref [64]	Proposed
L/C/D/S (Total)	2/3/0/4 (9)	2/3/0/4 (9)	2/3/2/4 (11)	2/5/0/6 (13)	2/3/0/4 (9)	3/4/0/4 (11)	2/4/0/5 (11)	2/3/0/4 (9)
Boost Gain	$\frac{1}{(1-d_1)^2}$	$\frac{1}{(1-d_1)^2}$	$\frac{1}{(1-d_1)^2}$	$\frac{(3-d_1)}{(1-d_1)^2}$	$\frac{1}{(1-d_1)^2}$	$\left(\frac{d}{(1-d)}\right)^2$	$\frac{(1+d_1)}{(1-d_1)^2}$	$\frac{1}{(1-d_1)^2}$
Buck Gain	$(d_2)^2$	$(d_2)^2$	$(d_2)^2$	$\frac{(d_2)^2}{(2+d_2)}$	$(d_2)^2$	$\left(\frac{d}{(1-d)}\right)^2$	$\frac{(d_2)^2}{(2-d_2)}$	$(d_2)^2$
Power Rating (W)	100	160	200	2000	500	500	500	200
Switching Frequency (KHz_2)	50	30	15	100	50	50	50	25
Efficiency (η) Boost Mode	95.7%	96.5%	83.2%	97.2%	97.1%	97.8%	96.8%	93.7%
Efficiency (η) Buck Mode	93.7%	93.2%	88.7%	97.4%	95.6%	97.5%	97.2%	95.3%
Continuous LV Port Current	YES	YES	YES	YES	YES	YES	YES	YES
HV port Common Ground	NO	NO	NO	NO	NO	YES	NO	NO
	YES	YES	YES	NO	YES	YES	YES	YES
Maximum Voltage stress on Switch	V_{HV}	$V_{HV}(2-d_1)$	V_{HV}	$V_{HV}\left(\frac{2-d_1}{3-d_1}\right)$	V_{HV}	$\left(\frac{V_{HV}}{d_1^2}\right)$	$V_{HV}\left(\frac{2}{1+d_1}\right)$	$V_{HV}(2-d_1)$
NTVS	$\frac{1}{2+\frac{1}{\sqrt{G_{Boost}}}}$	$\frac{3}{2+\frac{1}{\sqrt{G_{Boost}}}}$	$\frac{1}{3+\frac{1}{\sqrt{G_{Boost}}}}$	$\left(\frac{9-5d_1}{3-d_1}\right)$	$\frac{2}{2+\frac{1}{\sqrt{G_{Boost}}}}$	$\frac{2+3G_{Boost}+5\sqrt{G_{Boost}}}{G_{Boost}}$	$\left(\frac{6-2d_1}{1+d_1}\right)$	$\frac{3}{2+\frac{1}{\sqrt{G_{Boost}}}}$
				$d_1=\frac{(2G-1)-\sqrt{(2G-1)^2-4G(G-3)}}{2G}$, $G=G_{Boost}$			$d_1=\frac{(2G+1)-\sqrt{(2G+1)^2-4G(G-1)}}{2G}$, $G=G_{Boost}$	

In addition to the aforementioned comparison the proposed converter has only one element in the forward path for both buck and boost modes of operation, which none of the above converters persist. The simulated and experimental performance indices comparison is reported in Table 6.3.

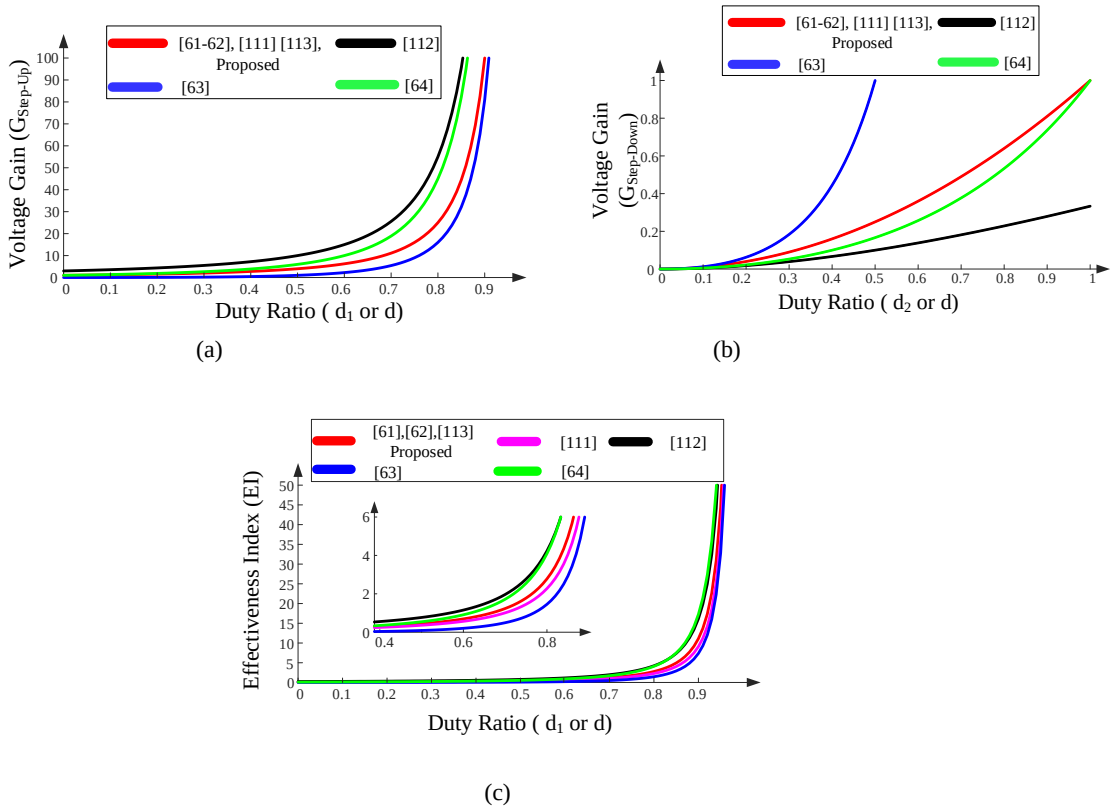


Figure 6.14. Performance comparison VTR's and effectiveness index (a) GBoost (b) GBuck (c) EI.

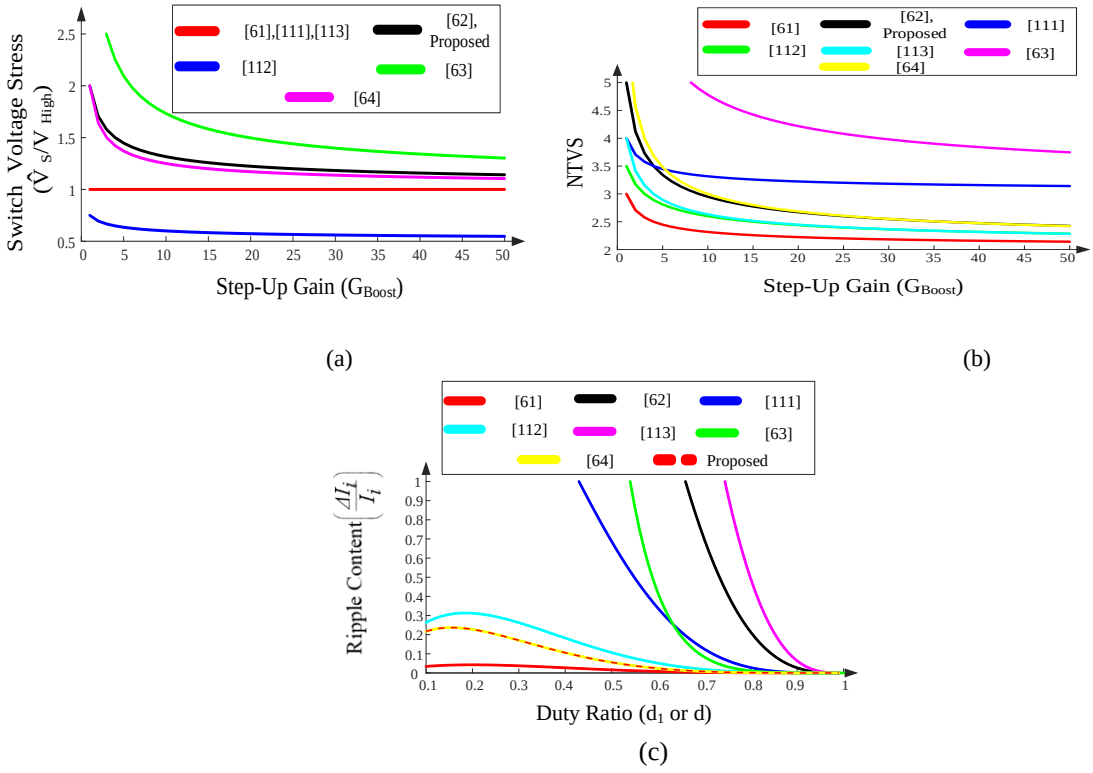


Figure 6.15. Performance comparison of switch voltage stress and input current ripple (a) Maximum switch voltage stress (b) NTVS (c) per unit current ripple.

Table 6.3 Performance comparison of simulation and experimental findings of the proposed BDC

Performance Indices	BOOST MODE		BUCK MODE	
	Simulation	Experimental	Simulation	Experimental
Output voltage (V_0)	240 V (V_{HV})	235 V (V_{HV})	40 V (V_{LV})	39.4 V (V_{LV})
Output current (I_0)	0.833 A (I_{HV})	0.799A (I_{HV})	5 A (I_{LV})	4.68 A (I_{LV})
Input current (I_i)	4.86 A	5.01 A	0.833 A	0.806 A
Inductor currents (I_{L1} & I_{L2})	5 A & 2.04 A	6 A & 4 A	5 A & 2A	5.6 A & 2.2 A
Switch voltage stresses	98.1 V& 240 V ($\hat{V}_{S1}$ & $\hat{V}_{S2}$)	100 V & 250 V ($\hat{V}_{S1}$ & $\hat{V}_{S2}$)	339 V & 99 V ($\hat{V}_{S0}$ & $\hat{V}_{S3}$)	360 V &100 V ($\hat{V}_{S0}$ & $\hat{V}_{32}$)
Switch current stresses	5.92 A & 2.32 A ($\hat{I}_{S1}$ & $\hat{I}_{S2}$)	6.7 A & 0.9 A ($\hat{I}_{S1}$ & $\hat{I}_{S2}$)	2.31 A & 3.56 A ($\hat{I}_{S0}$ & $\hat{I}_{S3}$)	4 A & 4 A ($\hat{I}_{S0}$ & $\hat{I}_{S3}$)
Capacitor voltage stress	97.92 V (C_1)	96.8 V (C_1)	98 V (C_1)	101 V (C_1)

6.7 Summary

A non-isolated quadratic boost bidirectional power flow converter is proposed in this article for HES driven EVs, which is the reconfiguration of a basic quadratic boost converter to have minimum semiconductor elements in the forward path. The proposed converter offers benefits such as a wide voltage range at LV port for buck and boost operations, moderate voltage stress on semiconductor elements, and absolute common ground. The static and dynamic performance of the proposed converter is good over a wide voltage range at the LV port. Therefore, it is suitable for the application of battery and supercapacitor bank-connected bidirectional dc-dc converters in modern EVs.

Chapter 7

A Dual Switched Inductor-Switched Capacitor based High Boost DC-DC Converters

7 A Dual Switched Inductor-Switched Capacitor based High Boost DC-DC Converters

7.1 Introduction

A dual switched inductor-switched capacitor-based dc-dc boost converter evolution and analysis are presented in this article. The front-end converter with single inductor and switched capacitor provides a voltage gain similar to Quasi-Z-Source converter while the succeeding modified SEPIC based structure is embedded to enhance the voltage gain further. The output capacitor elevated peak current is abbreviated by reconfiguring the aforementioned topology. On this premise, two converters with common ground and continuous source currents are proposed in this article. A 400V, 300W, 50 kHz prototypes are developed to verify the performance indices in steady state analysis.

This chapter reports a novel converter as shown in Figure 7.1 which is a topological integration of front-end Sheppard-Taylor H- Bridge type switched capacitor (HBSC) and intermediate modified SEPIC structures. The following are the features of the proposed dual switched inductor HBSC converter (DSL-HBSC).

- Common ground for the load and source terminals.
- Low input current ripple.
- Moderate element voltage and current stresses.

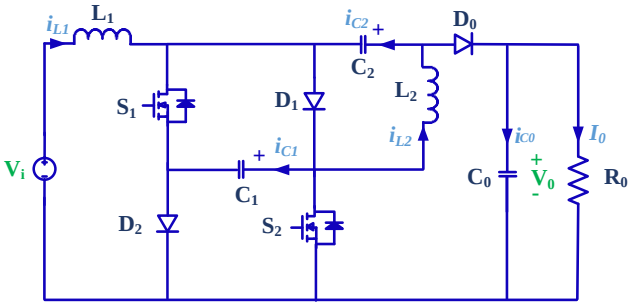
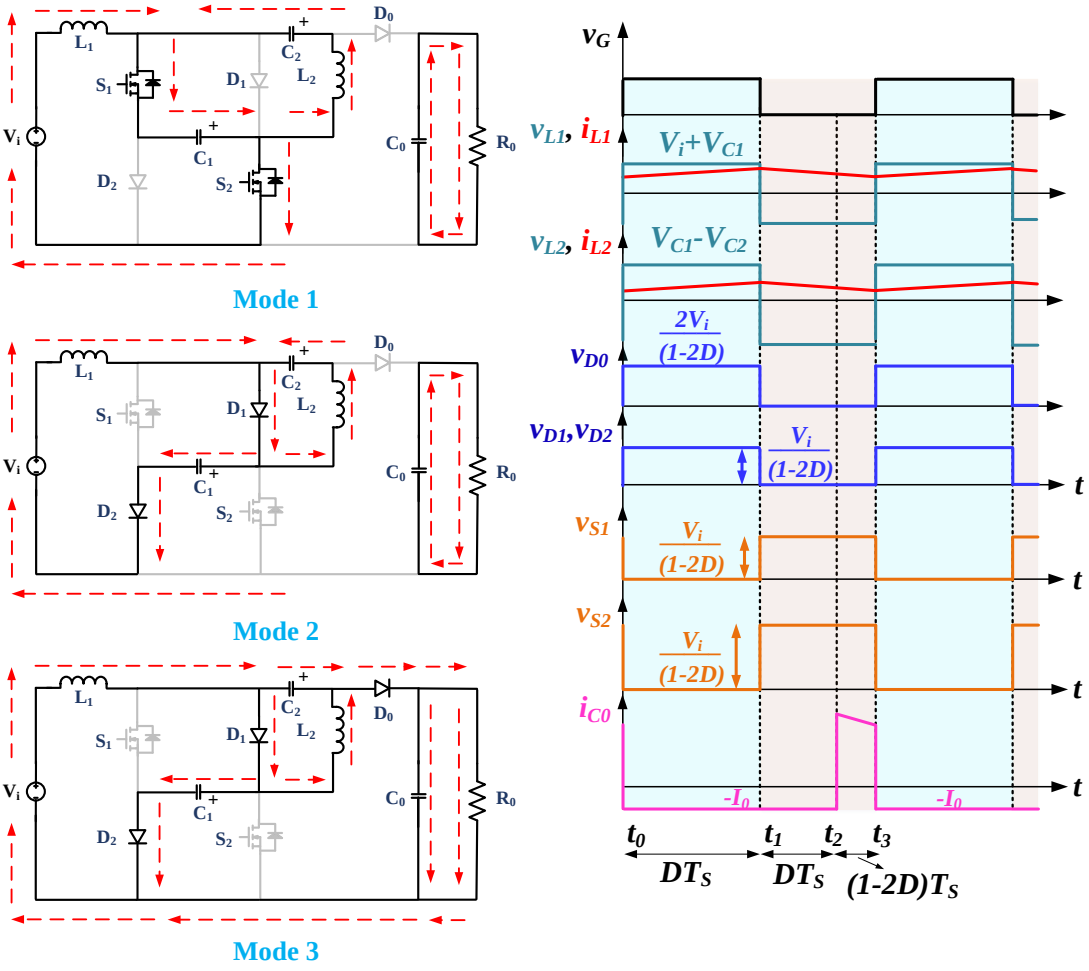


Figure 7.1. Proposed DSL-HBSC converter-I

The chapter has the following organization: Section-7.2 describes the steady state analysis, Section-7.3 presents case study (DSL-HBSC-II), Section 7.4 details about the experimental results. Section-7.5 discusses the performance comparison, and the summary is presented in Section-7.6.

7.2 Steady State Analysis

The proposed DSL-HBSC converter operates in three different modes as mentioned in Figure 7.2 (a) based on inductor-capacitor charging and discharging criteria. The following discussion emphasizes the complete operation of the DSL-HBSC-I converter in steady state continuous conduction mode (CCM) with the operating waveforms as shown in Figure 7.2 (b).



(b) (b)

Figure 7.2. DSL-HBSC-I converter (a) operating modes (b) ideal operating waveforms.

7.2.1 Mode 1: [t_0-t_1, DT_s]

In DT_S duration of mode 1, upon turning ON switches S_1 and S_2 inductor L_1 is charged with source and capacitor C_1 voltage and the series combination of inductor L_2-capacitor C_2 is charged by v_{C1} as shown in Figure 7.2 (a) All the diodes are at turn OFF condition and the capacitor C_0 powers the load R_0.

The KVL and KCL are applied to the selected loops to formulate the following equations.

$$\left.\begin{array}{c} v_{L1}=V_i+v_{C1} \\ v_{L2}=v_{C1}-v_{C2} \end{array}\right\} \tag{7.1}$$

$$\left.\begin{array}{c} i_{C1}=C_1\left(\frac{dv_{C1}}{dt}\right)=-(i_{L1}+i_{L2}) \\ i_{C2}=C_2\left(\frac{dv_{C2}}{dt}\right)=i_{L2} \\ i_{C0}=C_0\left(\frac{dv_{C0}}{dt}\right)=-I_0 \end{array}\right\} \tag{7.2}$$

7.2.2 Mode 2: [t_1-t_2, DT_s]

In DT_S duration of mode 2, the gate pulses are withdrawn for the switches causing the diodes D_1 and D_2 to turn ON at the instant t_1 as shown in Figure 7.2 (a) The dc source and the inductor L_1 charges the capacitor C_1 and inductor L_2 charges the capacitor C_2 as shown in Figure 7.2 (a). The capacitor C_0 is still in discharging state similar to mode 1. The following equations are developed with the aid of KVL and KCL for the conducting loops mentioned in Figure 7.2 (a).

$$\left.\begin{array}{c} v_{L1}=V_i-v_{C1} \\ v_{L2}=-v_{C2} \end{array}\right\} \tag{7.3}$$

$$\left.\begin{array}{c} i_{C1}=C_1\left(\frac{dv_{C1}}{dt}\right)=i_{L1} \\ i_{C2}=C_2\left(\frac{dv_{C2}}{dt}\right)=i_{L2} \\ i_{C0}=C_0\left(\frac{dv_{C0}}{dt}\right)=-I_0 \end{array}\right\} \tag{7.4}$$

7.2.3 Mode 3: [t_2-t_3, $(1-2D)T_s$]

In $(1-2D)T_S$ duration of mode 3, at the instant t_2 all the diodes are conducting and the switches are turned OFF as shown in Figure 7.2 (b). The charging profile of capacitor C_1 is similar to previous case and the capacitor C_2-inductor L_2 together charges the output capacitor C_0 and load R_0 as shown in Figure 7.2 (a). Thus, by using KVL and KCL for the conducting loops in this mode the following equations are deduced.

$$\left.\begin{array}{c} v_{L1}=V_i-v_{C1} \\ v_{L2}=v_{C1}-V_0 \end{array}\right\} \tag{7.5}$$

$$\left.\begin{array}{c} i_{C1}=C_1\left(\frac{dv_{C1}}{dt}\right)=\frac{i_{L1}}{2} \\ i_{C2}=C_2\left(\frac{dv_{C2}}{dt}\right)=-\frac{i_{L1}}{2}+\frac{I_0}{2} \\ i_{C0}=C_0\left(\frac{dv_{C0}}{dt}\right)=\frac{i_{L1}}{2}-I_0 \end{array}\right\} \tag{7.6}$$

Applying volt-sec balance on inductor L_1 and L_2, the following equations are deduced

$$(V_i+v_{C1})D+(V_i-v_{C1})D+(V_i-v_{C1})(1-2D)=0 \tag{7.7}$$

$$\left.\begin{array}{c} (v_{C1}-v_{C2})D+(-v_{C2})D+(-v_{C2})(1-2D)=0 \\ or \\ (v_{C1}-v_{C2})D+(-v_{C2})D+(v_{C1}-V_0)(1-2D)=0 \end{array}\right\} \tag{7.8}$$

Solving the above two equations (7.7) and (7.8)

$$\left.\begin{aligned} V_{C1}&=\frac{V_i}{1\text{-}2D}\\ V_{C2}&=DV_{C1}=\frac{DV_i}{1\text{-}2D}\end{aligned}\right\} \tag{7.9}$$

Using (7.9) in (7.8) the voltage gain expressed as

$$G\left(\frac{V_0}{V_i}\right)=\frac{1+D}{1-2D} \tag{7.10}$$

Similarly applying amp-sec balance on (7.2), (7.4) and (7.6) the average inductor currents are represented as

$$\left.\begin{aligned} I_{L1}&=\frac{I_0(1+D)}{1\text{-}2D}\\ I_{L2}&=I_0\end{aligned}\right\} \tag{7.11}$$

7.2.4 Voltage and Current Stresses

The mode 1 and mode 2 conducting paths are used to write KVL equations there by to find the semiconductor element voltage stresses, which are follows

$$\left.\begin{aligned} V_{D1}=V_{D2}=V_{C1}&=\frac{V_i}{1\text{-}2D}=\frac{V_0}{1+D}\\ V_{D0}=2V_{C1}&=\frac{2V_i}{1\text{-}2D}=\frac{2V_0}{1+D}\\ V_{S1}=V_{S2}=V_{C1}&=\frac{V_i}{1\text{-}2D}=\frac{V_0}{1+D}\end{aligned}\right\} \tag{7.12}$$

Similarly using KCL on operating modes of DSL-HBSC, the following average and peak switch current stresses are obtained.

$$\left.\begin{aligned} I_{S1}&=D(I_{L1}+I_{L2})\\ I_{S2}&=DI_{L1}\end{aligned}\right\} \tag{7.13}$$

$$\left.\begin{aligned} \hat{I}_{S1}&=(I_{L1}+I_{L2})+\left(\frac{\Delta I_{L1}+\Delta I_{L2}}{2}\right)\\ \hat{I}_{S2}&=I_{L1}+\frac{\Delta I_{L1}}{2}\end{aligned}\right\} \tag{7.14}$$

Where

$$\left.\begin{aligned} \Delta I_{L1}&=\left(\frac{V_i+V_{C1}}{L_1}\right)\frac{D}{f_s}\\ \Delta I_{L2}&=\left(\frac{V_{C1}}{L_2}\right)\frac{D}{f_s}\end{aligned}\right\}$$

7.2.5 Inductor and Capacitor Design

The inductors L_1 and L_2 can be designed by assuming an allowable ripple content (%x) in their average currents and similarly the capacitors (C_0-C_2) are also designed with the assumption of suitable peak-to-peak ripple voltage (%y) across them. The following expressions are the guide lines for the inductor and capacitor design.

$$L_1=\frac{(V_i+V_{C1})D}{(\%x_1)\,I_{L1}f_s}=\frac{2D(1-D)V_i^2}{(1-2D)(\%x_1)\,P_0f_s} \tag{7.15}$$

$$L_2=\frac{(V_{C1}-V_{C2})D}{(\%x_2)\,I_{L2}f_s}=\frac{D(1+D)V_i^2}{(1-2D)^2(\%x_2)\,P_0f_s} \tag{7.16}$$

Similarly

$$C_1=\frac{(I_{L1}+I_{L2})DT_s}{(\%y_1)V_{C1}}=\frac{(D)(2-D)(1-2D)P_0}{(\%y_1)(1+D)\,V_i^2f_s} \tag{7.17}$$

$$C_2=\frac{(I_{L2})DT_s}{(\%y_2)V_{C2}}=\frac{(1-2D)^2P_0}{(\%y_2)(1+D)\,V_i^2f_s} \tag{7.18}$$

$$C_0=\frac{(I_0)DT_s}{(\%y_0)V_0}=\frac{D(1-D)^2P_0}{(\%y_0)(1+D)^2\,V_i^2f_s} \tag{7.19}$$

7.2.6 Parasitics influence on Output Voltage and Efficiency

The aforementioned analysis is carried out under the assumption that all elements are ideal but in practical case numerous element parasitics will act and have a crucial role in the evaluation of converter voltage gain and efficiency. The element parasitics such as resistive nature of mosfet ($R_{DS\text{-}on}$), diode forward voltage drop followed by series equivalent resistance (ESR) of inductors and capacitors (termed as r_s, V_D, r_D, r_L, and r_c respectively) are now being considered to evaluate the performance indices specifically voltage gain and efficiency of DSL-HBSC as shown in Figure 7.3 (a).

The following (7.20) and (7.21) are the applied voltage for the inductor L_1 in time periods DT_S and $(1\text{-}2D)T_S$ under the influence of element parasitics

$$\left.\begin{aligned} v_{L1}&=V_i-I_{L1}r_L-(I_{L1}+I_{L2})r_s+v_{C1}-(I_{L1}+I_{L2})r_c\\ v_{L1}&=V_i-I_{L1}r_L-(I_{L1}+I_{L2})(r_c+r_D)-v_{C1}-2V_D \end{aligned}\right\}\rightarrow DT_S \tag{7.20}$$

$$v_{L1}=V_i-I_{L1}r_L-\left(\frac{I_{L1}}{2}\right)(r_c+r_D)-v_{C1}-2V_D\Big\}\rightarrow(1-2D)T_S \tag{7.21}$$

Using (7.20) and (7.21) for the volt-sec balance of inductor L_1

$$V_{C1}=\frac{V_i}{1-2D}-I_0r_L\left(\frac{1+D}{(1-2D)^2}\right)-I_0r_S\left(\frac{D(2-D)}{(1-2D)^2}\right)-I_0r_C\left(\frac{1+7D-6D^2}{2(1-2D)^2}\right)-I_0r_D\left(\frac{1-D+4D^2}{2(1-2D)^2}\right) \tag{7.22}$$

Since

$$V_0=V_{C1}(1+D) \tag{7.23}$$

The element parasitics influenced output voltage of DSL-HBSC-I converter is written as

$$V_{0\text{-}Parasitic}=\frac{\frac{V_i\,(1+D)}{1-2D}-V_D\left(\frac{2(1-D)}{1-2D}\right)}{1+a\left(\frac{r_L}{R_0}\right)+b\left(\frac{r_s}{R_0}\right)+c\left(\frac{r_c}{R_0}\right)+d\left(\frac{r_D}{R_0}\right)} \tag{7.24}$$

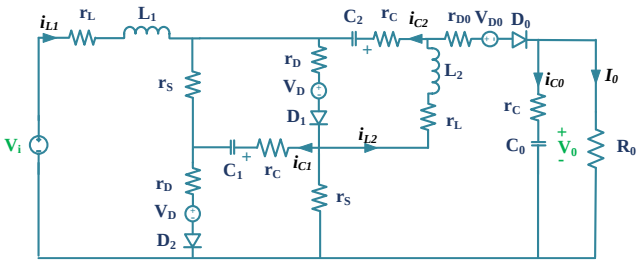
Where

$$a=\frac{(1+D)^2}{(1-2D)^2},\ b=\frac{D(2-D)(1+D)}{(1-2D)^2},c=\frac{1+8D+D^2-6D^3}{2(1-2D)^2},d=\frac{1+3D^2+4D^3}{2(1-2D)^2}$$

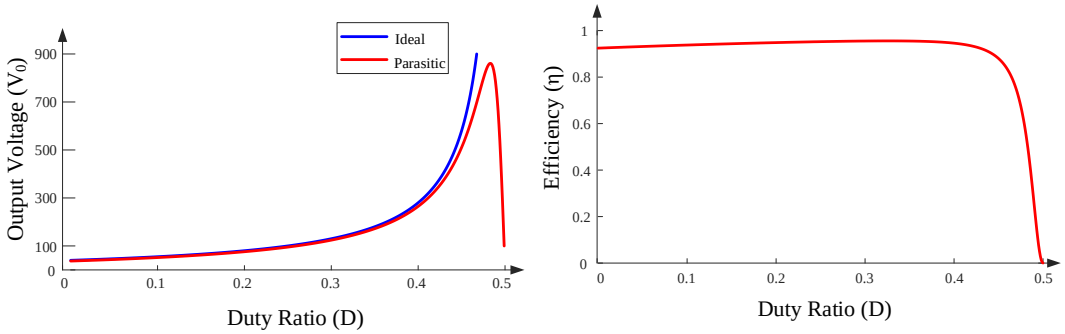
Using (7.24) the efficiency of the converter is written as

$$\eta = \frac{1 - V_D\left(\frac{2(1-D)}{V_i\,(1+D)}\right)}{1 + a\left(\frac{r_L}{R_0}\right) + b\left(\frac{r_S}{R_0}\right) + c\left(\frac{r_C}{R_0}\right) + d\left(\frac{r_D}{R_0}\right)} \tag{7.25}$$

The output voltage and efficiency variation with respect to the duty ratio is shown in Figure. 7.3 (b) and (c). The conclusive remarks from these plots are that the experimental efficiency and output voltage are in good accord with the evaluated values from (7.24) and (7.25).



(a)



(b) (c)

Figure 7.3. Parasitic influence (a) DSL-HBSC-I converter (b) $V_{0\text{-}Parasitic}$ and (c) η versus duty ratio.

7.2.7 Small Signal Modelling

The performance of the DSL-HBSC-I converter for dynamic variations in source voltage and load current is carried out by standard state space averaging method. A series ESR is accounted for capacitors and inductors in the control performance. The converter control variable is $d(t)$, $v_i(t)$ and $v_0(t)$ are considered as voltage variables, and the capacitor voltages ($v_{C1}(t)$, $v_{C2}(t)$ and $v_{C0}(t)$) followed by inductor currents ($i_{L1}(t)$ and $i_{L2}(t)$) are the state variables for the DSL-HBSC-I converter small signal modelling as specified in (7.26) and (7.27). A simple single loop PI controller is adopted as in (7.28) to get a steady output voltage against the perturbations in source voltage and load current.

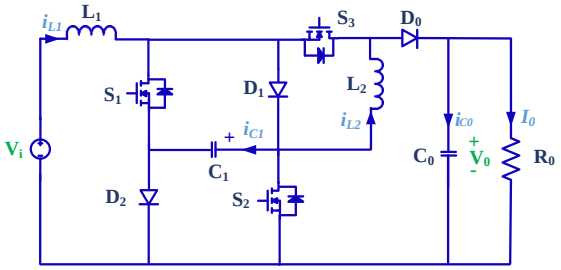
$$A=A_1D+A_2D+A_3(1\text{-}2D),B=B_1D+B_2D+B_3(1\text{-}2D),\ C=C_1D+C_2D+C_3(1\text{-}2D),$$
$$X=-A^{-1}BU,\quad F=\{(A_1+A_2)\text{-}2A_3\}X+\{(B_1+B_2)\text{-}2B_3\}U \tag{7.26}$$
$$G_{vd}=\frac{\hat{v}_o}{\hat{d}}=C(SI\text{-}A)^{-1}F+(C_1+C_2\text{-}2C_3)X$$

$$\begin{bmatrix}\frac{d\hat{i}_{L1}(t)}{dt}\\ \frac{d\hat{i}_{L2}(t)}{dt}\\ \frac{d\hat{v}_{c1}(t)}{dt}\\ \frac{d\hat{v}_{c2}(t)}{dt}\\ \frac{d\hat{v}_{c0}(t)}{dt}\end{bmatrix}=\begin{bmatrix}\frac{-6r_L+5r_c}{2L_1} & \frac{-r_c}{L_1} & \frac{-(1\text{-}2d)}{L_1} & 0 & 0\\ \frac{-5r_c}{2L_2} & \frac{-(2r_L+3r_c)}{2L_2} & \frac{(1\text{-}d)}{L_2} & \frac{-2d}{L_2} & -(1\text{-}2d)\left(1+\frac{r_L+r_c}{R_0}\right)\\ \frac{(1\text{-}2d)}{2C_1} & \frac{-d}{C_1} & 0 & 0 & 0\\ \frac{-(1\text{-}2d)}{2C_2} & \frac{2d}{C_2} & 0 & 0 & \frac{-(1\text{-}2d)}{C_0R_0}\\ \frac{(1\text{-}2d)}{2C_0} & 0 & 0 & 0 & \frac{-1}{C_0R_0}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}(t)\\ \hat{i}_{L2}(t)\\ \hat{v}_{c1}(t)\\ \hat{v}_{c2}(t)\\ \hat{v}_{c0}(t)\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1}\\ 0\\ 0\\ 0\\ 0\end{bmatrix}\hat{v}_i(t)+\begin{bmatrix}-\left(\frac{r_c}{L_1}+\frac{2(d\text{-}1)r_L}{L_1}\right) & \frac{-r_c}{L_1} & \frac{2}{L_1} & 0 & 0\\ \frac{(\text{-}3+4d)r_c}{L_2} & \frac{-(2r_L+3r_c)d}{L_2} & \frac{-1}{L_2} & \frac{-2}{L_2} & 2\left(1+\frac{r_L+r_c}{R_0}\right)\\ \frac{-1}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0\\ \frac{1}{C_2} & \frac{2}{C_2} & 0 & 0 & \frac{1}{C_0R_0}\\ \frac{-1}{C_0} & 0 & 0 & 0 & 0\end{bmatrix}\begin{bmatrix}I_{L1}\\ I_{L2}\\ V_{C1}\\ V_{C2}\\ V_{C0}\end{bmatrix}\hat{d} \tag{7.27}$$

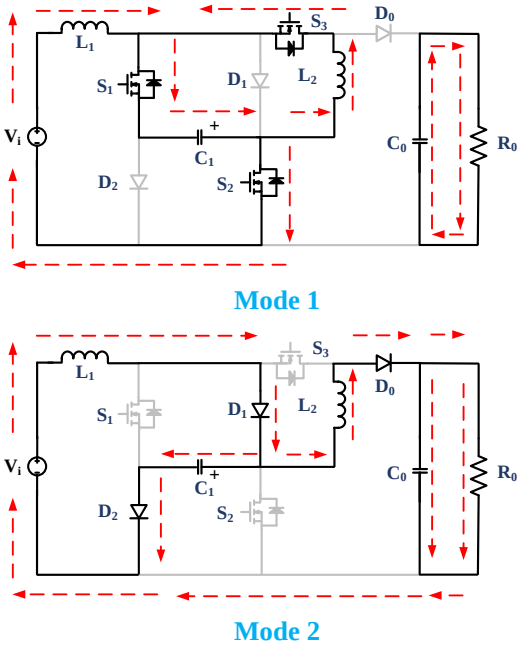
$$\hat{v}_{c0}(t)=[0\quad 0\quad 0\quad 0\quad 1][\hat{i}_{L1}(t)\quad \hat{i}_{L2}(t)\quad \hat{v}_{c1}(t)\quad \hat{v}_{c2}(t)\quad \hat{v}_{c0}(t)]^T$$

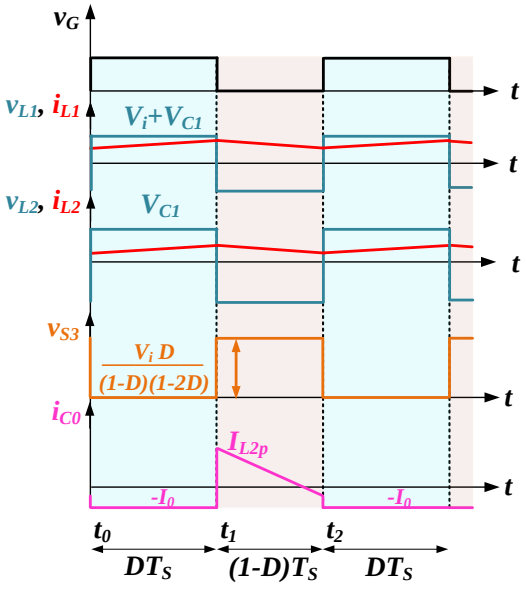
$$\left.\begin{aligned}K_P&=0.00025\\ K_I&=0.054\end{aligned}\right\} \tag{7.28}$$

7.3 Case Study



(a)





(b) (c)

Figure 7.4. DSL-HBSC-II converter (a) topology (b) operating modes (c) operating waveforms.

It can be observed from Figure 7.2 (b) that the capacitor C_0 is conducting for a short interval $(1\text{-}2D)T_S$. Moreover, in this duration the peak value of capacitor current i_{C0} is high. As a remedial measure to reduce this peak current stress a modified DSL-HBSC-II topology is proposed by replacing the capacitor C_2 with a switch S_3 as shown in Figure 7.4 (a). This converter is operating in two different modes for a duration of DT_S and $(1\text{-}D)T_S$ as shown in Figure 7.4 (b) and the ideal operating waveforms are represented in Figure 7.4 (c). A similar analysis as mentioned in DSL-HBSC-I converter is carried out and the CCM voltage gain is expressed as follows.

$$G\left(\frac{V_0}{V_i}\right)=\frac{(1/1\text{-}D)}{1\text{-}2D} \tag{7.29}$$

The following Table 7.1 represent the semiconductor element voltage and current stresses that are obtained by writing KVL and KCL for the conducting loops as shown in Figure 7.4 (b).

Table 7.1 voltage and current stress

Voltage Stress		Current Stress (Average)
Switches	**Diodes**	**Switches**
$V_{S1}=V_{S2}=V_{C1}=\frac{V_i}{1\text{-}2D}$ $=V_0\,(1\text{-}D)$	$V_{D1}=V_{D2}=V_{C1}=\frac{V_i}{1\text{-}2D}$ $=V_0\,(1\text{-}D)$	$I_{S1}=I_{L1}+I_{L2}=D\left(\frac{2I_0}{1\text{-}2D}\right)$
$V_{S3}=V_0\text{-}V_{C1}=\frac{V_1\,D\,(1/1\text{-}D)}{1\text{-}2D}$ $=V_0\,D$	$V_0+V_{C1}=\frac{V_i\,(2\text{-}D)\,(1/1\text{-}D)}{1\text{-}2D}=V_0$ $(2\text{-}D)$	$I_{S2}=I_{L1}=D\left(\frac{I_0}{(1\text{-}D)(1\text{-}2D)}\right)$ $I_{S3}=I_{L2}=D\left(\frac{I_0}{1\text{-}D}\right)$

7.4 Experimental Results

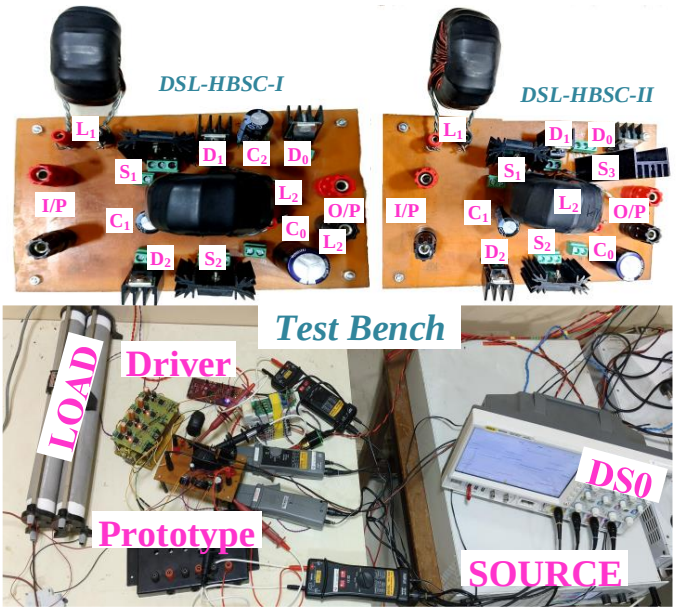


Figure 7.5. Proposed DSL-HBSC converters and test bench

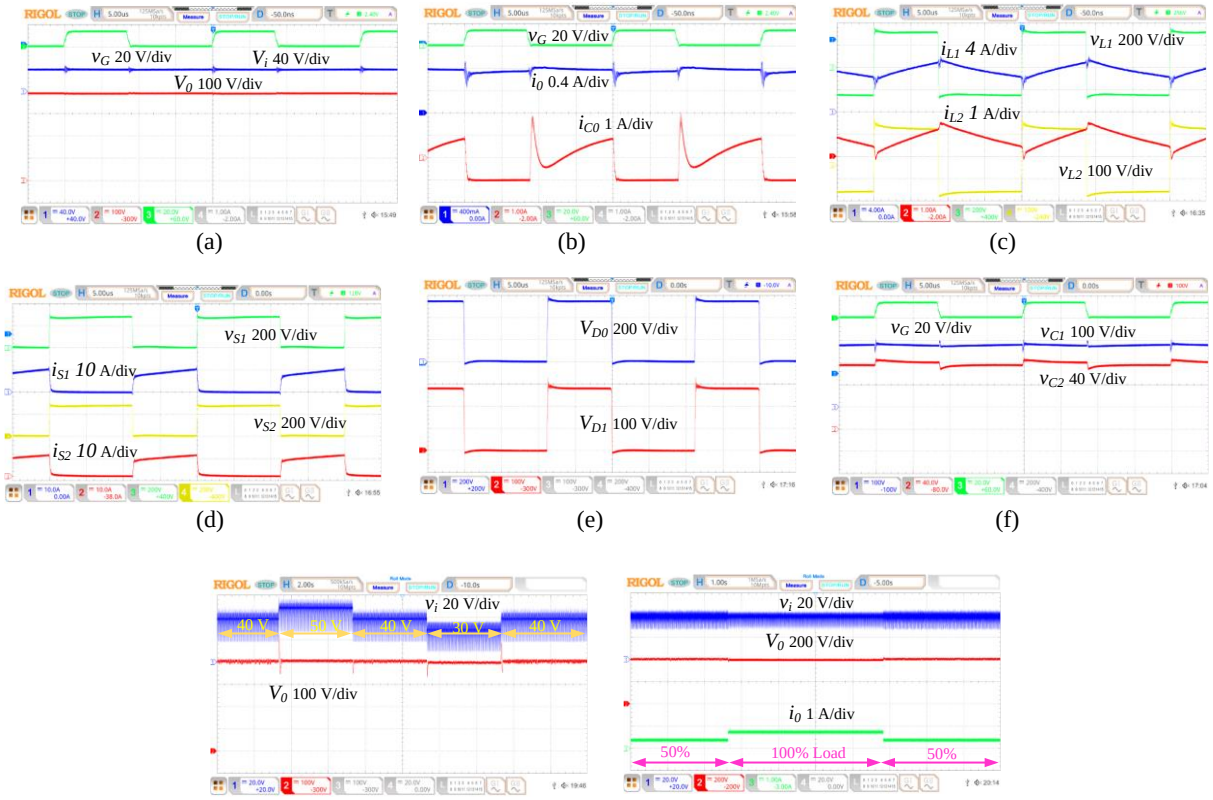


Figure 7.6. DSL-HBSC-I converter experimental results for 200 W (a) input and output voltages (v_i and v_0) (b) load and capacitor C_0 currents (i_0 and i_{C0}) (c) inductor voltages and currents (v_L and i_L) (d) switch voltages and currents (v_S and i_S) (e) diode voltages (v_{D0} and v_{D1}) (f) capacitor voltages (v_{C1} and v_{C2}); closed loop validation (g) stepped v_i and (h) stepped i_0.

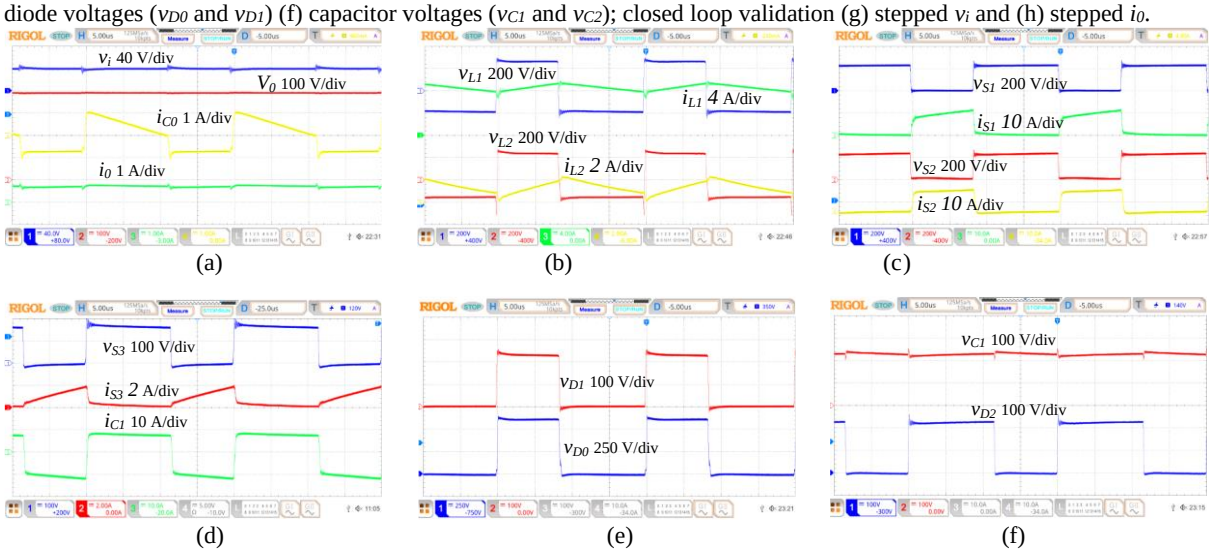


Figure 7.7. DSL-HBSC-II converter experimental results for 200 W (a) input and output voltages-currents (v_i, v_0, i_{C0} and i_0) (b) inductor voltages and currents (v_L and i_L) (c) switch voltages and currents ($v_{S1/2}$ and $i_{S1/2}$) (e) switch S_3 voltage-current and capacitor C_1 current (v_{S3} and i_{S3}; i_{C1}) (f) diode voltages (v_{D0} and v_{D1}) (f) diode D_2 and capacitor voltages (v_{D2} and v_{C1}).

A 400V/300W, prototype as shown in Figure 7.5 is developed for DSL-HBSC- I and II converters to experimentally validate the performance indices. The components which are used for experimentation are listed in Table 7.2. Both of the stated converters are operating at a input currents of 7.72 and 7.77 A for which the observed output voltage is 390 and 388 V as shown in Figure 7.6 and 7.7 (a). The aforementioned output voltages are obtained at a duty ratio of 0.429 and 0.415 with an average output current close to 0.74 A as shown in Figure 7.6

(b) and 7.7 (a) for the DSL-HBSC-I and II converters respectively. From the discussion it is clear that the respective operating efficiencies of both converters are 93.07% and 91.89%. The following discussion is carried out in two separate parts for the experiment validation of DSL-HBSC-I and II converters.

The inductor voltages and currents are in good accord with the ideal wave shapes and are simultaneously charging and discharging with an average current of 7.72 and 0.78 A as shown in Figure 7.6 (c). The switch voltages and currents are as shown in Figure 7.6 (d) and it can be observed from the Figure that both the switches are operating at a voltage stress of 70% of output voltage V_0. The diode voltage stresses D_1 and D_2 are identical and hence only V_{D1} is represented in Figure 7.6 (e) which is at a voltage stress of 0.7 V_0. The diode D_0 voltage stress is twice of V_{C1} as shown in Figure 7.6 (e). Moreover, from Figure 7.6 (f) it is observed that the capacitor voltage stresses are in good accord with their ideal conditions. The closed loop validation of DSL-HBSC-I converter is reported in Figure 7.7 (g) and (h) for a stepped source voltage (40V-50V-40V-30V-40V) and stepped load of condition (50%), which validates the proposed converter ability to maintain a constant output voltage.

The key features of DSL-HBSC-II converter are reported in Figure 7.7. The performance indices at input and output ports are as shown in Figure 7.7 (a) with no inrush at each interval starting for capacitor current i_{C0}. This feature is the crucial achievement of DSL-HBSC-II compared to DSL-HBSC-I converter. The charge and discharge profile of inductors L_1 and L_2 are as shown in Figure 7.7 (b) with a peak-to-peak ripple current of 1.6 A. The switches S_1 and S_2 stresses are analogous to DSL-HBSC-I converter and it is as shown in Figure 7.7 (c). The performance indices of switch S_3 and capacitor C_1 i.e., V_{S3}, i_{S3} and i_{C1} are reported in Figure. 7.7 (d), which concludes that there exist only two set of state variables (DT_S and $(1\text{-}D)T_S$) in small signal modelling of DSL-HBSC-II converter. Furthermore, the diode and capacitor (C_1) voltage stresses are as reported in Figure 7.7 (e) and (f), which are in par with their steady state conditions. Moreover, the ideal findings of the stated converters based on the simulation platform are reported in Figure 7.8 and 7.9. Additionally, the following Figure 7.10 emphasizes efficiency variation and standard loss distribution of proposed converters at rated power 300 W.

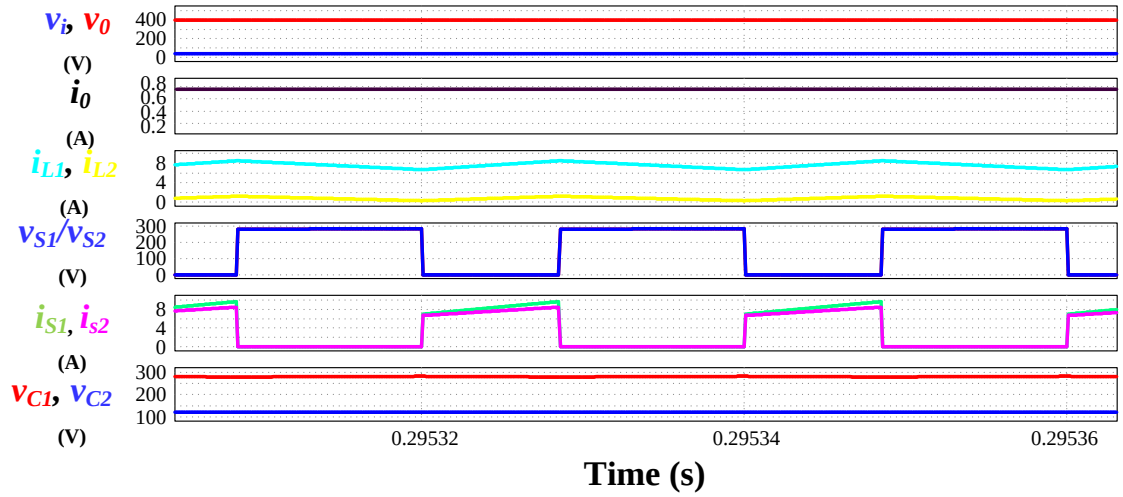


Figure 7.8. Simulated results of DSL-HBSC-I converter

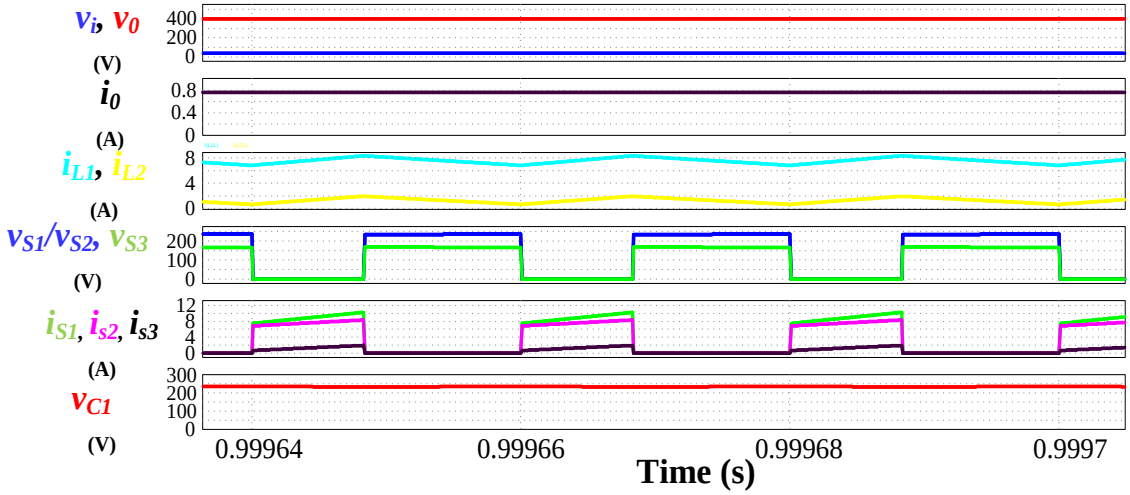


Figure 7.9. Simulated results of DSL-HBSC-II converter

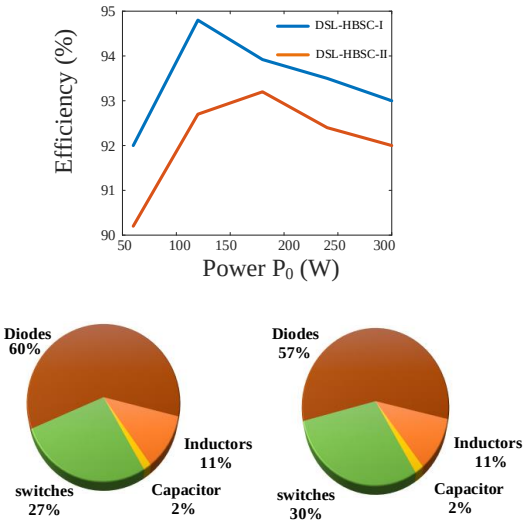


Figure 7.10. Efficiency and loss distribution of proposed converters

Table 7.2 Design Specifications

Specification	Rating
Input voltage	40 V
Output Voltage	400 V
Power	300 W
Inductors	$L_1 = L_2 = 1.5$ mH
capacitors	$C_1 = C_2 = 22$ μF, $C_0 = 100$ μF
Diodes	D_0 (STPSC10H065DI) D_1, D_2 (MUR 1560G)
Switches	S_1, S_2 (FCH072N60F)

7.5 Performance Comparison

The features and performance indices of DSL-HBSC-I and II converters are compared and presented in Table 7.3 and Figure 7.11. The selective performance indices for comparison are voltage gain, effectiveness index (EI) and input current ripple in per unit, normalized semiconductor (diodes (NDVS), switches (NSVS) and total (NTVS)) voltage stress, element count and operating conditions (η, P and f_s).

The first and foremost parameter of comparison is voltage gain and EI. The converters [114], [116] and [117] are having improved voltage gain compared to the proposed converters but their overall component count is high. In this regard the factor EI is considered which emphasizes the converters [114] and [116] performance is in par with the proposed converters as shown in Figure 7.11 (a). The subsequent parameter of discussion is normalized semiconductor voltage stress, in this regard the DSL-HBSC-I and II converters performance is moderate as shown in Figure 7.11 (b), (c) and (d). This is because of the fact that the output diode D_0 has a voltage stress more than V_0 which degrades the converter performance in terms of NDVS, NSVS and NTVS. The source current ripple ($\Delta I_i/I_i$) is made as low as possible to suit the numerous applications in this concern as shown in Figure 7.11 (e). From the Figure7.11 (e) it is observed that the two proposed converters performance is superior with a ripple content of 20%. The other miscellaneous features of the DSL-HBSC converters are common ground, initial inrush free continuous input current (as in [116]). The proposed converters operating efficiency and switching frequency are also superior in view of the inductor sizing. The stated two converters overall element count is low except the converter in [116] but it has high initial inrush for the input current and its voltage gain is not superior as shown in Figure 7.11 (a). A comparison study reflecting the differentiation between the simulated and experimental findings is reported in Table 7.4.

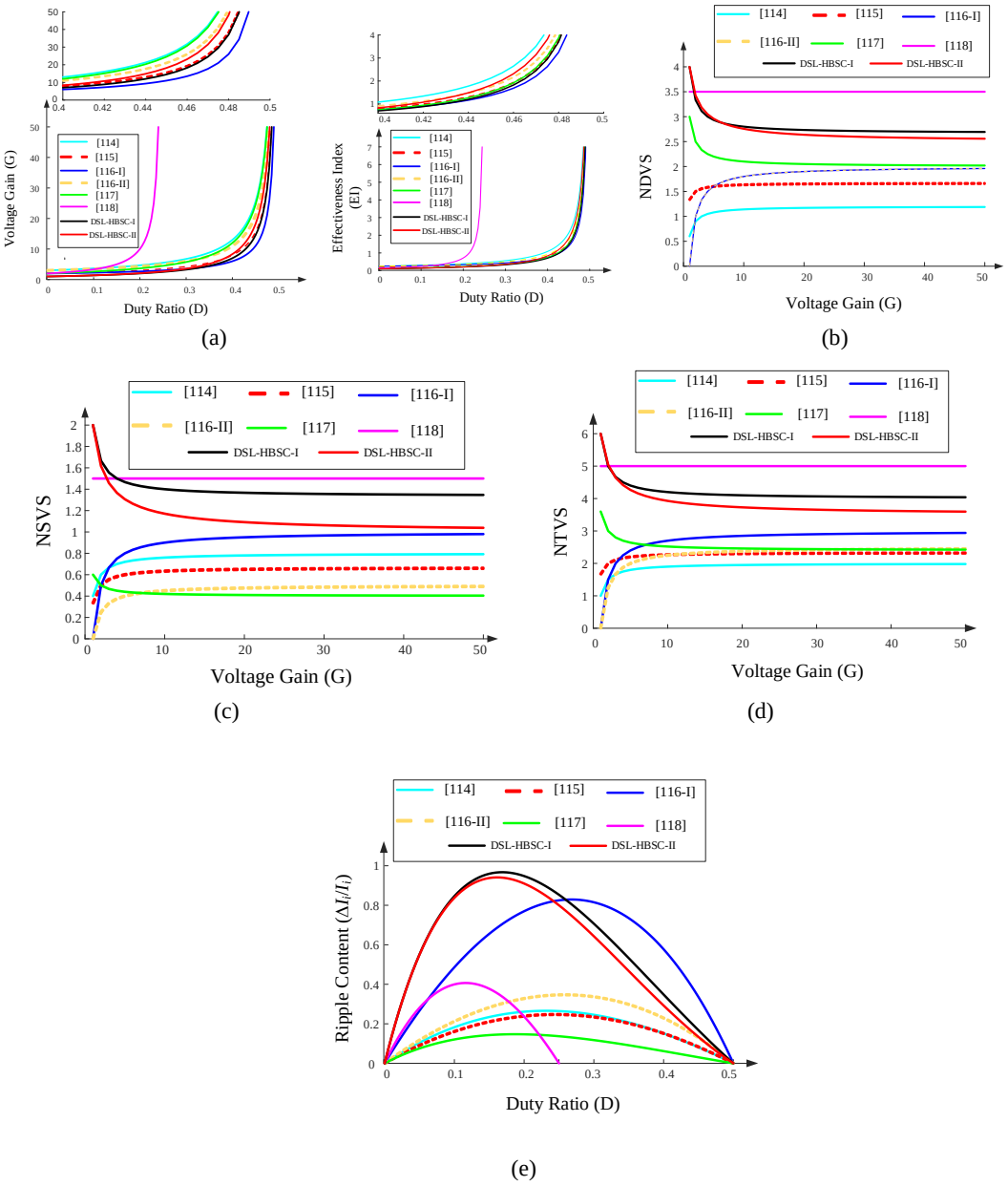


Figure 7.11. Proposed converters performance comparison (a) *G* and *EI* versus *D* (b) *NDVS* versus *G* (c) *NSVS* versus *G* (d) *NTVS* versus *G* and (e) per unit source current ripple versus duty.

Table7.3 Performance Comparison

Converter	Voltage Gain (G)	NDVS	NSVS	NTVS	Element Count C/L/D/S (Total)	Source current Ripple (ΔIi)	Common Ground	Continuous input current	η, P and fs
[114]	$\frac{3-D}{1-2D}$	$\frac{3(2G-1)}{5G}$	$\frac{2(2G-1)}{5G}$	$\frac{(2G-1)}{G}$	4/3/3/2 (12)	LOW	YES	YES	92%, 300 W And 50 kHz
[115]	$\frac{2-D}{1-2D}$	$\frac{5G-1}{3G}$	$\frac{2G-1}{3G}$	$\frac{7G-2}{3G}$	4/2/3/1 (10)	LOW	YES	YES	87%, 100 W And 50 kHz
[116-I] Improved QZSC	$\frac{2(1-D)}{1-2D}$	$\frac{2(G-1)}{G}$	$\frac{(G-1)}{G}$	$\frac{3(G-1)}{G}$	3/2/2/1 (8)	LOW (High initial inrush)	YES	YES	95%, 150 W And 10 kHz
[116-II] Improved SC-QZSC	$\frac{3-2D}{1-2D}$	$\frac{4(G-1)}{2G}$	$\frac{(G-1)}{2G}$	$\frac{5(G-1)}{2G}$	5/2/4/1 (12)	LOW (High initial inrush)	YES	YES	96%, 150 W And 10 kHz
[117]	$\frac{2+D}{1-2D}$	$\frac{5(2G+1)}{5G}$	$\frac{(2G+1)}{5G}$	$\frac{(12G+6)}{5G}$	7/3/5/1 (16)	LOW	NO	YES	91%, 150 W And 40 kHz
[118]	$\frac{2}{1-4D}$	3.5	1.5	5	5/2/5/2 (14)	LOW	YES	YES	89.7%, 200 W And 30 kHz
DSL-HBSC-I	$\frac{1+D}{1-2D}$	$\frac{4(2G+1)}{3G}$	$\frac{2(2G+1)}{3G}$	$\frac{2(2G+1)}{G}$	3/2/3/2 (10)	LOW	YES	YES	93.07%, 300 W And 50 kHz
DSL-HBSC-II	$\frac{(1/1-D)}{1-2D}$	4-3D	2-2D $D=\frac{3-\sqrt{1+(8/G)}}{4}$	6-5D	2/2/3/3 (10)	LOW	YES	YES	91.89%, 300 W And 50 kHz

Table 7.4 Performance comparison of simulation and experimental findings of DSL-HBSC converters

Performance Indices	DS-HBSC-I		DSL-HBSC-II	
	Simulation	Experimental	Simulation	Experimental
Output voltage (V_0)	400 V	390 V	400 V	388 V
Output current (I_0)	0.75 A	0.74 A	0.75 A	0.74 A
Input current (I_i)	7.5 A	7.72 A	7.6 A	7.77 A
Inductor currents (I_{L1} & I_{L2})	7.5 A & 0.75 A	7.72 A & 0.78 A	7.6 A & 1.3 A	7.77 A & 1.1 A
Switch voltage stresses	282 V & 282 V ($\hat{V}_{S1}$ & $\hat{V}_{S2}$)	295 V & 290 V ($\hat{V}_{S1}$ & $\hat{V}_{S2}$)	236 V, 236 V & 166 V ($\hat{V}_{S1}$, $\hat{V}_{S2}$ & $\hat{V}_{S3}$)	237 V, 240 V & 202 V ($\hat{V}_{S1}$, $\hat{V}_{S2}$ & $\hat{V}_{S3}$)
Switch current stresses	9.62 A & 8.44 A ($\hat{I}_{S1}$ & $\hat{I}_{S2}$)	10. 5 A & 10 A ($\hat{I}_{S1}$ & $\hat{I}_{S2}$)	10 A, 8.2 A & 1.8 A ($\hat{I}_{S1}$, $\hat{I}_{S2}$ & I_{S3})	12 A, 9A & 2 A ($\hat{I}_{S1}$, $\hat{I}_{S2}$ & I_{S3})
Capacitor voltage stress	281 V & 120 V (C_1 & C_2)	280 V & 118 V (C_1 & C_2)	235 V (C_1)	233 V (C_1)

7.6 Summary

A dual switched inductor-switched capacitor based topologies are evaluated in this article. The front-end single inductor-H bridge switched capacitor ensures a boosting factor similar to Quasi-Z-Source converter. Additionally, the embedded modified SEPIC structure with simpler means of C_1-L_2- C_2 enhances the boosting factor further to suit the stated 400V requirement. The high peak current of output capacitor in DSL-HBSC-I converter is abbreviated by means of a third switch in DSL-HBSC-II converter with low source current ripple and common ground. Moreover, a performance indices comparison between the proposed topologies and low duty based high gain dc-dc converters is also reported to give insight on the topological benefits.

Chapter 8

Conclusions and Future Scope

8. Conclusion and Future Scope

The pertaining research works on prominent and elegant nonisolated dc-dc converters with prime focus on attaining high voltage gains at low duty ratios are evaluated in this thesis. The stated research work contributions are the design, development, and validation of simple, robust, economical and ease of control based high boost dc-dc converters. These research endeavors are in comply with the notable applications of dc micro grids and hybrid energy source based electrical propulsion systems. The following section summarize the thesis incorporated research works outcome.

8.1 Conclusion

A split duty based NSDC is proposed for low and medium power applications of dc micro grid. The proposed converter reduces the elevated conduction intervals for the switches with the aid of split in duty thus reducing the average conduction period, thereby the cooling requirements for the switches are less and they are less prone to failure with high reliability. Moreover, in the second switching state the inductors are having a total input voltage as excitation therefore the stored energy in the inductors is increased which subsequently enhances the output voltage. A notably high boost factor is achieved without the state-of-the-art voltage lifting techniques, voltage multiplier cells and transformer. The proposed converter is simple and economical featuring low voltage stresses. A comparative study has been reported to validate the proposed converter performance indices which are in par with the current evolved topologies on split duty converters.

An active switched capacitor-switched inductor integrated quadratic boost converters are explored in this thesis. The proposed converters rear end inductor possesses inherent features of high input excitation because of the diode capacitor voltage lift arrangement associated with the primary switch. This makes the converter to attain the ultra-high voltage gain at moderate duty ratio and low voltage-current stresses. Furthermore, an extension to the initial topology is also reported by improving the excitation to the rear end inductor with aid of replicating the diode capacitor voltage lift arrangement for the load end switch there by enhancing voltage gain and reducing the duty ratio further. The major demerits of these topologies are lack of common ground between the source and sink terminals. To surpass this concern a switched capacitor based quadratic boost converter featuring low rear end diode voltage stress is reported in this thesis. The prime emphasis of the proposed converter is to have a limited number of forward path semiconducting elements so that the concerned voltage drop associated is lowered. Additionally, the stated converter also features an absolute common

ground along with ultra-high voltage gain at moderate duty ratio, reduced per unit source current ripple and low surface voltage standing on the converter. To comply with the ultra-voltage gain requirements in dc micro grids and EVs, an experimental demonstration of the proposed converter for 20 V to 800 V conversion is also validated.

The high and ultra-high voltage gain are often associated with the adverse effects like elevated duty ratios, high voltage-current stresses on semiconductors, degraded thermal aspects and low efficiency. An alternate approach for this concern apart from quadratic boost converter is to design a converter whose voltage gain is high at low duty by having an upper bound on it i.e., low duty based analogous Z-Source or Quasi Z Source converters (QZS). The discontinuous input current for Z-Source converters and moderate voltage gain even after integrating two inductors in QZS converters are the major short falls of these converter family. Thus, a single primary inductor based Modified Sheppard Taylor dc-dc converter with integrated SEPIC arrangement is proposed to surpass the aforementioned shortfalls and to comply with the high voltage gain requirements. A simple adjustment consisting of a replacement for intermediate capacitor by a switch in the subsequent proposed converter will further enhances the voltage gain and most importantly it reduces the high inrush currents of output capacitor by retaining the features of low input current ripple, an absolute common ground, low surface voltage stress standing on the converter, and improved efficiency.

The state-of-the-art bidirectional dc-dc converters demand the requirements of achieving extreme amplification and attenuation in the respective power flow paths to suit the applications of hybrid energy source driven electric propulsion systems. The stated high voltage gain is attained by designing a quadratic boost-buck converter featuring a common ground, low source ripple current content and most importantly moderate voltage stress on the semiconductors. The steady state and dynamic performance of the proposed converter are superior over a wide input voltage range at the low voltage port. Therefore, it is suitable for the application of battery or hybrid energy source and super capacitor bank connected bidirectional dc-dc converters in modern EVs.

In order to streamline the major outcomes of the listed contributions in this thesis, a comparison study is carried out as reflected in the Table 8.1. The stated comparison comprises of the crucial performance indices namely, voltage amplification factor, voltage gain attained at the operating conditions, power rating of the converters followed by the merits and demerits of the concerned converter to suit the intended application.

Table 8.1 Specific outcomes of listed contributions

	Contribution 1	Contribution 2	Contribution 3	Contribution 4	Contribution 5
Voltage gain	7.5 (High)	20 (Ultra-High)	20 (Ultra-High)	6 & 10 (High)	10 (High)
Power rating	150 W	100 W	200 W	200 W	300 W
Significant outcome	Split duty	Quadratic Gain	Quadratic Gain	Bidirectional Quadratic Boost-Buck Gain	Quasi Z-Source analogous gain
Merits	Low peak switch current stress	Low semiconductor voltage stress	Low semiconductor voltage stress & Low input current ripple	Low semiconductor voltage stress & Low input current ripple	Low input current ripple
Demerits	High semiconductor voltage- current stress	High peak switch current stress for ASCQBC-II	Moderate element count	Absence of continuous current at HV port	High semiconductor voltage stress

8.2 Future scope

The research works in this thesis evaluated nonisolated dc-dc converters for dc microgrids and EVs. Based on the topologies proposed, the future scope of these works includes the following.

1. The proposed works can be extended to coupled inductor based converter topologies to further optimize the spacing constraints.

2. All the proposed works are implemented for soft switching methodologies i.e., zero voltage switching and zero current switching which further reduces the switching

losses at high frequencies and also reducing the space and size concerns of energy storage elements.

3. The control aspects can be further revisited for the possible adoption of advanced controllers to attain high transient switching response.
4. The nonminimum phase nature of the stated topologies can be altered to minimum phase nature by providing a possible short duration interval of free wheeling for the inductors.

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3. **M. F. Baba,** A. V. Giridhar and B. L. Narasimharaju, "A Wide Voltage Range Bidirectional High Voltage Transfer Ratio Quadratic Boost DC-DC Converter for EVs With Hybrid Energy Sources," in ***IEEE Journal of Emerging and Selected Topics in Industrial Electronics***, vol. 5, no. 2, pp. 521-530, April 2024.

4. **M. F. Baba,** A. V. Giridhar, B. L. Narasimharaju,and Harish S krishnamoorthy " An Ultra High Gain Switched-Capacitor Boost DC-DC converter with Reduced Ripple Current," in ***IEEE Latin America Transactions*** (Accepted).

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