Design and Implementation of Compact High Performance On-chip Multilayer IPD Inductors for 5G Applications

submitted in partial fulfillment of the

requirements for the award of the degree of

Doctor of Philosophy

by

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APPROVAL SHEET

This Dissertation Work entitled **"Design and Implementation of Compact High Performance On-chip Multilayer IPD Inductors for 5G Applications"** by **Machavaram Venkata Raghunadh, Roll No. 718083** is approved for the degree of Doctor of Philosophy.

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DECLARATION

This is to certify that the work presented in the thesis entitled **"Design and Implementation of Compact High Performance On-chip Multilayer IPD Inductors for 5G Applications"** is a bonafide work done by me under the supervision of **Prof. N. Bheema Rao**, **Professor,** Department of Electronics and Communication Engineering, National Institute of Technology, Warangal and was not submitted elsewhere for the award of any degree.

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CERTIFICATE

This is to certify that the thesis entitled "**Design and Implementation of Compact High Performance On-chip Multilayer IPD Inductors for 5G Applications**" is being submitted by **Mr. Machavaram Venkata Raghunadh (Roll No. 718083)**, in partial fulfilment for the award of the degree of Doctor of Philosophy to the Department of Electronics and Communication Engineering of National Institute of Technology Warangal, is a record of bonafide research work carried out by him under my supervision and guidance and has not been submitted elsewhere for any degree.

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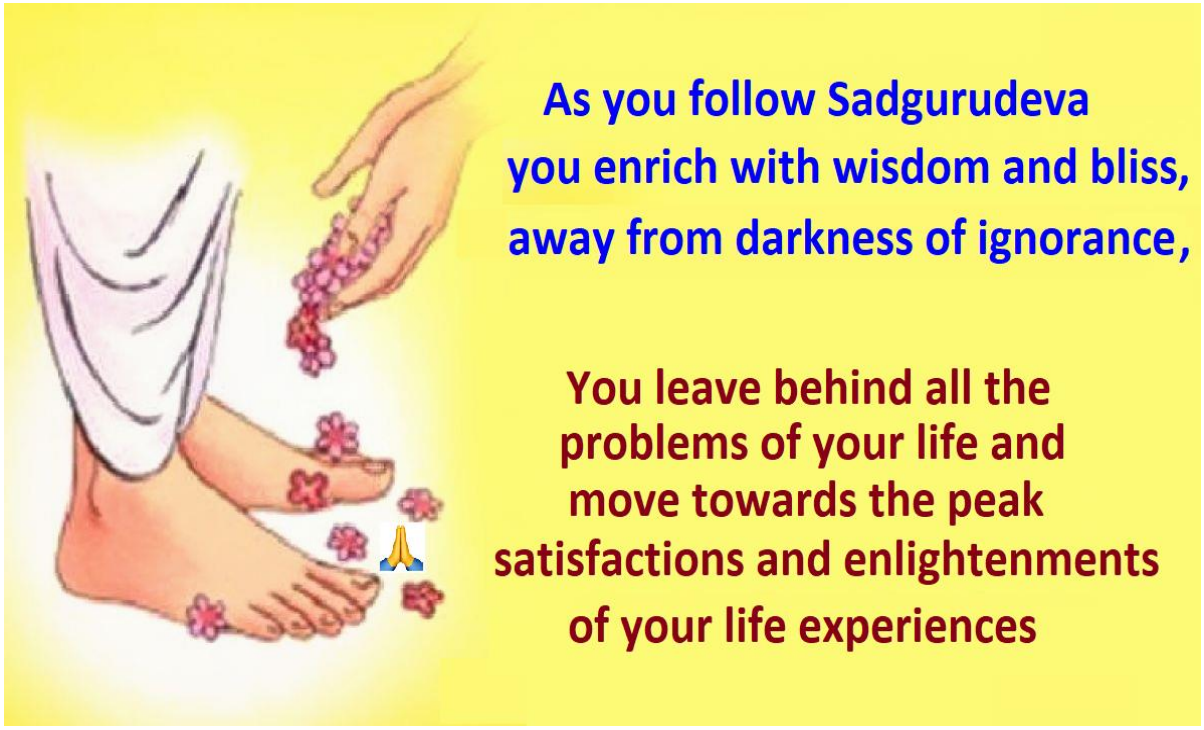
Dedicated to my beloved

Sadgurudattadeva Parama Pujya HH

SRI GANAPATHI SACHCHIDANANDA SWAMIJI



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Machavaram Venkata Raghunadh

ABSTRACT

Today's information centric world is witnessing a massive 5G proliferation, with an explosion of 5G devices in multitude of 5G applications like mobile cellular networks, Wireless local area network (WLAN), Internet of Things (IOT), smart systems, Vehicle to Vehicle (V2V), Machine to machine (M2M), Global Positioning System (GPS) navigation etc. Spectacular growth and worldwide deployment of 5G communication networks, spurred the need to design and develop very compact and yet high-performance on-chip passive inductors and capacitors, which facilitate the co-location of analog and digital components on the same chip.

In literature, successful radio frequency front end (RFFE) circuits prominently used the low-cost Complementary Metal oxide Semiconductor (CMOS) technology. Integrated Passive Device (IPD) technology based on-chip inductors and capacitors became indispensable, beyond 1 GHz due to their noise and power advantages. On-chip IPD passives play vital role in the miniaturization of the key performance deciders like voltage control oscillator (VCO), low noise amplifier (LNA), bandpass filter (BPF). Offchip IPD technology easily integrates with CMOS 5G radio frequency integrated circuits (RFIC) and system on-chip (SOC) to realize the low-cost 5G RFFE circuits.

The design of on-chip passives need trade-off between the cost of technology provisions and application demands, posing several challenges like design complexity, high quality factor, least on-chip area and fabrication costs. The spiral geometry passives became attractive as they exhibit large values of inductance, capacitance and moderate quality factors. In this thesis, the attractive multilayer spiral geometry is adopted not only to obtain larger values of inductance, self-resonant frequency (SRF) and quality factor (Q), but also to reduce the size of on-chip passive components. The multilayer inductor structure is developed based on vertical stacking concept (multilevel) of metal layers.

Initially, the constant width and variable width series stacked spiral inductors are proposed. The variable width of the metal decreases the series resistance and series stacking increases the metal trace length. It also helps to reduce the skin and proximity effects and up-down series stacking reduces the parasitic capacitance. Thus, it attains high Q and inductance over the standard planar inductor. A novel series stacked double-split structure is proposed to split the conductor metal path in all the layers. Optimal selection of the double-split track width

helps to reduce the skin and proximity effects, overall parasitic capacitance. Thus increases the Q value and SRF of the inductors. In this thesis, a planar spiral capacitor is developed in single layer. The sensitivity analysis of spiral capacitor gives a trade-off between electrical response and layout parameters.

Mathematical validation of on-chip passives is a key mechanism to justify the validity of proposed models. Frequency dependent and independent analytical expressions used to extract the inductance value, show much deviation in the extracted inductance values at 5G frequencies. Numerically solved integral equations yielded smaller error.

The proposed IPD inductors and capacitor are used in the implementation of LNAs and BPFs for 5G applications. A narrow band 5GHz LNA is implemented by using the proposed IPD ML series stacked double-split inductor and standard inductor. Also two 5G bandpass filters at 8.2 GHz and 25 GHz are designed, simulated, fabricated and tested using proposed IPD inductors and capacitor to validate the simulation results.

Design and simulation of the proposed inductors and their applications are carried out by using High-Frequency Structural Simulator (HFSS), Advanced Design System (ADS), and Sonnet EM simulator. As fabrication facility on silicon substrate is not available, the proposed IPD inductors and capacitor are scaled down from GHz to MHz level (scaled up dimensionally from μm to mm level). They are fabricated on FR4 substrate for PCB manufacturing and testing of respective LNA and BPF performance.

The proposed novel series stacked double-split multilayer IPD spiral inductors at different 5G frequencies had exhibited 325% improvement in inductance and a 68% increase in quality factor value for the equivalent on-chip area 0.0324 mm^2 compared to the standard spiral inductor at 5.5 GHz. The proposed novel double-split IPD inductor based LNA has improved the parameters like S_{11}, S_{21}, NF and Stability by 64%, 75%, 74%, and 129% respectively, over the CMOS Inductor. An 8.2 GHz BPF employing the proposed double-split IPD inductor has enhanced the loaded Q, S_{11} and S_{12}, by 242%, 30.7%, and 85% respectively, over a similar UWB filter. The results from simulations performed, are in very good concurrence with the experimental results for all IPD inductors and capacitor. Hence, this performance equivalence has successfully validated the supremacy of the proposed very compact IPD inductors for 5G applications.

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List of Abbreviations

3D	Three Dimensional
5G	Fifth Generation
AMS	Analog/mixed signal
ADS	Advanced Design System
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BOM	Body On Mass
BPF	Bandpass Filter
CMOS	Complementary Metal Oxide Semiconductor
EBG	Electro Magnetic Bandgap
EM	Electro Magnetic
FOM	Figure of merit
GHz	Giga Hertz
GP	Geometric Programming
HF	High Frequency
HFSS	High Frequency Structural Simulator
IC	Integrated Circuit
IDC	Inter Digital Capacitor
IPD	Integrated Passive Device
LNA	Low Noise Amplifier
MEMS	Micro Electro Mechanical Systems
MHz	Mega Hertz
MIM	Metal Insulator Metal
MIMO	Multiple Input Multiple Output
MOM	Metal Oxide Metal
NF	Noise Figure

OCA	On-chip Area
OCI	On-chip Inductor
Q	Quality Factor
QOS	Quality of Service
PCB	Printed Circuit Board
PBG	Photonic Band Gap
PGS	Patterned Ground Shield
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFFE	Radio Frequency Front End
S- Parameters	Scattering Parameters
SiP	System in Package
SoC	System on-chip
SDSSI	Symmetrical Trace Differential Stacked Spiral In
SEI	Silicon Embedded Inductor
SRF	Self-Resonant Frequency
TSMC	Taiwan Semiconductor Manufacturing Company
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
VLSI	Very Large-Scale Integrated Circuit
VNA	Vector Network Analyser
WLAN	Wireless Local Area Network
Y- Parameters	Admittance Parameters

List of Symbols

C	Capacitance
L	Inductance
fF	Fempto Farads
μm	Micro Meter
mm	Milli Meter
nH	Nano Henry
pF	Pico Farad
Q	Quality Factor
M	Mutual Inductance
M_+	Positive Mutual Inductance
M_-	Negative Mutual Inductance
ε	Epsilon
η	Eta
ω	Angular Frequency
Ω	Ohms
ρ	Resistivity

Chapter 1

Introduction

1.1 Overview

Today's information centric world is witnessing a massive 5G proliferation, with an explosion of 5G devices in multitude of ultra-speed low latency 5G applications. Smart 5G wireless standards need heavily miniaturized high-performance RF front end (RFFE) circuit components to reduce die size. In literature, successful RFFE circuits prominently used the low-cost high performance Complimentary Metal-Oxide Semiconductor (CMOS) process [1], [2]. Existing 4G LTE smartphones support 30 frequency bands, require over 60 filters that occupy more than 50% of RFIC chip space. For example, in an Ericson cell phone board, the active to passive component ratio is 1:21. Typically a cell phone RF front end has 85% of the passive component count occupying 70% of board area with 60% of board cost [3].

CMOS RFICs are regularly scaling down to reduce the chip sizes following the Moore's law. Unlike the active components, it is very difficult to scale down the passive components so faster due to the precise resistance, capacitance and impedance values required [4]. Thus a huge demand arose to shrink the size of on-chip passive inductors and capacitors with low loss and small size, to realize miniature high performance RFICs for the 5G devices. The integrated passive device (IPD) technology is successful to realize small size high quality on-chip passives in silicon substrate. Recent past witnessed the growth of IPD BPF and LNA circuits as single CMOS chips in a system in package (SIP), suitable for 5G radio access applications [5]. Thus, miniature LNAs and BPFs for different 5G frequency bands are being heavily researched now.

Spiral inductors and capacitors became most prominent Si IPD passive components. The CMOS active inductors possess high inductance but are noisy. Bond wire inductors have

large parasitic capacitances. Planar inductors are easy to fabricate, but suffer large chip area. Fractal inductors offer higher performance but complex to design and expensive to fabricate. IPD technology supports multi-layer vertically stacked inductors and capacitors to realize space efficient RF System on the Chip (SOC) architectures. The multilayer IPD spiral inductors are the best choice to heavily reduce on-chip area of passives and thus the die size [6]. Therefore, the design and development of multilayer on-chip spiral passives are concentrated in this dissertation.

A novel double-split series stacked multilayer inductor is proposed and developed with superior performance, against the square spiral and variable width inductors. The on-chip inductor's performance is determined based on quality factor (Q), self-resonance frequency (f_{SRF}), inductance (L), and on-chip area. Passive capacitors with high performance are also developed, with reductions in chip space. These miniature IPD on-chip passives with enhanced performance are employed to implement LNAs and BPFs for 5G and UWB applications, which also exhibited very good performances [7], [8]. Fabricated passive components and RF circuits demonstrated excellent performance equivalence.

1.2 5G Communication

Telecom technology had undergone spectacular global developments to support the ever-increasing user demands for high quality ultra-speed services. The dominant mobile industry witnessed rapid evolution from 1G to present ultra-fast 5G wireless technology. 2G networks started the digital voice communication era. 3G mobile networks provided the Internet over mobile devices and laptops enabling voice and video calling, file transfer, internet browsing, etc. The 4G technologies: Long-Term Evolution (LTE) and WiMAX provided 100 Mbps speeds for high-mobility communication (in trains and cars). The innovative ultra dense 5G network technologies ratified by ITU-R and 5GPPP are globally deployed since 2020. 5G use cases include: eMobile Broadband (eMBB), massive machine to machine communications (MMC) and accurate location and navigation [9]. 5G wireless communication is expected to satisfy "**anytime, anywhere, any one, any device, any service**" concept to meet local, regional and global smart ubiquitous real time wireless connectivity.

High-speed 5G WLAN standards like IEEE 802.11a (UNII) WLAN/ ETSI HIPERLAN2 (5.15-5.825 GHz); RFID (4.9-5.8GHz); ISM (5.2-5.35 GHz); WiMAX IEEE 802.16 (4.5 – 5.97 GHz) support 1 Gbps data rates for Massive MIMO and IOT, at reduced latency [10]. 5G proposals recommended three 5G bands: RF 3 - 6 GHz (Low 5G), microwave

25 - 30 GHz (Mid 5G) and milli meter wave 50 - 80 GHz (High 5G). 5G mobile wideband (5G WB) is also earmarked with 8-10 GHz spectrum to enable ultra-accuracy location services and navigation applications. 5G systems not only exploit the traditional low 5G band below 6 GHz, but also the cm-wave (6 to 30 GHz) band [11]. Around 2.5 GHz of cm-wave spectrum is available from 6 to 28 GHz, 4 GHz at 38 GHz, 10 GHz between 70 GHz and 86 GHz and around 3 GHz at 90 GHz. The academia and industry also focus on future 5G application scenarios in frequency bands above 6 GHz, by finalising Mobile Wireless Communication Enablers for the 2020 Information Society (METIS –II) project.

1.2.1 5G Wireless Radio Transceiver

The important building blocks of a typical 5G wireless radio transceiver are shown in Fig. 1.1. Performance deciding blocks include: LNA, BPF, VCO, PLL and impedance matching networks. Present generation 5G receiver architectures include PAs and LNAs also inside the RFFE module. Mixer is considered as an IF section circuit. High Q on-chip passives are highly essential to meet the stringent responses for the successful 5G quality of service (QOS). More recently, Indian mobile operators started 5G network services in all telecom circles to the benefit of mobile subscribers.

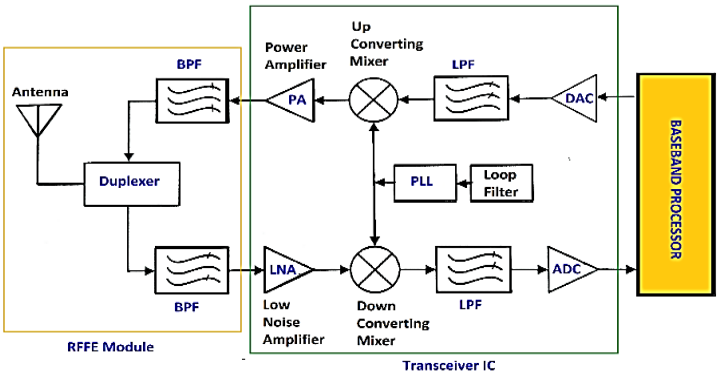


Figure 1.1 Generic 5G Transceiver with the Key Building Blocks

1.2.2 Low Noise Amplifier (LNA)

Being the first gain boosting component, the LNA is the direct influencer of overall noise performance of any receiver. Thus, it acts as a major performance decider for any RF front end electronics (RFFE). LNA must have a good input impedance match and small power consumption, which is a critical factor in portable mobile communications [12].

LNA design is quite complex, owing to the challenges involved in achieving low Noise Figure (NF), higher gain, lower power consumption, good input matching, and better linearity.

Hence, researchers employed design trade-offs between the performance's metrics. Optimal system on-chip (SOC) 5G LNA designs, primarily focus on minimal chip area via happy integration of low-cost CMOS process and high quality IPD passives. It is still a big design challenge to simultaneously optimize the desired parameters like minimum on-chip area (OCA), small losses, input and output matching, smaller NF, and higher gain, high linearity, unconditional stability.

Common-gate (CG) topology LNA produces better reverse isolation, good linearity, and large bandwidth but had very low gain and high NF [13]. A resistive feedback topology LNA produced good input matching, high gain, and better linearity, but suffered performance decrease at high frequency. Cascode LNA with inductive source degeneration is better topology to implement a narrow band LNA, with low power, good input matching, and low NF. A compact low NF 5 GHz LNA using constant width, variable width and double-split multilayer IPD inductors is designed and implemented in ADS. The novel double-split multilayer IPD inductor LNA has improved the S11, S21, NF and Stability of 64%, 75%, 74%, and 129% respectively, over CMOS Inductor [14].

1.2.3 Bandpass Filter (BPF)

Bandpass filters are direct deciders for the selectivity (tuning) and interference rejection of any radio receiver, in the receiver signal processing as depicted in Fig. 1.1. The RF BPF and IF BPF heavily influence the passing through of desired baseband and simultaneously rejecting the undesired in-band/adjacent-band interferences for high fidelity signal recovery. Primarily these filters in the receiving side shall be designed carefully as they must process the weakest signals corrupted by noise [15].

Efficient 5G wireless transceivers require integrated on-chip BPFs and LNAs. A multiband 5G smartphone like iPhone uses more than 50 on board filters for voice, video, internet, navigation, Bluetooth and Wi-Fi services. LTCC BPFs suffer heat and size problems [16]. MEMS based on-chip BPFs offer good performance but suffer from power constraints. Stub-loaded resonator BPFs easily support multiband response but the stub lengths are large [18]. Passive Silicon spiral devices are prominent due to smaller power loss, by using thick Silicon substrate layer and thin oxide layer. Obtaining minimum on the chip area (OCA), minimum insertion loss and maximum selectivity are still big challenges to design the passive BPFs [17], [18].

Many passive LC resonator BPFs using Si IPD CMOS technology were proposed in recent past to suit 5G wireless applications [19], [20]. Inexpensive lumped LC resonant filters became successful for RF applications [21]. The values of inductance, capacitance and the quality factor of passives, majorly influence the design of LC circuit as an RF BPF. Compact High Performance BPF using the proposed multilayer IPD inductor and planar capacitor is designed and implemented for UWB and 5G Communications at 8.2 GHz and 25 GHz respectively.

1.3 CMOS and IPD Technology

CMOS is a popular IC design and fabrication technology for microelectronics applications. CMOS ICs house billions of transistors (MOSFETs) integrated into a single chip or die. Standard CMOS technology employs either NMOS or PMOS to allow large scale integration of logic gates on VLSI IC. RF CMOS integrates the analog and digital electronic circuits co-located on a mixed-signal CMOS RFIC.

Tremendous growth of the mobile industry by 21st century was largely possible, with large scale use of digital signal processing (DSP) in wireless communications, propelled by the development of low-cost VLSI RF CMOS technology. It enabled sophisticated "anytime, anywhere" mobile communications revolution with small, low-cost, low-power mobile devices. CMOS RFICs with deep submicron MOSFETs operating up to 100 GHz frequency were commercially developed recently. Fig.1.2 shows the RF CMOS chips embedded onto miniature on-chip IPD passives, used in variety of wireless applications [22]. Maxim Integrated Products, Inc. has developed a fully integrated WLAN RF front end SOC with on-chip passive count of only 4 resistors, 4 inductors and 33 capacitors.

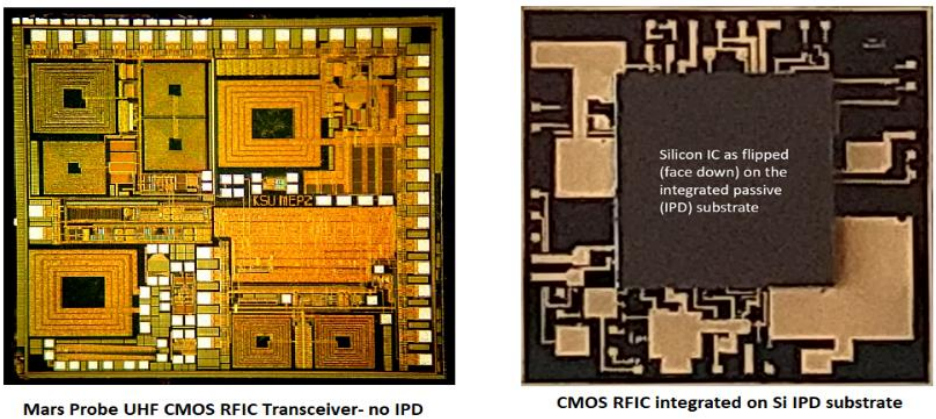


Figure1.2 Mars probe UHF CMOS RFIC transceiver without IPD and a CMOS RFIC integrated on a Si IPD substrate (courtesy: Kansas state university and Wikipedia)

IPD process is popular choice to integrate the key building blocks of CMOS RFICs like LNA, BPF, VCO and Power amplifiers, on the same silicon substrate [1]. IPD technology permits the simultaneous low cost, compact size and excellent performance for all 5G radio front end electronic circuits realized in a single chip die [23]. Many UWB filters are being realized in a Si IPD platform which offers high level of integration compared to many microwave substrates [24]. This research work also focused to design and develop IPD passive inductors and capacitor to successfully implement LNA and BPF circuits for 5G applications, exhibiting very good performance.

1.4 On-chip passives

On-chip passives devices are inductors and capacitors realized on the CMOS silicon wafers. Passive components are a must to use in the high frequency (HF) RFICs, as the inductive loads help to obtain higher center frequencies. Placing the high-quality RF passive components onto the silicon RF CMOS wafers is a big challenge for RF researchers. The large sized RF passive inductors and MIM capacitors are major problems in reducing the area of high quality 5G RFIC transceivers [25]. Specialized EDA tools help to develop on-chip passive components permitting a single silicon chip circuits and package interconnects. High Q on-chip passives easily provide interstage impedance matching to minimize the power consumption.

Overall die size gets reduced because many numbers of passive elements are embedded on the same die. High resistivity silicon (HRS) substrates, help to improve the quality factor of passive elements, by lowering eddy current losses in Si substrate [26]. Losses associated with CMOS are generally classified into two: metal losses and substrate losses. Metal losses enforce limits on Q factor of inductor at lower frequencies, while substrate losses impose limits on the Q factor at higher frequencies. The classical spiral structures are realized with vertically stacked multilayer geometry to avoid substrate induced losses. More recently, the popular IPD technology enabled the chip space reduction and successfully integrated the passive components with CMOS circuits on same silicon substrate.

1.4.1 On-chip inductors

Today's smart mobile devices necessitate large scale integration of multiple applications like phone, e-mail, camera, web browsing, GPS, multitude of Apps, etc. Such demands impose a daunting task for high performance RFIC designers to integrate the digital, analog, and RF circuits on a single wafer. The biggest hurdle is the passive component

integration onto the RFIC, transformed the design and development techniques in past few years.

On-chip inductor (OCI) is the most influential passive element doing performance enhancement and also size reduction for a CMOS RFIC [27]. The performance metrics of the on-chip inductors are: ascertained based on- quality factor (Q), self-resonance frequency (f_{SRF}), inductance (L), and on-chip area. Several geometry parameters, process parameters and fabrication process influence the final electrical performance of the on-chip inductor [28]. The required inductance value decreases, as the RFIC operating frequency increases. Realizing such low inductance is very difficult for an off chip inductor (externally placed) [29]. Advanced CMOS and IPD technologies allow the fabrication of on-chip passive inductors to realize fully integrated mixed-signal SOC. Silicon Embedded Inductor (SEI) is created by inserting the conductor metal into a non-conductive silicon substrate, with through-Silicon-Via contacts.

Based on the design methodologies, the high frequency (> 1 GHz) on-chip RF inductors are categorized into: Active, Bond wire, differential, fractal and spiral inductors. Active inductors use Op-Amps and the gyrator-C methods. Active inductors support multi band operation with tunable inductance [30]. The active and gyrator inductors are shown in Fig.1.3.

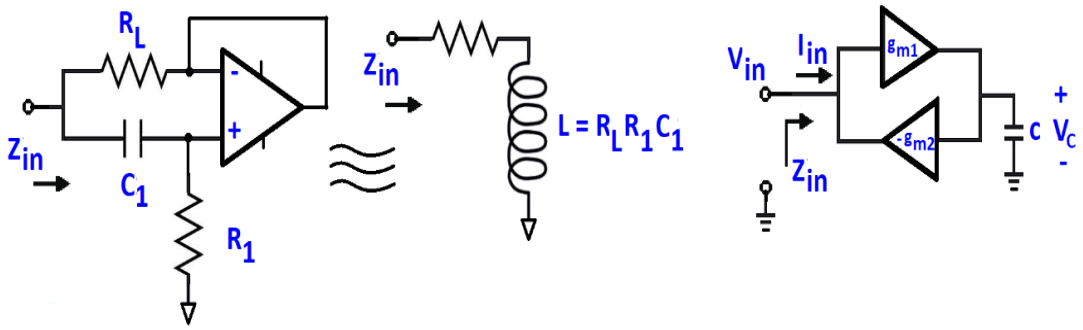


Figure 1.3 Op-Amp active inductor and a Gyrator active inductor (courtesy: https://wiki.analog.com/)

An inductor is realized by a simple cascade of resistors, an Op-Amp and a capacitor. Op-Amp represents high impedance, behaving like an inductor. The Op-Amp inductors exhibit smaller Q, due to the series resistor R_L [31]. This occupies larger on-chip space and has nonlinearity. Gyrator – C based active inductor connects two transconductors in feedback to realize an inductive impedance, by transforming its intrinsic capacitance. This inductor operates below 1 GHz. The effective impedance of gyrator inductor is given by Eq. 1.1.

$$L_{effective} = \frac{C}{g_{m1}g_{m2}} \quad (1.1)$$

Where gm is transconductance of two gain op-amps and C is the parallel capacitance. Active inductors suffer from smaller Q factors, poor noise performance and larger power consumptions due to parasitic capacitances [3].

Bond wires create electrical interconnections between semiconductors or ICs and silicon chips using bonding wires made of very thin gold and aluminium materials. Bond wire inductors were developed in 1990s for RFIC connection to a package as shown in Fig. 1.4.

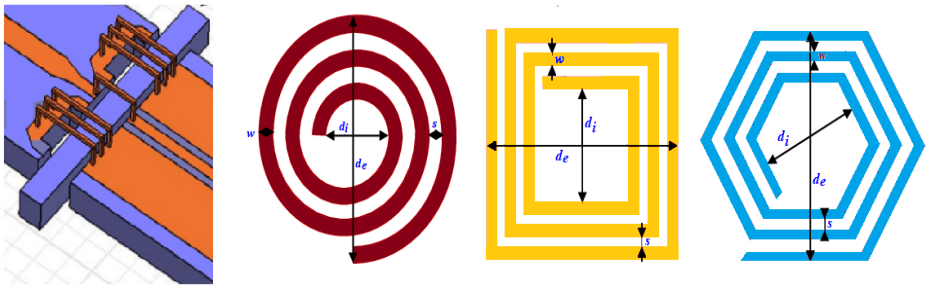


Figure 1.4 Bondwire, Circular Spiral, Square Spiral and Hexagonal Spiral Inductors (Courtesy: https://en.wikipedia.org/wiki)

Bond wire is modelled as a parasitic inductor in series with some resistance. Typically they possess nH inductances, mΩ resistances, gold wire diameters from 25 to 300 microns and 1-5 mm lengths. They exhibit higher Q (25-75) due to small resistances. Inductance associated with the bond wire depends on: wire metal, diameter, length, thickness, separation and height above the substrate. This inductor introduces significant parasitic capacitance, underpass resistance and possess crosstalk problem [32]. Hence their usage at 5G frequencies is limited.

Spiral inductor is an easy to generate popular model of all the on-chip inductors, as shown in Fig. 1.4. Planar spiral inductors in Si technologies are fabricated, using minimum of two metal layers. The top layer forms the inductor structure and the bottom layer brings the inner port to external connector, using the underpass (via). A popular implementation of monolithic inductors is the square spiral inductor. Initially such planar inductors were developed for variety of RF inductor applications. The figure of merit (FOM) for the on-chip spiral inductor are (i) Q factor (Q) (ii) optimal frequency, (f_{max}) where Q factor attains its maximum value, Q_{max} (iii) self-resonant frequency, f_{SRF}. The inductance and quality factor are frequency dependent properties.

Spiral inductor structure ensures the conductor turns having current flow in same direction are placed closely and conductor turns having current flow in opposite direction are

separated further apart. This increases the net positive mutual inductance and increases the total inductance value [33]. Such Planar inductors have shown smaller Q value, because of resistive loss and substrate losses, which occur due to skin depth of metal and eddy current losses at high frequencies. The substrate loss due to the magnetic field penetration represents the mutual inductance between substrate and metal layers. The metal and substrate pattern ground shielding (PGS) below the inductor was employed to reduce the substrate loss. PGS inclusion helped in enhancement of Q but resulted in SRF reduction [34]. The on-chip area of an RF planar inductors is high so as to achieve higher SRF and Q values.

Need for heavy miniaturization and performance enhancements of the on-chip inductors for 5G RFICs prompted the development of multilayer inductors. Modern CMOS RFIC fabrication techniques easily permit multiple metal layers vertically stacked and interconnected as a series cascade (series stacking), to increase the overall conductor length. Thus, a multilayer inductor produces much larger inductance value relative to planar inductor. Such multiple layers occupy the same on-chip area equal for planar inductor, but yields increased inductance and Q values. Hence multilayer inductors are highly miniaturized for given chip space constraint, suitable for 5G RFIC applications. Typical multilayer inductor structure is shown in Fig. 1.5 [35].

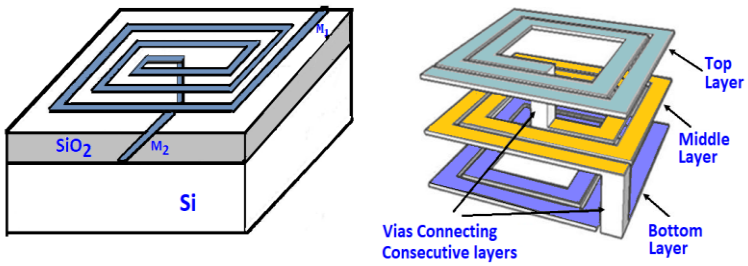


Figure 1.5 Multilayer (3 layer) Inductor and a 3D Inductor

A miniature 3D multilayer inductor was proposed and fabricated in one poly four (1P4M) 350 nm CMOS technology [36]. This structure with symmetrically placed output and input ports, is shown in Fig. 1.5. This 3D inductor is a series stacking of three spiral inductors placed in three different layers. It considerably reduces the overall on-chip are for a given increased inductance.

Spiral inductors can have geometries with symmetry or asymmetry. Two asymmetric spirals can be merged to form a standard symmetric differential inductor, having differential inputs. This can be easily integrated with any active component since both the ports are in the

same layer. Thus, differential inductors possess high Q factors, but occupy smaller chip spaces, in a typical RFIC. Differential inductors were limited by inductance values and track widths which increases the overall capacitance. Fig. 1.6 shows a typical fractal inductor based on Hilbert curve [32].

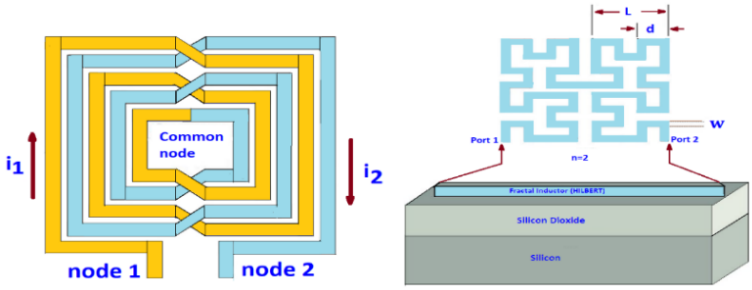


Figure 1.6 Differential Inductor and a Hilbert Fractal inductor on the chip

Recently multilayer differential inductors were developed with high performance and significant area reduction. Off late, the fractal inductors are developed with increased inductance value, but without footprint enlargement. Fractals are mathematical space filling curves that iteratively fill a bounded area. Fractal curves have wide variety of shapes and sizes to develop a geometrical structure to represent inductor and capacitor models. Fractal geometry is successfully adopted by RFIC designers for wireless applications. Fractal methods can also help miniaturization of the IPD passives for RFIC and MMIC applications. Fractal capacitors also possess higher capacitance in a single layer structure [32]. Fractal inductors have design complexity and also fabrication expenses.

1.4.2 On-chip capacitors

The chip capacitors are the capacitors fabricated as IC devices, to protect RFICs from noise problems. IC capacitors are placed on the package substrates, or embedded in the die. Their capacitance is defined by the geometry and the dielectric constant of semiconductor. On-chip capacitor is a vital reactive component employed in impedance matching network, VCOs, tuned resonators and BPF circuits [37]. 5G RFICs need miniature on-chip capacitors to minimize the die sizes. The performance parameters of an RF capacitor are: capacitance per unit area, break down voltage, quality factor and linearity. S-parameters from an EM simulator or a vector network Analyser (VNA) are utilized to determine the capacitance and Q values at high frequencies.

Metal-oxide-semiconductor (MOS) capacitors employ MOS transistor as a capacitor, with a thin oxide insulator in the gate. It acts as a varactor, whose capacitance depends on the

applied DC voltage. But, the capacitance value gets changed due to depletion effects or the charge accumulation at the oxide layer interface. Hence, the stackable Metal-insulator-metal (MIM) electrode capacitors with a high k dielectric oxide layer insulator in between two parallel metal layers became popular [38]. MIM capacitor forms by enclosing the field between upper two metal layers only and thus possess insensitivity to the substrate effects. On-chip area of an MIM capacitor increases due to its incapability to scale down along with process technology scalings. Interdigital capacitors (metal fringe) employ interdigital structure that exploits the fringing fields to produce higher capacitance [39]. But they suffer heavily from parasitic effects. Fig. 1.7 shows the generic structure for above inductors.

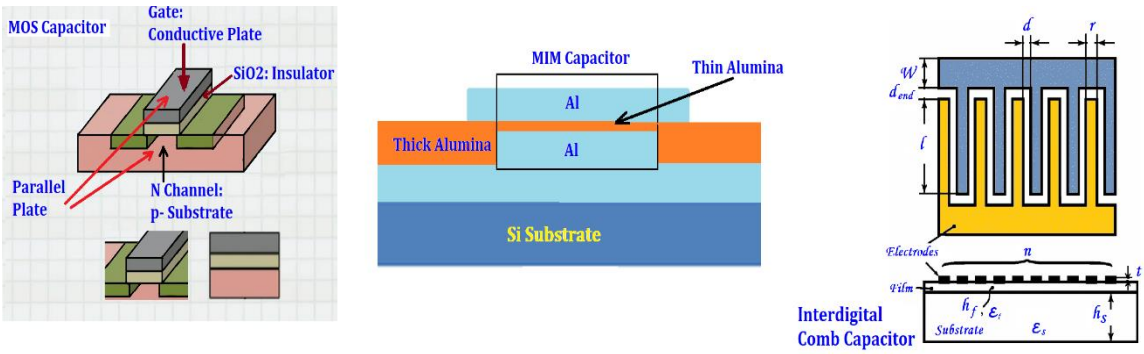


Figure 1.7 Generic structure of MOS, MIM and interdigital capacitors

Single or multilayer fractal capacitors are easily designed and simulated in HFSS, by setting the process parameters of metal, dielectric and substrate layers as per CMOS technology [40]. Selecting orthogonal metal traces help to reduce the series resistance and inductances and. Fractal geometry helped to increase capacitance by more than 10%, Q value by 50% and the SRF by 20% over standard spiral capacitor [41]. However, the fractal capacitors suffer from design complexity and fabrication costs. Fig. 1.8 depicts the structures for these on-chip capacitors suitable for RFIC applications [42]. RF IPD process employs a high resistivity substrate for 3D passive integration of high quality passive components like capacitors and inductors.

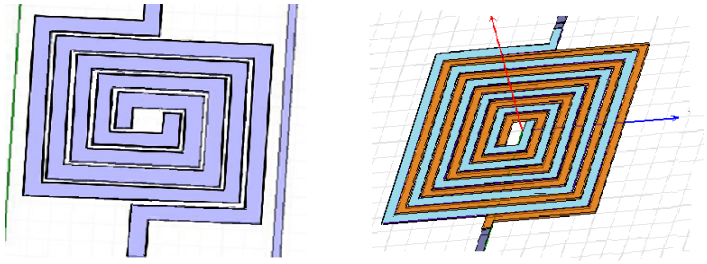


Figure 1.8 Generic structure of the spiral and fractal capacitors

Exploiting the advantages of multilayer spirals, recently multilayer fractal capacitors were proposed at 5G frequency bands [43]. They exhibited enhanced capacitance density for same chip area. It was found that the layer spacing has influence over the value of capacitance.

1.5 On-chip passive component design

Decades of dedicated research works on Si RF CMOS ICs produced low-cost RF on-chip passive devices with improved performances. RFIC researchers are optimizing these compact, low loss and high quality on-chip passives to extend the capabilities of scalable CMOS RFIC designs for 5G applications. Single-layer and multilayer inductors capacitors are providing good performance through 40 GHz. They are used in internal and external configurations in RFICs. Planar capacitors act as excellent impedance matching networks, when placed inside or outside a CMOS RFIC.

1.5.1 IPD Inductors

The best reported value of Q factor for on-chip CMOS inductors lie in a range of 10 to 20, depending on the technology [44]. Past designs of an on-chip inductor had accuracy below 10% [45]. IPD inductors utilizing the flip chip package are developed to overcome the substrate loss for an on-chip CMOS inductor.

Multi-chip module (MCM) packaging is developed to fabricate a CMOS chip with active devices and an IPD chip with on-chip passive device. Then these CMOS and IPD chips are interconnected using a micro bump bonding, for area efficient low-cost SiP technology. The IPD technology supporting high quality on-chip passive inductors, compatible with CMOS IC process, is a proven technology for 5G RF applications. SiP solutions employ a modular architecture which integrates the mixed ICs and passive devices like the resistors, inductors, capacitors, filters, balun, transceivers directly onto a Si substrate for a cost effective system solution. Silicon IPDs reported size reduction by 50% compared to LTCC [46]. This research work has successfully produced IPD-inductor based LNAs, with lower NF, higher gain and minimum losses than the on-chip-CMOS inductor based LNA. Many foundry services include a fully characterized standard IPD library solutions to support customized IPD designs. Fig. 1.9 depicts a NASA eWLB chip scale module with a CMOS amplifier chip (on the right) and an IPD filtering chip (on the left), interconnected by embedded wafer level ball array (eWLB) package technology. It also shows a typical single chip LNA realized by a happy integration of CMOS circuit and IPD passives.

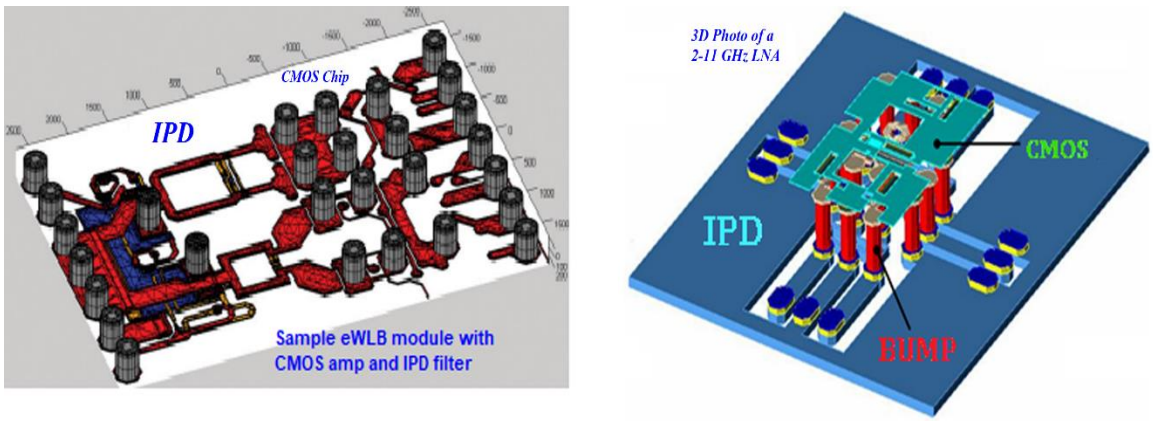


Figure 1.9 Standard SiP applications with co-located CMOS chip and an IPD chip (Courtesy: *https://www.jcetglobal.com/*)

1.5.2 Design parameters and their classification

The parameters such as signal fidelity, noise, distortion, and interference represent the performance of RF circuits. Lumped components (wires, resistors, capacitors, inductors, connectors etc.) behave differently at low and high frequencies. Skin effect restricts the current conduction close to the periphery with reduced current density at the center. The state of art on-chip passives used in the 5G RFICs are mostly based on the basic spiral structures and hence considered in this dissertation work carried. Inductors are geometrically larger than integrated capacitors and resistors.

On-chip passive components like resistors, inductors, and capacitors are modelled and designed using many control parameters, which are broadly categorized into: Lateral (design control) and Process (process control) parameters [3]. These parameters are influential in deciding the RF characteristics any passive device. Lateral parameters mostly include the structural or geometrical dimensions of passive components. Process control parameters (vertical) are technology parameters, material properties of the substrate, oxide and the metal. The on-chip passive design controlled parameters include:

- Metal width, w
- Turn Spacing, s
- Turn (side) length, 1
- Number of turns, N
- Number of metal layers
- Outer and inner diameters, D_{out} and D_{in}
- Fill Ratio

The Process-controlled parameters known as 'vertical' parameters, include:

- Shape of spiral (circle, square, hexagonal)
- Metal resistivity.
- Substrate resistivity.
- Metal thickness.
- Oxide thickness.

These parameters will define the inductance, capacitance, quality factor, SRF and other Parasitics of the on-chip passive components, such as:

- Series resistance, Rs,
- Spiral capacitance, C
- Substrate capacitance, Cs
- Substrate resistance, R_{sub}
- Spiral capacitance, C
- Spiral Inductance, L
- Self-Resonant Frequency (f_{SRF})
- On-chip Area (OCA)

Design parameters of RF resistors include: Material resistivity, power rating, frequency range, Resistance, package type, parasitic capacitance and footprint. Flanged RF thin film resistors offer 10 to 1000 Ω resistance, 1000 W power rating, operating frequency up to 18 GHz and a size of 26.42 x 48.26 x 6.22 mm. The Resistance is expressed by Eq. 1.2.

$$\boldsymbol{R = V/I} \qquad \boldsymbol{R = \frac{\rho l}{A}} \tag{1.2}$$

where l is length, A is the area and ρ is resistivity. High frequency behaviour of an on-chip resistor including parasitic effects [34] is shown in Fig. 1.10.

RF inductors impede current variation, with impedance increasing with frequency, and magnetic field stores energy to preserve the circuit current. The basic equation to calculate the impedance of an inductor at different frequencies is

$$\boldsymbol{Z = j\omega L} \tag{1.3}$$

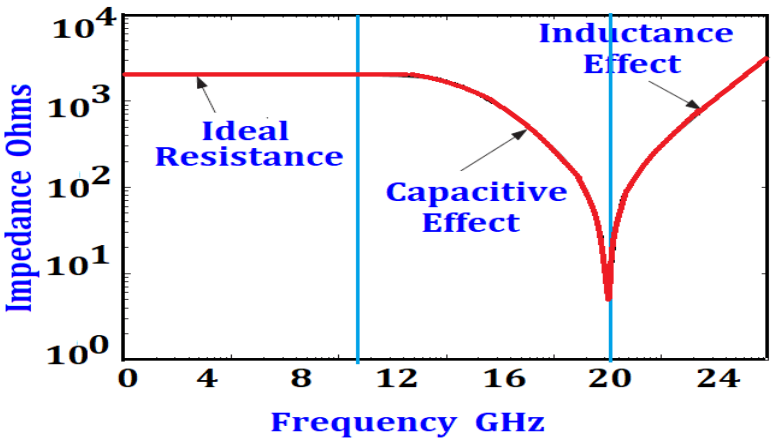


Figure 1.10 Performance regions for an RF on-chip resistor (Courtesy: https://www.edn.com)

The on-chip spiral layouts are analysed by considering the lumped series RL and shunt RC π-model. The RF on-chip inductor used in floating configuration is a two port network without grounding any port. Its shunt configuration connects one port to the circuit and second port to ground. A two-port inductor model is employed in this work, since the shunt inductor model is derived from a floating model by grounding one port. The on-chip spiral inductor layout and its equivalent π-network model [34] are shown in Figure 1.11.

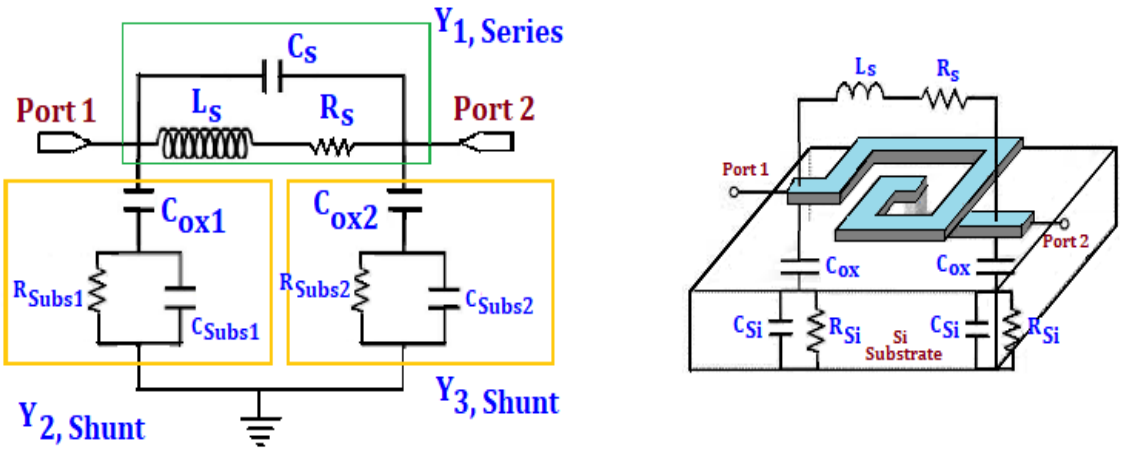


Fig. 1.11 3D view for spiral inductor and its Physical π- equivalent model on Silicon

This π- model comprises of a series inductance with a resistance, and a shunt capacitance in series with a resistance as shown above. The performance metrics such as the Q factor, inductance, and self-resonance frequency are shown. Also shown are the lateral parameters, substrate and oxide capacitances (C_{si}, C_{ox}), substrate resistance (Rsi) and spiral capacitance, inductance and resistances (C_s, L_s and R_s). These substrate capacitances and resistances would model the resistive loss and capacitive losses, which vary with frequency.

The mutual coupling between inductor segments produce different values of mutual inductances (positive and negative), parasitic resistances and capacitances [17].

On-chip inductors are designed mostly using EM simulators like HFSS, ADS and Sonnet etc., for ease of modelling and design verification. They are used to design and simulate the inductors up to SRF and generate two-port S-parameters. The Y-parameters are obtained from the simulated S-parameters. The inductance values, series resistance and spiral capacitance values for equivalent circuit π-model for the inductor are calculated from the derived Y-parameters. Metal resistance (R_s) and the inductance (L_s) are found [47] from Eq. 1.4. The Capacitance between conductor segments is expressed in Eq. 1.5.

$$\boldsymbol{R_s = Re\{-\frac{1}{Y_{21}}\}} \qquad \boldsymbol{R_{DC} = Re\{\frac{1}{Y_{12}}\}} \tag{1.4}$$

$$\boldsymbol{C_s = \frac{L_s}{R_s^2+(\omega_c L_s)^2}} \qquad \boldsymbol{L_s = \frac{Total\ Flux,\varphi}{current,I} = \frac{1}{\omega} Im\{\frac{1}{Y_{11}}\}} \tag{1.5}$$

Q factor for spiral inductor is defined as the ratio of total time average of stored magnetic energy (Wm) and the time average of electrical energy (We) as given by Eq.1.6.

$$Q\ Factor = \frac{Stored\ Energy}{Dissipated\ Energy} = \frac{\omega(W_m - W_e)}{P_L} \tag{1.6}$$

where P_L is power loss. The Q factor and oxide capacitance are also defined using Y parameters as given by Eq.1.7.

$$Q = \frac{-Im[Y_{11}]}{Re[Y_{11}]} \qquad C_{oxide} = \frac{Im[Y_{11}+Y_{12}]}{\omega} \tag{1.7}$$

The performance of a Si spiral inductor is judged by plotting its quality factor and its inductance L [48], as shown in Fig. 1.12. The frequency where the Q factor value becomes zero, is the self-resonance frequency (f_{SRF}) of the inductor. After SRF, the inductor behaves as if it is a capacitor.

On-chip Capacitor is a vital passive component in wireless RFIC applications. They are prominent performance influencers of Wireless transceiver building blocks like VCOs, Filters, LNAs, Mixers and impedance matching network etc. Miniature on-chip capacitors are most sought in 5G CMOS RFICs to minimize the die sizes [49]. The design of low leakage and high-quality capacitors is a big challenge for RF researchers. At radio frequencies, the

scattering or S-parameters represent the capacitor behaviour, like that of an on-chip inductor. The capacitance and quality factor values are determined from the S-parameters obtained from the EM simulator or a vector network Analyser (VNA). Then Y- parameters are calculated from these S-parameters. The basic capacitance value and the Q factor value are calculated using Eq. 1.8 and Eq. 1.9.

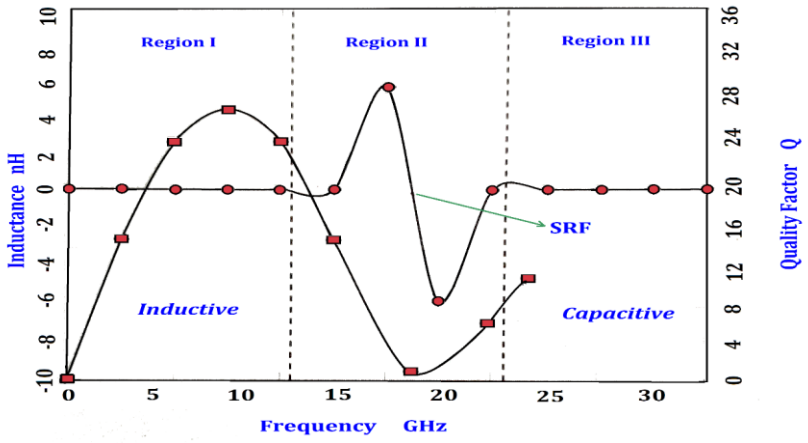


Figure 1.12 Performance regions for an on-chip inductor in Silicon

$$Capacitance = \frac{-Im[Y_{21}]}{\omega} \qquad C = \frac{\varepsilon A}{d} = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{1.8}$$

$$Q\ Factor = \frac{-X}{R} = \frac{Im[Y_{11}]}{Re[Y_{11}]} \tag{1.9}$$

The performance of a Si spiral capacitor is judged by plotting its quality factor and its capacitance C w.r.t. frequency [48], as shown in Fig. 1.13. The self-resonance frequency (f_{SRF}) of the capacitor is the frequency at which, its Q=0. After SRF, the capacitor behaves as if it is an inductor.

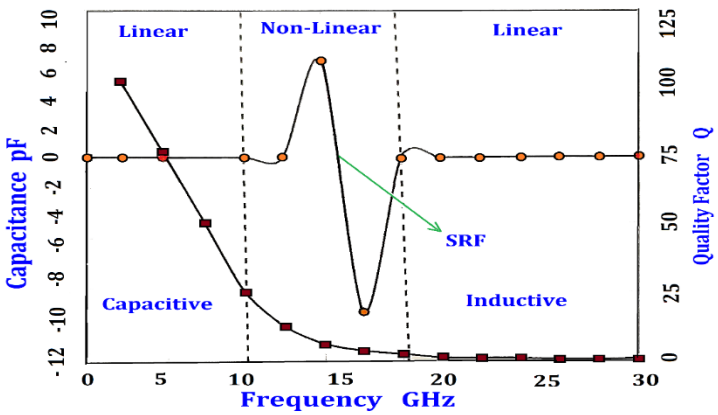


Figure 1. 13 Performance regions for an on-chip spiral capacitor

1.5.3 Parasitics and losses associated with on-chip spiral passives

A parasitic element in both analog and digital CMOS RF circuits is an undesired and unavoidable circuit element (resistance, inductance or capacitance), possessed by an on-chip passive component. The most commonly seen parasitic elements are the parasitic resistance and inductance of the leads and the parasitic capacitance of the packaging. RF passive designers strive hard to minimise parasitic elements but are unable to eliminate them. Lumped component models popularly represent the parasitic elements in equivalent circuits. Parasitic resistance reduces the fill factor and affects the series and shunt resistance. Parasitic inductance is an undesired inductive effect which is unavoidable in all the electronic devices. Parasitic capacitance is unwanted capacitance existing between two or more parts of an electronic component which are in close proximity to each other.

The Q factor of an on-chip inductor is expressed as the ratio of magnetic energy and electrical energy, is given as,

$$Q = 2\pi \left(\frac{Peak\ Magnetic\ Energy - Peak\ Electrical\ Energy}{Energy\ Loss\ per\ Cycle} \right) \tag{1.10}$$

Q value of the on-chip silicon substrate spiral inductor derived from its physical model shown in Fig. 1.11, is given as,

$$Q = \underbrace{\frac{\omega L_s}{R_s}}_{Ohmic\ Loss} \cdot \underbrace{\frac{1}{1+\frac{R_s}{R_p}\left\{\left(\frac{\omega L_s}{R_s}\right)^2+1\right\}}}_{Substrate\ LOss} \cdot \underbrace{\left[1 - \frac{R_s^2(C_s+C_p)}{L_s} - \omega^2 L_s(C_s+C_p)\right]}_{Self\ Resonance\ Factor} \tag{1.11}$$

$$R_p = \frac{1}{\omega^2 C_{oxide} R_{Silicon}} + \frac{R_{Silicon}(C_{oxide}+C_{Silicon})^2}{C_{oxide}^2} \tag{1.12}$$

$$C_p = C_{oxide} \frac{1+\omega^2(C_{oxide}+C_{Silicon})C_{Silicon}R_{silicon}^2}{1+\omega^2(C_{oxide}+C_{Silicon})^2 R_{silicon}^2} \tag{1.13}$$

$$f_{SRF} = \frac{1}{2\pi\sqrt{LC_{eq}}} \tag{1.14}$$

Here, ω is the angular frequency, R_s is the inductor series resistance, L is overall inductance, C_{oxide} is the oxide capacitance, C_s is capacitance existing between conductor turns, $C_{Silicon}$ is capacitance of substrate, $R_{Silicon}$ is the resistance of substrate. C_p and R_p are total parasitic capacitance and resistances, caused by the parasitics C_{oxide} , $C_{Silicon}$ and $R_{Silicon}$. In low frequency region the inductor's Q value depends on series Resistance found from the first term

($\omega L/R_s$) from Eq. 1.11. The substrate loss is found from second term in Eq. 1.11. Thus, Q value reduces (>5GHz), mainly due to combined influence of self-resonance and the substrate losses. The penetrated displacement current from metal to the substrate produces the substrate loss. This is modelled as an RC network comprising the C_{Oxide}, $C_{Silicon}$ and $R_{Silicon}$. Typically, the Q factor gets reduced by 10-30% due to silicon substrate losses.

The net inductance of on-chip spiral inducer is affected at gigahertz frequencies due to the metal-to-substrate mutual inductance, magnetically induced eddy currents. Such eddy currents flow in opposite directions to currents in a spiral, so that the negative mutual inductance increases. This leads to inductance reduction as well as the Q value [50]. In GHz range, the current crowding effects reduce the skin depth forcing an increase in series resistance. Such increase in Rs, decrease Q value correspondingly.

RF performance of spiral inductor gets degraded due to the ohmic loss, substrate loss and current crowding. Substrate losses are caused by penetration of Electric and Magnetic fields into the substrate. The ohmic (metal) losses are due to non-uniform current flow within the metal caused by the skin effect and proximity effects. Proximity effect produces eddy current loss, when magnetic field from adjacent metal lines penetrate the metal traces. Patterned ground shield (PGS) method reduces substrate loss and increase the Q value, but SRF decreases. Multilayer inductors increased the total inductance, SRF and Q values having same chip space [51].

1.5.4 Tools Employed

In general, on chip passives are modelled, designed and simulated to verify their performance using many EM simulation software packages like, HFSS, ADS, SONNET, etc. HFSS is developed based on the numerical technique, Finite Element method (FEM). In HFSS, the entire structure of a passive is subdivided into smaller subsections as the finite elements called as mesh. Maxwell's equations are solved by applying the boundary conditions, to generate the scattering matrix. It is proven that the final results obtained are accurate enough to exhibit the desired RF performance. The solution flow in HFSS consists of the steps:

- Apply mesh to entire structure
- Calculate the EM fields inside structure for excitation frequency
- Percent error calculation
- If found unsatisfactory, redefine the mesh and compute error afresh

- Rerun till for adaptive process convergence for converged error
- HFSS solves for entire frequency sweep without mesh re-definition.

The EM simulators used for most of the works done in this thesis include: HFSS, ADS Momentum and Sonnet. The performance verification for the fabricated on-chip passive inductors, capacitor, BPFs were done by measurements conducted using a Vector Network Analyser (VNA). Circuit simulations for LNA and BPF were performed in HFSS and ADS.

The desired component variables are extracted from the previously given expressions in terms of Y- parameters and S-parameters. HFSS generates waveform plots also for easy visual observation. Proposed component variables are extracted in touchstone format to validate the simulation results relative that of other tools. Advanced Design System (ADS) from Agilent technologies is a popular electronic design automation (EDA) tool for EM simulation of RF, microwave and CMOS ICs. It has many wireless system libraries and circuit level co-simulation features. It provides RF solutions with unified schematics, layouts and 3D EM full wave results for ICs and component designs. Touchstone HFSS file is exported easily into S- parameter definition of ADS. Hence, the results from both HFSS and ADS can be correlated to validate the proposed models of on-chip passives and corresponding LNA and BPF circuits. Sonnet software is used for layout generation and component simulations.

1.6 Motivation

Diminishing sizes for CMOS RFICs due to technology scaling and the recent IPD technology are fast converging to meet the demand for highly miniaturized RFICs for 5G applications. High frequency (≥1GHz) on chip passive inductors and capacitors are being realized with High Q and higher SRFs, but they still occupy large on chip area. The IPD technology employs minimum area multilayer geometry to produce the miniature on chip passives (L and C). IPD technology permits easier integration (stacking) of small size on chip passives along with low-cost CMOS components, to realize size reduced RFICs. Highly miniaturized on-chip passives heavily reduce the occupied chip space and lead to size and cost reductions for 5G devices and terminals. Happy integration of CMOS and the IPD technologies, is core theme behind the design and development of efficient 5G RF LNAs and BPFs in the current research for low-cost miniaturized 5G RFICs and systems. Hence the on-chip area reduction plus simultaneous performance enhancement is the main goal behind this research work towards miniaturization of 5G building blocks.

1.7 Problem Statement

To design and develop, miniature high quality on-chip series stacked multilayer IPD Inductors to implement the high performance BPFs and LNAs for UWB and 5G Applications.

1.8 Research Objectives

- *Design of Series Stacked On Chip Multilayer (ML) Spiral Inductors Using the IPD Technology for 5G Communications.*
- *Design and Implementation of Novel Series Stacked Double-split multilayer Spiral Inductors for 5G Frequencies.*
- *Fabrication of the Proposed Novel ML Inductors and Validating their Simulation Results with their Measurement Results.*
- *To Implement the Bandpass Filters and Low Noise Amplifiers employing the above Proposed Multilayer IPD Inductors and Capacitors for 5G Communications.*

1.9 Organization of the Work

The thesis presents the design, simulation, fabrication and the performance analysis of on-chip series stacked multilayer IPD spiral inductors to improve performance metrics of the IPD components for the equivalent on-chip area. It also reports the implementation of 5G CMOS LNAs at 5.0 GHz and 5.5 GHz using the proposed IPD inductors. It also reports the implementation of 5G BPFs at 8.2 GHz and 25 GHz using the proposed IPD inductors.

Chapter 1: *Presents an introduction to the research work, Motivation, and Problem statement.*

Chapter 2: *Reviews the notable amount of most updated literature and brief outline of the thesis is also presented*

Chapter 3: *Presents the design, simulation and implementation of multilayer series stacked inductors and a novel double-split spiral inductor*

Chapter 4: *Illustrates the design and simulation of LNAs using proposed Double-split inductors for 5G RFIC applications*

Chapter 5: *Presents the design and simulation of BPFs using the Proposed Double-split inductors for 5G RFIC applications*

Chapter 6: *Conclusions and Future Scope.*

Chapter 2

Literature Survey

2.1 Introduction

Spectacular technological advances and evolutionary research developments made the wireless network operators to deploy 5G communications globally much to the happiness of service quality demands across different use cases. Prominent circuit elements employed in the design of on-chip ICs are resistors, inductors and capacitors, apart from the active devices. On chip Passive components are indispensable beyond 1 GHz due to their noise and power advantages. Highly miniaturized on-chip IPD passive components are easily integrated today with low-cost CMOS RF circuits to produce small sized mobile devices using SiP technology. Especially, the on-chip inductors being larger in size compared to on-chip capacitor, play key role in deciding the performance of 5G RFIC building blocks like LNAs, BPFs and VCOs etc. Heavily researched on-chip IPD inductor structures had exhibited very good performance metrics with reduced chip spaces. This literature survey, reports and discusses, the structural and performance analysis of different on-chip inductors and capacitors researched so far. Also reported are the 5G applications of these on-chip passive components in the design and implementation of the LNAs and BPFs, till recently.

2.2 Review of On-chip Inductor Design

Researchers had identified the difficulty of integrating the on-chip inductors in practice, due to their large size and low Q factors at GHz frequencies. Literature on inductors cover from the standard planar spirals to series stacked multilayer structures. We proposed novel double split stacked multilayer inductor structure which not only exhibited very good performance but also possessed the minimum area occupied on chip, at different 5G

frequencies. On-chip silicon inductor is the most essential and performance deciding circuit component. Miniaturization of the silicon inductor has, therefore, become a major area of research, and significant work has already been done in this area. This section discusses several on-chip inductors reported so far with their merits and drawbacks.

2.2.1 Standard Planar On-chip Spiral Inductor

This section presents past works on planar on-chip spiral inductors with their salient merits and demerits.

In [52] E. Frlan et al., developed a lumped equivalent model for first time, to present the characteristics of a 0.065 mm^2 square spiral inductor. It was fabricated on an alumina substrate with inner dia of 160 μm. Its inductance value is 1.75 nH at an SRF of 20 GHz.

In [53] N.M. Nguyen et al., had fabricated two Si substrate square spiral inductors with an outer diameter of 230 μm and 115 μm, respectively. They had inductances of 9.3 nH and 1.3 NH with the corresponding SRFs of 9.7 and 2.47 GHZ. Both the inductors showed Q factor values from 3 to 8. An LC resonant low pass filter realized using them showed improved performance in terms of the linearity, gain and input matching.

In [54] J.YC. Chang et al., designed a spiral inductor of a large 100 nH inductance with an outer dia of 440 μm. The substrate losses got reduced along with an improved Q and SRF, by etching of the substrate underneath. The SRF also enhanced to 3 GHz from 800 MHz. A standard CMOS IC tuned amplifier using this inductor could achieve 14 dB gain at 770 MHz, 6 dB NF, and a 7-mW power dissipation for 3V supply.

In [34] C.P Yue et al., presented physical inductor model for a silicon substrate on-chip inductor. This model is based on substrate losses, copper losses and parasitic losses, to optimize the inductor performance. This modelling has paved way for developing many innovative on-chip inductor structures subsequently.

In [55] Min P Park et al., tested the fabricated standard CMOS inductor with three substrates having different resistivities. Using the high resistive substrate led to the substrate loss reduction along with quality factor enhancements. A detailed analysis showed the effect of several layout parameters like the metal thickness, metal width, spacing, inner diameter and the number of turns, on the Q value and inductance for all the three substrates.

In [56] J. Burgahartz et al., fabricated 10 μm width square spiral inductor with a spacing of 3.5 μm and an on-chip area of 160 x 160 μm. The inductor possessed 2.45 nH inductance, Qmax value of 9.7 at an SRF 5.3 GHz. An LNA, VCO and BPF were implemented utilizing high Q square spiral inductor. Insertion loss of the BPF got improved by more than 5 dB. LNA showed higher gain, low power consumption, and smaller NF. The VCO achieved power savings and phase noise improved by 7 dB.

In [34] C Patrick Yue and SS Wang, reported a GPS receiver circuit model with an integrated Si spiral inductor using a ground shield, showing the high frequency skin effects and substrate losses. The oxide capacitance and series resistance were traded to optimize the inductor at 2 GHz. The multi-level interconnect scaling and the low k dielectric effects on Q factor were studied. The 0.5 μm CMOS process with five metal layers had closely tallying measurement and model values of L and Q around 10 nH and 6.3 respectively.

In [57] RK ULRIC et al., described that mass produced active components led to significant cost reductions, while the passive components being highly expensive. The big sized passives occupying major die size, were a big hurdle in not only miniaturizing but also making low-cost RFICs. Typical size of a discrete component in a modern RFFE circuit is around 1.125 μm^2.

In [58] AM Neknejad and RG Meyer, analysed the monolithic CMOS inductors, with the eddy current expressions. The Magnetic potential is evaluated using Maxwell's equations to extract the inductance and Q factor with enhanced accuracy. The reported inductor had Q factor of 5, 9 nH inductance, 10.5 μm metal width and an outer dia of 240 μm.

In [59] WB Kuhn and Ibrahim NM, analysed the effects of current crowding in multi-turn spiral inductors at high frequencies, using EM simulations. It is found that the proximity effect had significantly increased the inductor resistance beyond a particular frequency. The fabricated inductor showed an SRF of 2 GHz, Q factor of 8, inductance of 12 nH and an outer dia of 350 μm.

In [60] S Pan et al., analysed the performance of on-chip spiral inductors by varying the geometry parameters like outer and inner diameters. Also examined were the performance influences of the metal spacings, widths and number of turns etc. The maximum values found are an inductance of 6 nH and a Q factor value of 12 corresponding to an outer dia of 220 μm.

In [61] Heng-Ming Hsu, reduced the metal width gradually from outer turn to inner turns using a step change following arithmetic progression. The magnetic field density got reduced, which further decreases the eddy current loss. As a consequence, the inductor series resistance also reduced and the quality factor increased compared to a standard spiral inductor. Quality factor improvement is directly proportional to step width.

In [62] Jinglin Shi et al., reported a pattern ground shield (PGS) inserted below 0.18 μm CMOS fabricated inductor. The metal PGS provided good isolation to prevent the electric and magnetic fields reaching the silicon substrate. This reduced the substrate losses and increased the Q value. The performance testing proved that the use of PGS compensated for the decrease in Q.

In [50] F Huang et al., gave a frequency independent asymmetric model to predict high frequency effects for on-chip spiral inductor. Basically, all the parasitic effects were unified in a comprehensive circuit model to examine the inductors, using IE3D EM simulator. They found that the inductance value decreased if the frequency or the substrate conductivity are increased. A maximum of 1.4 nH inductance was obtained for an outer dia of 200 μm.

In [63] Buyuktas et al., developed a novel technique of reducing the oxide capacitance to improve the Q value of an RF inductor, by employing very low permittivity oxide material. An improvement in Q value from 10 to 15 was reported for a 2.2 nH inductor at an SRF of 3 GHz, with outer dia of 213 μm. The reduction in the overall capacitance value helped moving the SRF to a higher frequency.

In [64] Fang DM et al., reported a high performance MEMS planar spiral inductor fabricated using micromachining method. Measurement results were found for two types of inductors (Type A and Type B). Type- A inductor exhibited 4.61 nH inductance with Q_{max} value of 15.8 at a frequency of 1.4 GHz. Type- B inductor had shown 1.4 nH inductance with Q_{max} value of 19.7 at a frequency of 4.1 GHz.

In [65] Ukaegbu IA et al., had reported a high inductance compact low temperature cofired ceramics (LTCC) octagonal spiral inductor with high Q factor. The semi stacked configuration produced a maximum inductance of 14.41 nH, with a smaller outer dia of 1430 μm compared to a TCC planar spiral inductor.

In [66] X. Jin et al., presented a single π- equivalent spiral inductor model (using parallel LR and an LCR) with PGS. The ground shield produced good isolation between the substrate and passive inductor at high frequencies. The proposed model is validated by the excellent coherence between the circuit model and an EM-simulation up to 40 GHz.

In [67] HA Aebischer, derived a precise inductance formula for rectangular cross section spiral coil with aspect ratio of 4. The formula is similar to current sheet approximation, but the conductor segment gaps being incorporated. The formula is tested with PCB measurements on 16 RFID antennas. This inductance formula had a maximum error value of 1.2 %.

In [68] Hao-Hui Chen et al., developed analytical design for the variable width on-chip spiral inductors. The analytical expression to calculate the metal resistance of the spiral inductor is found by analysing the eddy-current and ohmic losses. A simple design expression to find the appropriate line width for each coil is then determined. The proposed variable width inductor had significantly improved the Q-factor value for several tested 180 nm CMOS spiral inductors.

2.2.2 Multilayer On-chip Spiral Inductor

All the reported planar inductors had shown good high frequency performances, but suffered from the larger occupied chip spaces. Advanced structural designs favoured the stacked multilayer inductors, which placed one conductor turn per each vertical layer on top of the substrate with intermediate oxide layers. This series stacking of inductor turns had increased the overall length and thus increased the overall inductance along with enhanced Q values. Multilayer inductor improved the inductance and quality factor for the equivalent area compared to planar inductors.

In [56] J.N. Burghartz et al., reported a standard 0.8 μm BiCMOS multilayer spiral inductors which consists of four metal layers, with a metal width of 16 μm and metal to metal spacing of 10 μm. The metal layers are connected in parallel using via arrays producing an increased effective metal thickness. This increased thickness had reduced the inductor series resistance which further improved the Q factor. This inductor is proposed with a single metal layer (MM3) with three shunted metal layers (M2/M3/M4) produced Q factor values of 6.5 and 8.6, respectively for an on-chip area of 0.051 mm^2.

In [35] Zolfaghari et al., had designed a series stacked multilayer spiral inductor using 5 metal layers. Layer spacing is increased to reduce the parasitic capacitance between them. This achieved enhanced SRF keeping error difference with analytical model within 5 % only, even at GHz frequencies. This 7-turn inductor had 8 GHz resonant frequency and 45 nH inductance with an area of 0.0576 mm^2.

In [36] Chih-Chun Tang et al., developed a compact 3D inductor in the 0.35um one poly four metal (1P4M) CMOS process. This miniature inductor employed nonsequent metal layers, to reduce inter-layer capacitance and increase the SRF. This 3D inductor exhibited superior performance with a huge 80% area saving relative to planar inductor. This 3D inductor also showed 34% SRF improvement, but with 8% decreased Q value, for the same inductance value occupying the equivalent on-chip area relative to a stacked inductor. A 2.4 GHz CMOS LNA is realized with this miniature 3D inductor that reduced the area and cost of the RFIC.

In [69] P Findley et al., reported a novel differential structure to improve the SRF. This differential design removes high voltage swing and decreases the effective shunt capacitance by 50% for each port. This inductor achieved 60% enhanced SRF compared with a standard differential inductor for same on-chip area.

In [70] N Bheema Rao and AN Chandorkar, developed a 3 D inductor with large inter turn segment distance, that carried currents in opposite directions. This 3D inductor exhibited an improved Q factor by 23 to 25 % along with an added improved inductance by 19 to 23 %.

In [71] I Iramnaaz et al., presented high quality RF inductors employing multilayer structure with alternate ferromagnetic films and copper materials. The skin effect was suppressed mainly due to the zero-effective permeability at the ferromagnetic anti resonant frequency. Hence found increased Q value for this inductor. Reported inductor had 0.5 nH inductance, Q value of 21 at an outer dia of 200 μm. The Q value increased by 86% relative to an inductor based on the conventional copper spiral inductor.

In [49] VNR Vanukuru et al., developed a 0.18 μm CMOS multipath parallel stacked inductor, having metal layers divided into multiple segments, with midway cross overs providing equal path lengths. This inductor achieved 30% Q factor improvement over the standard parallel stacked inductor owing to the decreased proximity effects and skin effects.

In [72] VNR Vanukuru et al., proposed a multipath series stacking octagonal spiral inductor using equal path lengths. This reduced the interlayer capacitance resulting in an increased SRF. Multi-path technique reduced the skin effect and proximity effects. This structure simultaneously reduced both the AC resistance and capacitance and also higher inductance values. This inductor was fabricated on 180 nm Silicon on Insulator (SOI) employing the dual thick metal stacks. It showed 10% improvement in Q_{max} value, 50% improvement in Q_{max} frequency and 100% SRF improvement relative to a standard multipath series stacked inductor.

In [3] BVSM Nagesh and N Bheema Rao, reported the parametric analysis of a miniature 3-D 100 μm ×100 μm on-chip inductor. The influence of number of turns, conductor width and spacing on value of inductance, Q value and SRF were studied. The experimental verification was carried with dynamic variation of associated parameters from 10 to 60 GHz. This analysis had obtained a Q_{max} value of 18 at 30 GHz, a maximum inductance of 5 nH at 48 GHz and an SRF of 72 GHz.

In [73] P Akhendra Kumar and Bheema Rao N, proposed a series stacked multilayer fractal inductor using the modified Hilbert curves. This three-layer inductor had shown two times inductance improvement over planar fractal inductor. The increased thickness of lower metal layer had reduced the inductor series resistance, which increased the Q factor value compared to a standard series stacked multilayer fractal inductor. But, this inductor has moderate SRF value due to inter layer parasitic capacitance.

In [74] Robert Ondica et al., presented an overview of fully integrated multilayer inductors. Different structures are compared based on the key electrical parameters like Q value, inductance L, SRF, Frequency of Q_{max}, and series resistance, etc. geometrical parameters like on-chip area, process technology are also employed. The proposed solution obtained highest inductance density L_A of 23.59 nH/mm^2 and second highest Q value of 10.09 compared with similar reported solutions.

2.3 Review of On-chip Spiral Capacitor Design

Most of the on-chip passives in electronic circuits are the capacitors followed next, by number of resistors and inductors. Majority of on-chip capacitors are categorised into: Parallel plate capacitor, Active Capacitor (MIM, MIS, Gate), MEMS capacitor, and passive capacitor. Metal-insulator-silicon (MIS) capacitor structure is prominent in Silicon ICs for long, due to the ease of fabrication. The double poly structure capacitor produced excellent electrical

performance than MIS. Different capacitor structures were developed to improve the electrical properties for analog circuits, but showed high resistive loss and parasitic capacitance at high frequencies. Metal-insulator-metal (MIM) structures were proposed with higher conductive electrodes, lower parasitic capacitances and good voltage linearity. The 3D integration (IPD) method in silicon is prominently used to manufacture, high-density trench and MIM capacitors [75]. The proposed cost effective simple IPD capacitor in this work employs a thick substrate for loss reduction and thin oxide to accomplish higher capacitance density.

In [76] S.S. Gevorgian, et al., analyzed an interdigital capacitor with a proposed conformal mapping methodology. The proposed model showed good matching results with the available models.

In [77] H Samavati et al., developed a novel fractal capacitor to achieve better linearity, area minimization and process scaling along with the reduction capacitance. With the technology scaling, the capacitance density also increases proportionately.

In [75] A Kar Roy et al., showed the first successful 0.25 μm CMOS RF integrated MIM capacitor. It had capacitance density of 2.0 fF/μm^2 with Q value of 80 at 2 GHz. This had indicated that high density sub-micron MIM capacitors are suitable for successful integration in the mixed-signal applications.

In [78] Armacost M et al., proposed a highly reliable 0.18 μm copper MIM capacitor for the first time. It achieved capacitance density of 0.72 fF/μm^2 which is higher than that of an aluminum MIM capacitor.

In [79] Imamura M et al., proposed a bent comb capacitor (BCC) using the standard 0.13 μm CMOS technology. This BCC possessed smaller parasitic inductance. It achieved 0.85 pF capacitance with an area of 0.01 mm^2.

In [39] Subramaniam K et al., proposed a lumped circuit model for multilayer finger capacitors. The voltage, temperature and process variations, variations of the parasitics and series resistance are included. The scattering parameters are converted into the circuit model parameters. The equivalent circuit lumped elements for finger capacitor is also presented.

In [80] Nikhat Dib et al., developed a lumped circuit model for a coplanar wave (CPW) interdigital capacitor. It measured the value of series capacitance accurately compared to the

ful1l wave Method of Mordents. A multilayer feedforward artificial neural network (ANN) is used to model this CPW interdigital capacitor.

In [81] M. Bakri-Kassem et al., presented a MEMS variable capacitor with career beams possessing a high tuning range. This capacitor is fabricated in polyMumps process with capability to operate up to frequency range of 11 GHz.

In [38] P. Gonon and C vallee found an analytical expression to evaluate the nonlinearities in MIM capacitors and predict the voltage coefficients of MIM capacitance accurately. However, the area of these MIM capacitors increases with the CMOS process scaling. Lateral flux interdigital capacitors were proposed to follow technology scalings. The signal spreads to multiple fingers to exploits the fringe capacitance created between the fingers.

In [82] Y. Chen et al., developed and fabricated a glass substrate MEMS spiral capacitor. It possessed 0.54 pF capacitance value from 0.2 to 8 GHz with a Q factor value of 300. This capacitor is compatible to copper fabrication.

In [40] AM Elshurafa and KN Salama presented a MEMS fractal capacitor. It achieved a highest SRF in polyMUMPS. Experimental results showed the Q value of 4 from 1 to 15 GHz with an SRF of 20 GHz. Fabricated capacitor achieved a capacitance of 2.9 pF at an SRF of 4 GHz.

In [49] V.N.R. Vanukuru et al., developed a miniaturized 0.18 μm process mm wave BPF using an interdigital capacitor. The designed interdigital capacitor had higher Q factor (>15) better than that of an MIM capacitor. This BPF does not need any MIM processing, which minimized the fabrication cost. The IDC employed has effectively exploited the fringe fields to enhance the capacitance value per unit area, at the cost of inherent parasitics.

In [41] P Akhendra Kumar and N Bheema Rao simulated and fabricated a single layer fractal spiral capacitor. The PCB prototype fractal spiral capacitor tested using VNA produced results showed that the fractal concept had increased capacitance by 10.3% and Q value improved by 52.4% along with SRF increased by 20% relative to a standard spiral capacitor.

In [83] Silvester Vančík et al., developed a 3D miniature on-chip capacitor using high K dielectric materials on Si wafer. Property of metal-oxide compounds Al_2O_3 and HfO_2 as dielectrics for on-chip MIS capacitors are studied to increase the capacitance density.

Experimental results showed very good break down voltage and leakage currents. Trenches are fabricated as 100 mm^2 silicon chips on a 4-inch Si wafer to enhance the capacitance density.

In this summary, the research and development of the high performance on-chip capacitors is presented with a review of their innovative design methods to exploit vertical and lateral flux fields.

2.4 Review of On-chip Low Noise Amplifier Design

Being the first gain elevator, LNA is the direct influencer of overall noise performance of any receiver. LNA design is a bit tough, owing to the challenges involved in achieving low Noise Figure (NF), high gain, low power consumption, good input matching, and better linearity. Different LNA topologies and circuit configurations were researched in the past that yield high performances. Mostly, the active components of LNA circuit are designed with low-cost CMOS technology, while the on-chip passives are realized in small area IPD technology. This helped to reduce power loss smaller than CMOS process, but possess very low chip space. This work had proposed compact low noise figure LNA using constant width, variable width and double split series stacked multilayer IPD inductors designed and simulated in ADS at 5 GHz and 8.2 GHz.

In [84] Choi BG et al., implemented a two stage source degenerated LNA using the PHEMT MMIC resulting a very low NF of 0.76 dB and gain more than 16 dB at 5.4 GHz. The minimal parasitic resistance of the on-chip single spiral inductor input matching network helped to achieve such lower NF.

In [85] Fanucci L et al., designed a fully integrated 3V LNA using bootstrapped inductor and a preselecting input filter. It achieved a gain of 36 dB, Q value of 13, bandwidth of 140 MHz and small 2 dB NF at 1.8 GHz. The manufactured LNA IC had small dynamic range with 1 dB compression point of -46 dBm.

In [86] D Barras et al., presented a low power 0.25 μm SiGe BiCMOS LNA for UWB radio front end. This LNA used peaking inductor and a double feedback to optimize its gain and impedance matching, It showed a 10 dB peak gain and a 5 dB noise figure over 3.4 to 6.9 GHz. The LNA consumed only 3.5 mW using a 1V supply.

In [87] D Linten et al., designed for the first time a low power 5.5 GHz fully integrated 90 nm RF CMOS LNA with the electrostatic discharge (ESD) protection. This LNA demonstrated a power gain of 13.3 dB, return loss of –14 dB, 1.35 GHz bandwidth, 9.7 mW power consumption, 2.9 dB NF and IIP3 of -2.7 dBm.

In [88] Hsieh-Hung Hsieh et al., presented a folded cascode 180 nm CMOS LNA with gain enhancement stage and a capacitive divider in 5 GHz band. This LNA had a remarkable 14.1 dB gain with DC power of 1.68 mW.

In [89] A Pourmand et al., presented a fully integrated 0.18μm CMOS cascode LNA using on-chip spiral inductor matching network for IEEE 802.11a applications. LNA power consumption is reduced to 16 mW with a gain of 17.82 dB and reverse isolation of -58.37 dB at 5.5 GHz. The values of S11 and S22 are -16.1 dB and -32 dB, respectively. This LNA has IIP3 of +3 dBm and a NF of less than 2.9 dB.

In [90] Anuj Madan et al., reported an inductively degenerated cascode 5.0 GHz CMOS LNA featuring using a body contact NMOS transistor and high Q on-chip passives. This LNA achieved a record NF of 0.95 dB, gain up to 11 dB, 5 dBm IIP3, input return loss of -33 dB, while consuming only 12 mW.

In [91] Masumesh Shams et al., reported a three stage 3-10.6 GHz wideband UWB 130 nm CMOS LNA employing current reuse, a resistive feedback and an inductive peaking common source (CS) amplifier configuration. This LNA circuit has 17 dB power gain. NF of 5.5 dB, IIP3 of -7.7 dBm and 15 mW power from 1 V supply. The input and output return losses are -10 dB and -25 dB, respectively.

In [92] S Mallick et al., reported a source degenerated LNA circuit employing particle swarm optimization (PSO) algorithm executed in MATLAB. The variables like the inductor, capacitor and aspect ratio values are used to optimize the CMOS LNA design. The implemented 180 nm CMOS LNA produced a gain of 22.0 dB, NF of 0.8 dB and power consumption of 6.6 mW.

In [93] Zhengmin Ke et al., presented a compact 0.81 dB low noise 5 GHz LNA using SISL platform and pHEMT transistor. This self-packed structure with air cavity is easy to fabricate on PCB has advantages of size reduction and lower dielectric losses. It had power gain of 23 dB, S11 of -16 dB and an area of 528.5 mm^2.

In [94] Hsien-Ku Chen et al., designed a CMOS LNA using the off the chip high Q IPD passive inductor for input matching and improving the noise figure. The large 4.7 nH IPD inductor is stacked vertical on top of CMOS IC for chip area savings. This novel IPD integrated CMOS LNA is cost effective and also possessed high performance against pure CMOS LNA. This CMOS IPD codesigned 2-11 GHz LNA exhibited gain of 12, minimum NF of 3.4 dB, and power consumption of 12 mW with an area of 0.36 mm^2.

In [32] Sunil Kumar T and Bheema Rao N, proposed an orthogonal differential series stacked inductor based 28 GHz 90 nm CMOS LNA for 5G band. Measured results for a multilayer PCB fabricated fractal inductor had shown doubled inductance, 56% enhanced Q factor, and 33% reduced series resistance relative to a standard fractal inductor for an equivalent on-chip area. LNA with above inductor achieved an enhanced gain of 30.668 dB, lower NF of 0.7 dB, a return loss of – 10.44 dB, power consumption of 5 mW for 2.2 V supply in 27-30 GHz.

In [95] Jin-Fa Chang et al.,] proposed a body floating self-biased 3–9-GHz CMOS LNA for Sub-6-GHz 5G Communications. This LNA exhibited S11 of -10.1 to -41 dB, S12 of 10.7 dB, consumed power of 1.36 mW at 0.8V supply, NF of 3.46 dB, IIP3 of -6.2 dB and a bandwidth of 6 GHz.

In summary, majority of the past developed CMOS LNAs greatly enhanced several performance metrics, however the occupied die sizes being still very large. This work had employed the IPD on-chip passives successfully to develop high performance 5G CMOS LNAs with minimized die size.

2.5 Review of On-chip Bandpass Filter Design

Performance deciding RF BPF circuits were successfully designed and implemented with high Q passive devices for SOC applications. The miniature RF BPF design research favours IPD passive’s based Si CMOS technology, based on their lower power consumption, smaller footprints, and good integration capabilities. Obtaining least on-chip area (OCA), lowered insertion loss, improved gain, low noise figure and better selectivity are still big challenges faced in design of passive BPFs [96]. Many passive LC resonator BPFs using Si IPD CMOS technology were proposed in recent past to suit 5G radio access applications. This work had developed and implemented the compact high performance BPFs using the proposed

multilayer series stacked IPD inductors and planar capacitor for 5G communications at 8.2 GHz and 25 GHz.

In [97] Yue Wu et al., proposed a 2nd order 900 MHz tunable BPF using pMOS active inductor in 0.35 μm CMOS process. This fabricated filter has Q value of 40, gain of 15 dB, IIP3 of -15 dBm and chip area of 0.028 mm^2.

In [98] WS Tung et al., implemented a mmWave inductive π-network BPF using the Monolithic microwave integrated circuit (MMIC) technology. The fabricated 26 GHz lumped resonator filter showed 5 dB insertion loss and -16 dB return loss in the passband with an occupied area of 0.0176 mm^2.

In [99] Ching-Wen Tang et al., designed a broadband 3.875 GHz BPF using low temperature co-fired ceramic (LTCC) BPF employing a quadruple resonator with MIM capacitors. The fabricated filter measured results showed transmission zeros of 0.8, 5.25 and 8 GHz. Its insertion loss is 2.5 dB, return loss is 13 dB and area is 6.8 mm^2.

In [100] AA Saadi et al., proposed an efficient 0.18 μm CMOS UWB BPF implementation based on hourglass function using a zigzag technique, covering UWB spectrum from 3.1 to 10.6 GHz. This filter good 11 dB matching, 1.8 dB insertion loss and 15 dB stop band rejection.

In [101] BVNSM Nagesh Deevi and N Bheema Rao, proposed a simple 40 GHz on-chip LC resonator BPF using multilayer passive elements. This miniature BPF circuit had 3.17 GHz bandwidth, 8% fractional bandwidth, Q value of 12.5, S11 of -18 dB, S12 of -2.1 dB and an occupied area of 0.0256 mm^2.

In [102] Peng Dong et al., presented the design of Si cavity 5.6 GHz BPF using interdigital resonator with MEMS fabrication technology. The measured and HFSS simulation results closely match with 2.04 dB insertion loss, 16% fractional bandwidth and a chip size of 43.8 mm^2.

In [103] Ki R Shin et al., discussed a compact low-cost BPF using 1608 size Si IPD process for 5G NR n78 band. Transmission zeros used in top coupled filter resulted in 1.8 dB insertion loss, outband rejection more than 30dB. Filter showed S11 of -25 dB and occupied area of 1.28 mm^2.

In [20] Yasir IA Al-Yasir et al., reviewed the progress in design of microstrip and reconfigurable 4G/5G filters. Also discussed the current advancements in high quality resonator filters with tunable bandwidth, center frequency and selectivity. Survey on reconfigurable mm Wave filters for the present and next generation of wireless communications is also given. Most recent research results are summarized in the performance comparison.

In [104] J Song et al., presented compact 4th order 2.8 GHz BPF using GaAs IPD process combline filter. The tested and simulation results closely tallied with 5 dB insertion loss, 30 dB stop band rejection and a chip size of 1.84 mm^2.

In [82] Yang Chen et al.,] presented a compact 1.8-3.0 GHz BPF using IPD on GaAs substrate. LC resonators yielded high selectivity by using transmission zeros. Experimental and simulation results tallied for less than 3 dB insertion loss, outband rejection more than 33 dB. Filter showed fractional bandwidth of 50%, S11 of -12 dB and occupied area of 2.86 mm^2.

In [105] Naser O Parchin et al., developed a compact 2.8-11 GHz UWB microstrip BPF using coupled stubs in a top layer with defected ground structure (DGS) in bottom layer, on a Rogers 40030C substrate. This filter demonstrated three resonant frequencies at 3.8 GHz, 7.4 GHz, and 10.5 GHz. This filter had S11 of -22 dB and S12 of -1 dB at 7.4 GHz, with an area of 64 mm^2.

In [106] Pao-Nan Lee et al.,] demonstrated the design and fabrication of a 5G n77 and n79 BPFs on glass IPD layer stack. The n77 BPF showed only 1.4 dB loss in 3.3 to 4.2 GHz, 30 dB attenuation at 2.69 GHz and 5.15 GHz. The n79 BPF showed only 2 dB pass band loss in 4.4 to 5 GHz, with 17 dB attenuation at 5.49 GHz. Both filters have same area of 2.5 mm^2.

In [96] Xiaozhen Li et al., proposed a miniature 3.9 GHz BPF fabricated using the GaAs IPD process. The filter showed a measured 3 dB insertion loss, return loss of 10 dB, a 3 dB bandwidth of 1.2 GHz, and an occupied area of 1.13 mm^2.

In [107] Yusuke Uemichi et al., fabricated a low loss narrowband 28 GHz 5G BPF using Si post wall waveguide (PWW) with 5 resonators. This BPF circuit had 2 GHz bandwidth, 7% fractional bandwidth, Q value of 14, S12 of -1.3 dB and an occupied area of 110 mm^2.

In [108] Hao Wu et al., fabricated a 4th order LTCC tunable bandwidth and center frequency BPF, employing four circular patch resonators and two varactors to produce three transmission zeroes. This BPF had demonstrated a 50 MHz bandwidth at 2.86 GHz, 7% fractional bandwidth, Q value of 14, S11 of -13 dB, S12 of -3.5 dB and an occupied area of 66 mm^2.

In [109] Alina-Cristina Bunes et al., fabricated GaN/Si SAW resonator 8 GHz BPF. The filter showed a measured 13.2 dB insertion loss at 8.06 GHz, 10 dB reflection loss, Q value of 403, 20 MHz bandwidth and an occupied area of 2.175 mm^2.

2.6 Summary of the Literature Review

This chapter reports a thorough review of the past research works done on the on-chip passives and also the key 5G RFFE building blocks like LNAs and BPFs. A progress review on the optimization of several high performance on-chip spiral inductor is presented. Spiral inductor performance is enhanced by design transformation from a single planar layer to the multilayer IPD process. Past research optimization methods tried to improve Q factor by reducing the substrate losses and minimize the chip area using multilayer concepts. The benefits of IPD multilayer inductors have motivated to take up this research work to design and successfully develop highly miniaturized on–chip passives employing IPD technology.

Especially, this work focusses on using these small area IPD passives to further reduce the die sizes of the key performance deciders like LNA and BPF for globally proliferating 5G wireless communications. Thorough review of the past research works on the LNA and BPF circuits is briefly presented to understand the past research conducted in this direction.

Chapter 3

Design and Implementation of Passive Components

3.1 Introduction

On chip Passives became key performance deciders above 1 GHz due to their noise and power advantages. Researchers faced difficulty to integrate the on-chip inductors in practice, due to their large size, high noise, substrate and metal losses, and low Q values at GHz frequencies. The size of active devices was getting reduced with CMOS technology scalings. It was very difficult to place the nH inductance values off the chip for GHz inductors in small sized CMOS RFICs [110]. Placing the integrated inductors in CMOS is a challenge, due to their large influence on the performance of RF circuits. The Q factor of an inductor in CMOS is limited by the substrate and metal losses inherently present with the CMOS technology.

The design of on-chip passives need trade-off between the cost of technology provisions and application demands, posing many challenges like design complexity, high quality factor, least on-chip area and manufacturing costs. Among several types of the on chip inductors, square shaped spiral inductors are popular RFIC choice due to their ease of modelling, design and fabrication. Conventional spiral inductors built on a high conductive substrate in the CMOS process suffers from high capacitive and magnetic losses [111]. The smaller footprint multilayer spiral geometry passives are attractive as they exhibit large values of inductance, capacitance and good quality factors. Highly miniaturized on-chip passives heavily reduce the occupied chip space and lead to size and weight reduction for 5G devices

and terminals [65]. Miniaturization of the silicon inductor is of prime importance in state of art research.

All this made researchers to develop the IPD technology, which could move the bulky off-chip passives into RFIC circuits as miniature on-chip passives. The IPD technology employs minimum area multilayer geometry to produce the miniature on chip passives (L and C). IPD technology permits easier integration (stacking) of small size on chip passives along with low-cost CMOS circuits, to realize size reduced RFICs. High performance miniaturized on-chip IPD passive components are being integrated today with low-cost CMOS 5G RFICs, on the same substrate [112]. Happy integration of IPD with CMOS technology is core theme behind the design and development of efficient 5G RFFE circuits like LNAs and BPFs in the current research for low-cost and low size miniaturized 5G RFICs and systems. The on-chip passives helped the RF filters to achieve increased performance than that of the active filters, because of high linearity, higher center frequency, low noise and interference. The on-chip passives helped the RF amplifiers to possess high gain, stability, good linearity (IIP3) and small noise figure etc.

This chapter presents the enhancement of both the inductance and quality factor metrics along with chip space reduced inductor structures, by taking the advantage of multilayer geometry. Multilayer inductors were successful in the inductance improvement, capacitance enhancement, increased Q factor, and increased SRF etc. Initially, the standard spiral inductors are proposed and implemented in IPD multilayer structure to obtain the enhanced inductance and Q (for same on chip area) for a broad frequency range of 1-16 GHz. Later the constant width and variable width series stacked spiral inductors are proposed for 5G bands. Variable width and multitrack methods reduce the proximity effects and skin effects to increase the inductance and Q factors. We proposed a novel Double-split series stacked multilayer IPD inductor structure which not only exhibited very good performance but also possessed the minimum area occupied on chip, at different 5G frequencies. A planar and a multilayer spiral capacitor are also designed in this work.

Modelling of the on-chip passive elements is categorized into three broad impedance extraction techniques [3].

- Electro Magnetic (EM) field solution model :

  The available EM field solving simulators best solve the Maxwell's equations for given boundary conditions, to provide an accurate model. For example,

Ansoft's High Frequency Structure Simulator (HFSS), EM-Sonnet, MG-IE3D, Dassault Systems CST Studio, Agilent/Keysight Advance Design System (ADS), etc. these simulators solve the Maxwell's integral equations employing different mathematical methods. For Example, IE3D employs method of moments, HFSS and ADS employ the finite element methods. These simulators are capable to produce best accurate solutions but they are computationally intensive with time consuming executions. However, they help the designers to easily verify the suitability of proposed model and design the on-chip passives for RF problems.

- Distributed model:

  On-chip passive analysis permits that every metal segment in a spiral turn is assumed as an individual line and hence very turn (conductor path) is treated as a distributed network line. Thus, for every single turn (arm) of square spiral in one layer, a total of four distributed networks shall be solved equivalently, as shown in Fig. 3.1. So, each conductor segment equivalently consists of series resistance, series inductance and associated parasitic capacitances. The self-inductance and mutual inductances are calculated using Greenhouse method or Wheeler method. The distributed model is simple but has large complexity relative to an EM field solver. For multi turn passive structures, this model needs huge run time simulations.

- Lumped equivalent model:

  The heavy computational burden of above two methods, is minimised by the lumped π–equivalent circuit, as depicted in Fig. 3.2. This model shall be incorporated into a circuit simulator to provide final solution. The π–equivalent circuit model comprises of inductor metal turn with its series resistance, metal spiral to substrate capacitance and a shunt parasitic capacitance. Thus, this model is also referred to as series LC model and shunt RC lumped π–circuit model. Usually, this lumped models provide good accuracy till the desired SRF where the passive element behaves like an inductor. Also this model possess fast run times and help achieving compact sizes also. Hence in practice, this lumped inductor model is prominent in on-chip passive research.

The performance metrics for any Induct6or are its quality factor (Q), inductance value L, and SRF (f_{SRF}). These are primarily influenced by the design control (lateral/structural)

parameters and process parameters. Lateral parameters include the substrate resistance (R_{si}), Substrate capacitance (C_{si}), oxide capacitance (C_{ox}) and spiral capacitance (C_s). The lumped π–equivalent circuit model is developed depending on these lateral parameters as shown in Fig. 3.1, for a typical single turn on-chip square spiral inductor [34]. The distributed circuit model, is depicted in Fig. 3.2.

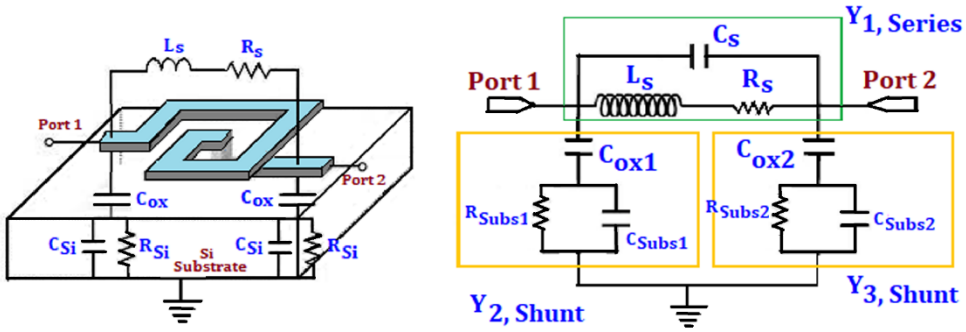


Figure 3.1 Structure of a single turn square spiral inductor and its lumped π–equivalent circuit model

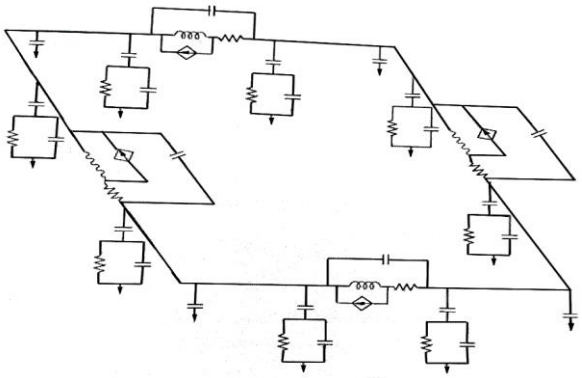


Figure 3.2 Distributed circuit model of a square spiral inductor for four conductor segments
Courtesy: *https://en.wikipedia.org/*

The inductance of the passive spiral inductor is represented by series inductance L_S. Other elements of equivalent circuit show the parasitic mechanism corresponding to the layout of the structure. R_S is the resistance of the metal segments and the underpass. C_S is the capacitance existing between metal paths. Substrate resistances R_{SUB1} and R_{SUB2} are proportional to the area of the metal turns above substrate. C_{OX1} and C_{OX2} are the capacitances formed between the metal paths and oxide layer. C_{SUB1} and C_{SUB2} models the substrate capacitances.

These developed IPD inductors and capacitors are fabricated on PCB to validate the design simulations. The design and simulation of the proposed IPD inductors and their applications are carried out by using High-Frequency Structural Simulator (HFSS), Advanced

Design System (ADS), and Sonnet EM simulator. The proposed IPD inductor and capacitors are fabricated on FR4 substrate due to manufacturing difficulty and technology limits on silicon. The results of these simulations are in veery good concurrence with experimental results and successfully validated. They are further used to implement the LNAs and BPFs for 5G applications. The design, simulation and fabrication of above three types of multilayer IPD inductors are presented in section 3.2, 3.3 and 3.4, correspondingly.

3.2 Multilayer IPD Inductor

3.2.1 Constant Width Planar (Single Layer) Inductor

The conventional RF on-chip inductors started with a single layer structure referred to as planar inductor, which is highly compatible with an RFIC interconnect. It may comprise of one or more conductor turns depending on the performance requirements. The planar spiral inductor is chosen because of its small size, large positive mutual inductance, excellent Q-factor value and ease of design. Inductors realized on Si substrates use a minimum of two metal layers [101]. Top layer houses the inductor structure while the bottom layer brings the port connection outside by an underpass contact. A constant width spiral inductor is proposed as shown in Fig. 3.3. It is a popular simple choice on-chip inductor, due to ease of generation by any standard layout tool. The HFSS simulated planar inductor structure is also shown.

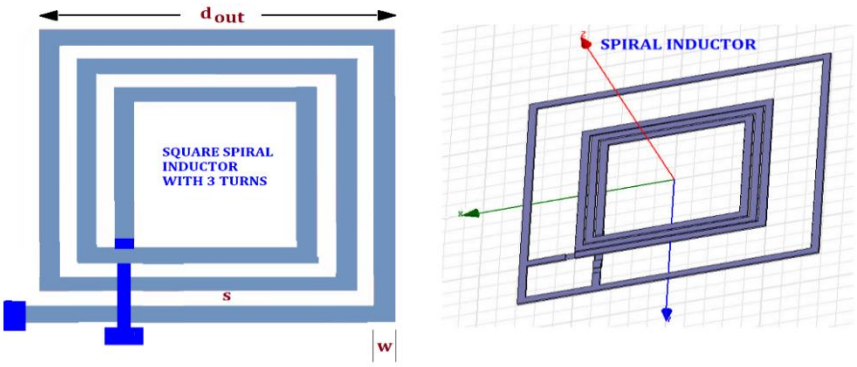


Figure 3.3 Three turn constant width square spiral inductor and its HFSS simulated structure

The geometry parameters of the inductor structure are: metal width (w), metal spacing (s), outer dia (d_{out}) and number of metal turns (N). In this structure, the conductors which carry the current in same direction, are close to each other. The conductors carrying current in the opposite direction, are distanced apart. This increases the net positive mutual inductance and

enhances total value of inductance. Most important design parameter of a spiral inductor is quality factor Q, which is a function of both the frequency and the geometry. Electromagnetic coupling between metal lines, makes it challenging task to model a spiral inductor.

Design equations for single layer square spiral inductor are evaluated for the above π–equivalent circuit model, as.

$$R_s = \frac{\rho l}{W\delta\left(1-e^{t/\delta}\right)} \qquad C_s = \frac{nW^2\varepsilon_{ox}}{t_{ox}} \tag{3.1}$$

$$C_{Subs} = C_{ox}\frac{\left[1+\omega^2(C_{ox}+C_{Si})C_{Si}R_{Si}^2\right]}{1+\omega^2(C_{ox}+C_{Si})^2R_{Si}^2} \tag{3.2}$$

$$R_{Subs} = \frac{1}{(\omega^2C_{ox}^2R_{Si})} + \frac{\left[R_{Si}(C_{ox}+C_{Si})^2\right]}{C_{ox}^2} \tag{3.3}$$

where, $\boldsymbol{\ell}$ is total spiral length, n is number of turns, W is metal width, t is metal thickness, t_{ox} is oxide thickness, ρ is resistivity and δ is skin depth. SRF is the frequency where the parasitic capacitance resonates with the ideal inductance to result in very high impedance. Below this frequency, it acts as an inductor. The main objective is to obtain a desired inductance in least chip space, while keeping parasitics low enough to ensure that the SRF is outside the desired frequency band. The inductance L and quality factor Q are computed form Y parameters obtained from the simulated S-parameters.

$$Inductance\ L = \frac{Im\left(-\frac{1}{Y_{12}}\right)}{2\pi(frequency\ f)} \qquad Quality\ Factor\ Q = \frac{Im(Y_{11})}{Re(Y_{11})} \tag{3.4}$$

$$Self\ Resonant\ Frequency\ f_{SRF} = \frac{1}{\sqrt{2\pi LC}} \tag{3.5}$$

Where Y_{11} and Y_{12} are the Y-parameters of the π-circuit model.

The design and simulation of on-chip square spiral inductor is performed with the specifications given in Table 3.1.

The designed on-chip planar spiral inductor with three turns is simulated in the Ansoft HFSS software. The S-parameter results obtained from HFSS are converted into Y parameters and further into the performance parameters: Inductance L, Q factor Q and SRF. The inductance sweeps and variation of Q factor for this 3 turn planar spiral inductor are shown in Fig. 3.4.

Table 3.1 Design specifications for the planar square spiral inductor

PARAMETER	SPECIFICATION
Number of Turns	3
Material	Copper
Width of metal turn μm	8
Thickness μm	2
Substrate	Silicon Si
Oxide	Silicon Dioxide SiO_2
Spacing between turns μm	2
On-chip area mm^2	0.048

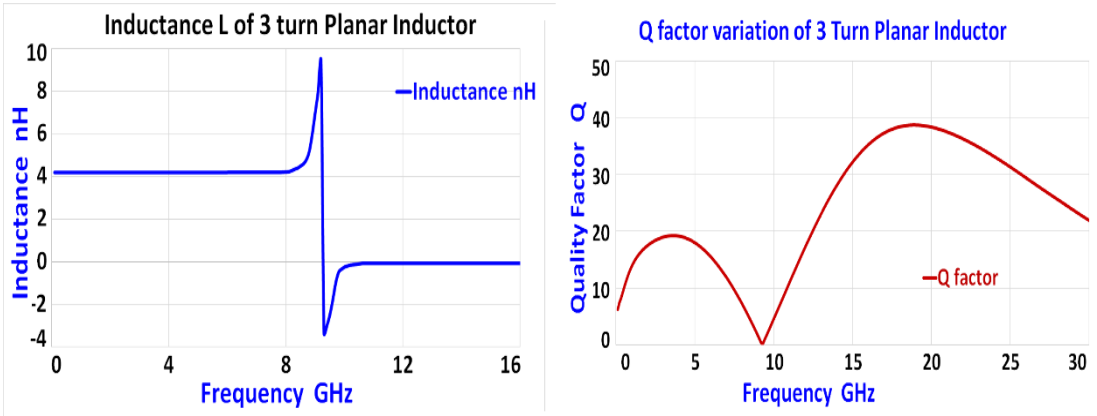


Figure 3.4 Inductance variation and Q factor variation for 3 turn planar square spiral inductor

Table 3.2. Performance comparison for proposed planar inductor with state-of-art

Ref.	L(nH)	Q_{max}	No. of Turns	Outer Dia (μm)	Rs (Ω)	f_{SRF} (GHz)	f_{Qmax} (GHz)	Chip Area (mm^2)
Ref. [64]	4.61	15.8	5.5	1920	-	9	1.4	3.686
Ref. [68]	3.46	7.88	3	160	6	20	3.3	0.0256
Ref. [3]	0.804	17.3	3	100	-	80	20	0.001
This Single Layer Planar Inductor	**4.195**	**19.25**	**3**	**220**	**28**	**9.28**	**3.6**	**0.048**

The SRF of this planar spiral inductor is equal to 9.28 GHz. Its inductance is 4.195 nH at 5 GHz. The maximum Q value exhibited below the SRF is equal to 19.25 at 3.6 GHz. Hence, this inductor is suitable for the 5G RFIC circuits in C and X bands. The simulated performance results of this three-turn planar spiral inductor are compared with state of the art, in the Table 3.2.

3.2.2 Constant Width Three-layer (Multilayer) Inductor

Square spiral geometry simplifies the fabrication complexity along with uniform current density. Hence this shape is prominently employed to design both the on-chip IPD inductors and capacitors. Series stacked multilayer inductor structures became popular due to footprint reduction, as they need smaller outer dia for equal inductance. Else they exhibit increased inductance for same on-chip space. 3D inductors need fewer turns for given inductance. Fewer turns not only reduce inductor size but also help reduction of substrate related losses, which further enhances Q value of 3D structures. ML inductors have very high self-inductance and mutual inductance due to presence of vertical and lateral conductor coupling. The upper layers are protected from the substrate losses and effects as the lowermost metal layer acts as a shield to them and hence the same inductance of planar structure is achieved with lesser area in stacked inductor. They also showed improved self-resonant frequency over conventional spiral inductors.

In order to reduce the device losses, thick substrate layers and high conductivity materials were considered. Placement of non-orthogonal metal layers with parallel conductor geometry enhances inductance and Q values yet possessing minimal proximity effects and parasitic capacitances. But they have higher metal to metal capacitance. Device geometry parameters are traded with process parameters to develop low loss and yet super compact Inductors [113]. Most RFIC fabrication processes are employing multilayer structures with easier integration capabilities utilizing popular IPD technology. It is proposed a novel 3-Dimensional series stacked ML inductor structure with full CMOS compatibility

Greenhouse method (based on Grover's formulas) evaluates the net inductance as the sum of self and mutual inductances. The mutual inductance is sum of positive mutual (M_+) and negative mutual (M_-) inductances. The opposite current carrying conductors are placed in different layers in order to increase the distance between conductors. This placement results in decreasing the negative mutual inductance and increasing the overall inductance. The electromagnetic coupling between the metal lines, metal-substrate, makes it a big challenge to

model a ML stacked spiral inductor. Parasitic resistances are reduced and Q factor value is increased for spiral inductor, with copper conducting material. The proposed inductor employed run of copper conductor on a thick Si substrate.

This three-layer three turn inductor is designed with 3 conductor turns per each layer. This configuration is characterised by the absence of non-orthogonal conductors with oppositely flowing currents on the same metal layer. This three-layer ML constant width spiral inductor is designed with a constant width of 10 μm for all the turns in each layer. The spacing between each conductor path is 2 μm. Conductor thickness is 2 μm. The inductor has 3 turns per each layer. The inner and outer diameters are 61 μm and 180 μm. On-chip area occupied is just 180 μmx180 μm (0.0324 μm^2) excluding the ports. A 300 μm thick Si substrate layer and 10 μm thin oxide layer are chosen to reduce losses, which further increased the operating frequency and also the Q-factor. Design and simulation of on-chip series stacked ML square spiral inductor is performed with the specifications given in Table 3.3.

Table 3.3 Design specifications for the series stacked multilayer IPD spiral inductor

PARAMETER	SPECIFICATION
Number of Layers (Levels)	3
Number of Turns	1
Material	Copper
Width of metal turn μm	10-10-10
Thickness μm	2
Substrate	Silicon Si
Oxide	Silicon Dioxide SiO_2
Spacing between turns μm	2
Spacing between Levels μm	2
On-chip area mm^2	0.0324

The designed on-chip IPD spiral inductor with three turns is simulated in the Ansoft HFSS software. The S-parameter results obtained from HFSS are converted into Y parameters and further into the performance parameters: Inductance L, Q factor Q and SRF. The proposed three turn constant width multilayer spiral inductor planar view, 3D view and its HFSS simulated structure as shown in Fig. 3.5.

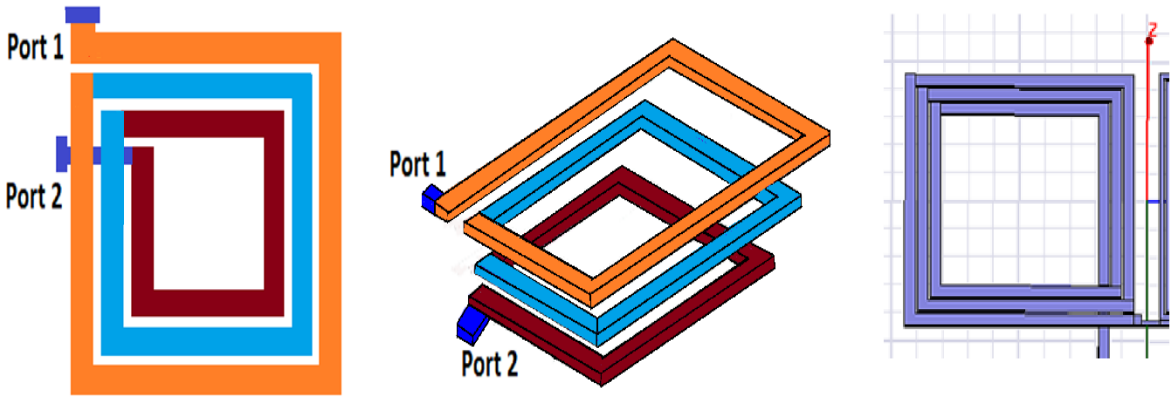


Figure 3.5 Three turn constant width multilayer spiral inductor - planar view, 3D view and its HFSS simulated structure

The inductance sweep and variation of Q factor for this 3 level single turn ML spiral inductor for 0-25 GHz are shown in Fig. 3.6.

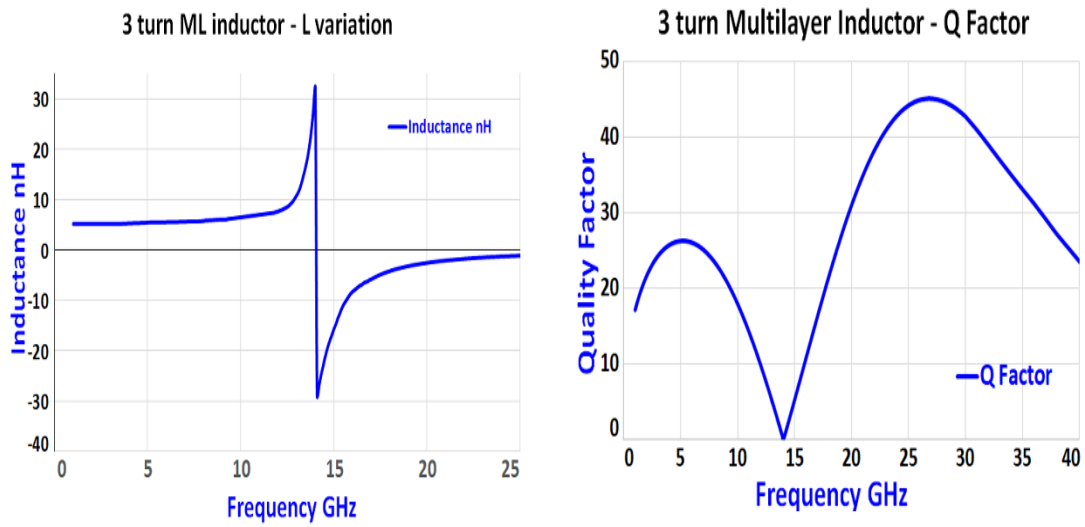


Figure 3.6 Inductance and Q factor variation for 3 turn multilayer spiral inductor

The SRF of this 3-level single turn (3/1) ML spiral inductor is equal to 14 GHz. Its inductance is equal to 5.42 nH at 5 GHz. The maximum Q value exhibited below the SRF is equal to 26.3 at 5.1 GHz. Hence, this inductor is suitable for the 5G RFIC circuits in C and X bands. The simulated performance results of this three turn ML spiral inductor are compared with state of the art, in the Table 3.4. The results of the three-turn planar inductor also are compared with multilayer IPD inductor.

Table 3.4. Performance comparison for the proposed ML inductor with state-of-the art

Ref.	L(nH)	Q_{max}	Levels/ Turns	Outer Dia (µm)	Rs (Ω)	f_{SRF} (GHz)	f_{Qmax} (GHz)	Area (mm^2)
Ref. [114]	10.5	12	2/7	220	15	4.5	2.2	0.0484
Ref. [115]	2.3	11.8	2/7	400	-	14	1.8	0.16
Ref. [3]	5	18	2/4.5	100	-	72	30	0.01
Our 3_turn Planar Inductor	4.19	19.25	1/3	220	28	9.28	3.6	0.048
This 3_turn ML Inductor	**5.42**	**26.3**	**3/1**	**180**	**24**	**14**	**5.1**	**0.0324**

These results indicate a clear possibility of geometry optimization, which simultaneously improved the quality factor, inductance and area efficiency significantly. It is also clearly proven that the multilayer inductor has better performance than the planar inductor for same dimensions.

3.2.3 Three-layer Bidirectional (Multilayer) Inductor

It is also proposed to develop and analyse the performance of a bi-directional multilayer spiral inductor to enhance the metrics L and Q. Literature review showed their enhanced performance. Bi-direction means that every layer has only one-half conductor turn and the second half placed in next layer using a via connection. Thus a 3 turn inductor structure requires 6 layers. A symmetric bi-directional inductor is proposed with the structure having conductor path traced from metal layer 1 to metal layer 2 and then to layer 3 in particular direction. Its normal and 3D views are shown in Fig. 3.7 correspondingly.

The conductor path can be run in random or sequential, typically chosen to increase the L and Q values. For random metal run, let the first half conductor turn is run in layer 1. The next half conductor turn of this path can be placed in any other of remaining 5 layers. It is decided to place it in layer 6 to increase the inter layer spacing to maximum possible, to minimize the parasitic capacitance, which leads to minimum loss and higher Q value. The sequence of conductor half turns selected in this simulation are first half turn in layer 1, next half turn in layer 6, next half in layer 3, next in layer 5, next one in layer 4 and the last half in

layer 2. The inter layer spacing is uniformly maintained at 10 μm. The physical dimensions of this bi-directional IPD inductor are: 8 μm conductor width, 2 μm conductor spacing, 2 μm conductor thickness and 10 μm layer spacing.

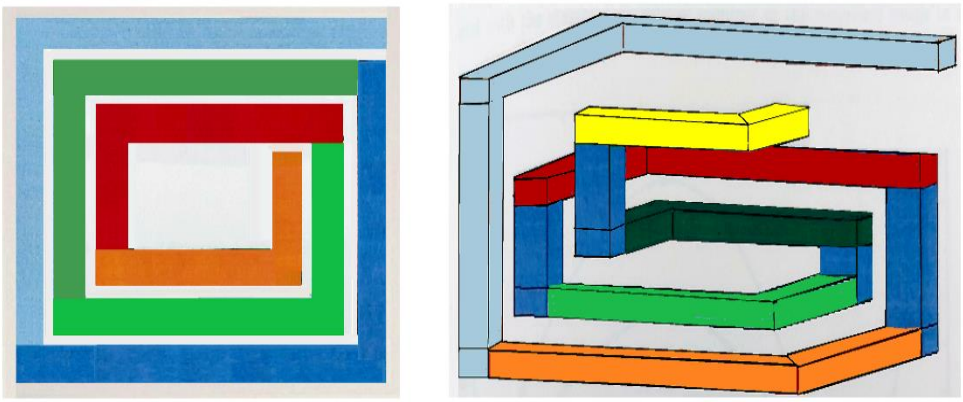


Figure 3.7 Normal and 3D views of 3 turn 6 layer bi- directional multilayer spiral inductor

The RF performance of this proposed bi-directional inductor is compared with previous reported three turn multilayer inductor in terms of its inductance and Q value variations as shown in Fig. 3.8. They clearly depict the improvement of bot these metrics by the bi-directional multi-layer inductor.

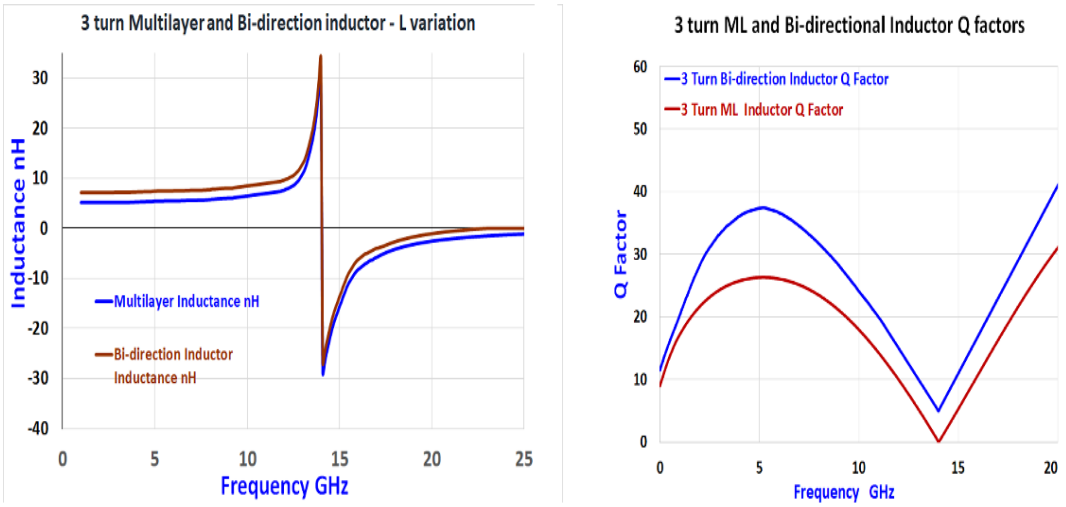


Figure 3.8 Inductance and Q value comparison of 3 turn multilayer and bi-directional inductors

The problem of nonuniform lengths for vias that connect different turns in distant layers would increase the resistive losses and influence the RF characteristics of this inductor. The RF performance of bi-directional inductor is compared with previous reported inductors and also the conventional multilayer (three) reported earlier (section 3.2.2) is given in Table 3.5.

Table 3.5 Performance comparison of bi-directional 6 layer inductor

Ref.	f_{SRF} (GHz)	L (nH)	Q_{max}	Area (mm^2)
Ref. [36]	8.6	7.8	7	0.064
Ref. [64]	9	4.61	15.8	0.0484
Ref. [3]	76	20	60	0.01
Our 3_turn Planar Inductor	9.28	4.19	19.25	0.0484
our 3_turn ML Inductor	14	5.42	26.3	0.0324
This 3_turn Bi-directional Inductor	**14.5**	**7.96**	**37.6**	**0.0144**

3.2.4 Three-layer Variable Width Inductor

Conventionally constant width planar inductors were popular due to ease of design and fabrication simplicity. But, they exhibited inferior RF performance against multilayer inductors. Research trends further improved the inductor performance by using different parametric variations. Thus the width of the conductor turns is varied uniformly inward or outward to gain superior performance [116]. It is proposed to develop a three-layer variable width ML inductor with one turn per each layer. The conductor width is chosen to decrease uniformly, while moving from outer layer to inner layers [117]. The widths of the first turn, second turn and third turns in the three layers are chosen as 12 μm, 10 μm and 8 μm. The conductor spacing is 2 μm, conductor thickness is 2 μm and the inter layer spacing is 10 μm.

Non-uniform electric field is generated due to induction effect by the eddy currents produced across the inner turns. Thus, the series resistance is increased producing losses. This proposed conductor width variation would reduce such eddy current losses, and hence lead to the quality factor enhancement [61]. Also, larger widths further increase the overall inductance of such inductors. The proposed three-layer variable width ML inductor and its HFSS implementation structure is shown in Figure 3.9.

RF performance of this proposed variable width inductor is compared with a three turn constant width ML inductor in terms of its Q value and inductance variations as shown in Fig. 3.10. It is observed that these metrics are enhanced by this variable width inductor multi layer inductor.

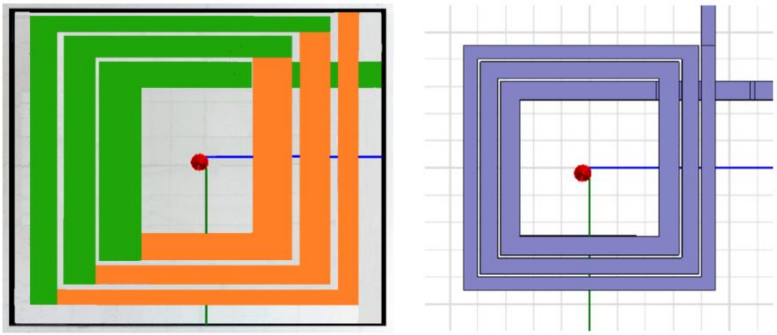


Figure 3.9. Three-layer variable width ML inductor and its HFSS structure

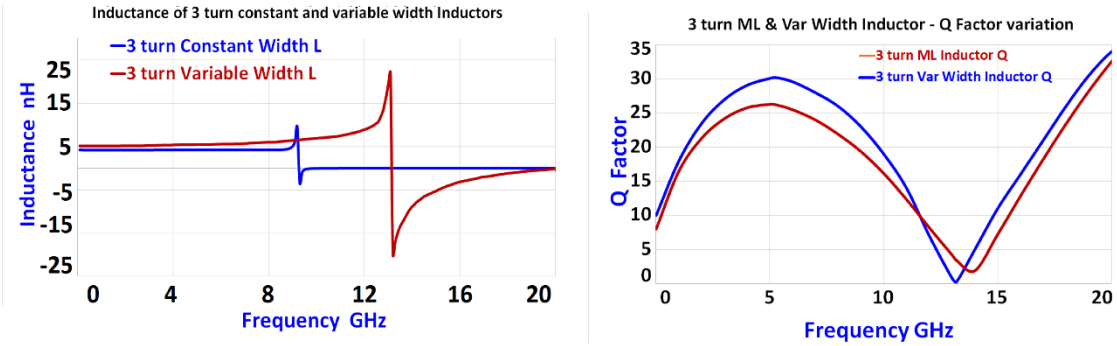


Fig. 3.10 Inductance and Q factor comparison of the three-layer constant width and variable width inductors

The RF performance of this variable width inductor is compared with previous reported inductors in the following Table 3.6.

Table 3.6 Performance comparison of the three-layer variable width ML inductor

Ref.	Width Ratio µm	f_{SRF} (GHz	L (nH)	Q_{max}	Chip Area (mm^2)
Ref. [68]	14.7_11.6_9.1	20	3.34	8.12	0.0256
Ref. [64]	40_40_40	14	4.61	19.7	1.0
Ref. [118]	20_15-10_5	12	2.4	24	0.0576
Ref. [3]	12_10_8	76	20	60	0.01
Our 3_turn Planar Inductor	8_8_8	9.28	4.19	19.25	0.0484
our 3_turn ML Const. Width Inductor	10_10_10	9.5	5.42	26.3	0.0324
This 3_turn Variable Width Inductor	**12_10_8**	**13.2**	**6.138**	**30.2**	**0.0324**

The variable width inductor exhibited an increase of 13.2472% in inductance value and 14.8289% in Q value against the constant width ML inductor for same on-chip area.

3.2.5 Parametric Analysis of proposed IPD Inductors

With technology scaling, the multilayer IPD inductors can be optimized to improve their performance. The values of the performance parameters like the inductance, Q_{max} and SRF of a ML spiral inductor are mainly influenced by its layout (geometrical) and the technology (process control) parameters. Design of spiral inductor involves finding an optimal combination of these two types of parameters to obtain the maximum possible inductance L, Q factor and SRF frequency values. These parameters are listed in following Table 3.7.

Table 3.7 Consolidated Geometrical and Process Parameters for IPD passive components

Design Parameters of on-chip IPD passive components	
Geometrical (Layout)	Conductor length (l), Conductor width (w), Conductor spacing (s), Conductor thickness (t), Number of conductor turns (n), Number of layers (N), Number of conductor paths/tracks (p), Outer diameter (D_{out}), Inner diameter (D_{in}), Substrate thickness (Tsub), On-chip area (A)
Technology (Process)	CMOS technology scale, conductor metal, Substrate material, Dielectric material,

All the on-chip IPD passive components reported in this work are designed and simulated in HFSS and SONNET EM simulators, using the standard CMOS technology 180 nm process. The CMOS process and metal stack for the 180 nm CMOS technology are shown in following Fig. 3.11. The fabrication process for proposed IPD passive inductors and capacitors are compatible with the TSMC 180 nm CMOS technology.

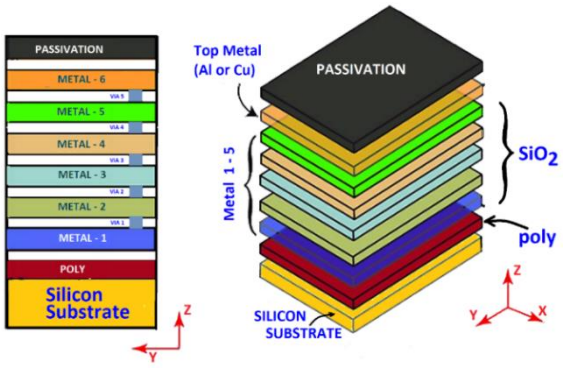


Figure 3.11. The metal stack and technology parameters for the 180 nm CMOS technology

3.2.5.1 Device Layout Parameter Analysis

Performance of the proposed multilayer IPD inductors is analysed in terms of the variation of conductor width, conductor spacing and number of turns of the device. This analysis uses the conductor widths as: 6µm, 8µm, 10µm and 12µm. The selected conductor spacings are: 1 µm, 2 µm, 3 µm and 4 µm. The selected number of turns are: 1, 2 and 3. Simulation results to study the influence of these selected device layout control parameters are shown below in Figures 3.12, 3.13 and 3.14.

From the Figure 3.12, it is observed that quality factor value increases as the conductor width increases (due to reduction in series resistance value). Also the inductance value decreases while the resonant frequency SRF increases as the conductor width is increased [60]. In this analysis the conductor spacing is fixed at 2µm and the number of turns of the device is fixed as 3.

From the Figure 3.13, it is observed that the inductance increases (due to increase in mutual inductance value) as the conductor spacing is increased. The quality factor also got increased [60]. In this analysis, conductor width is fixed at 8µm, and the number of turns of the device is fixed as 3.

From the Figure 3.14, it is observed that quality factor got decreased (parasitic capacitance between conductor turns increases) as number of turns of device increases. The overall conductor length increases with increased number of turns. This leads to the inductance enhancement [55]. In this analysis, conductor width is fixed as 10 µm and spacing between conductors is fixed as 2µm.

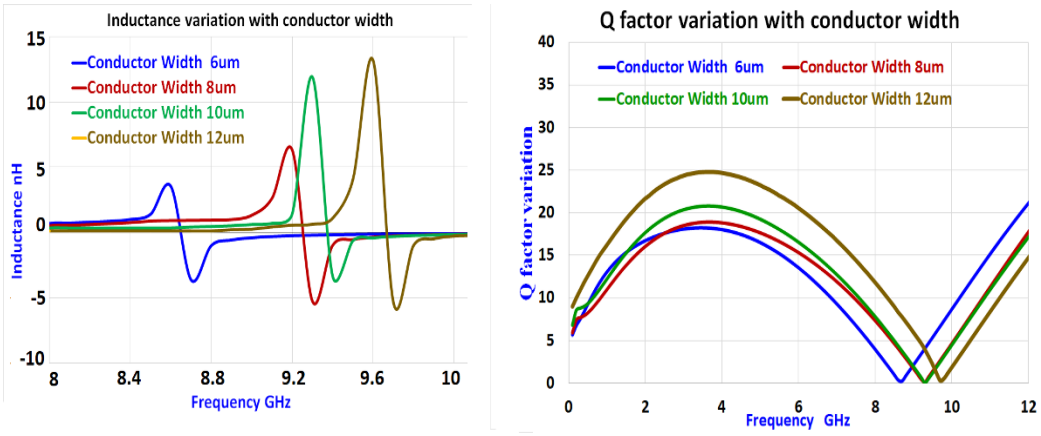


Figure 3.12 Inductance and Q factor variation with conductor width for a multilayer Inductor

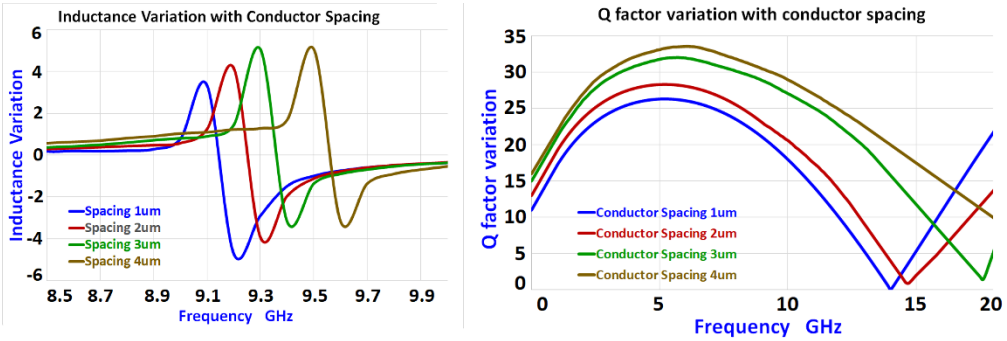


Figure 3.13 Inductance and Q factor variation of multilayer (N=3) Inductor with the conductor spacing

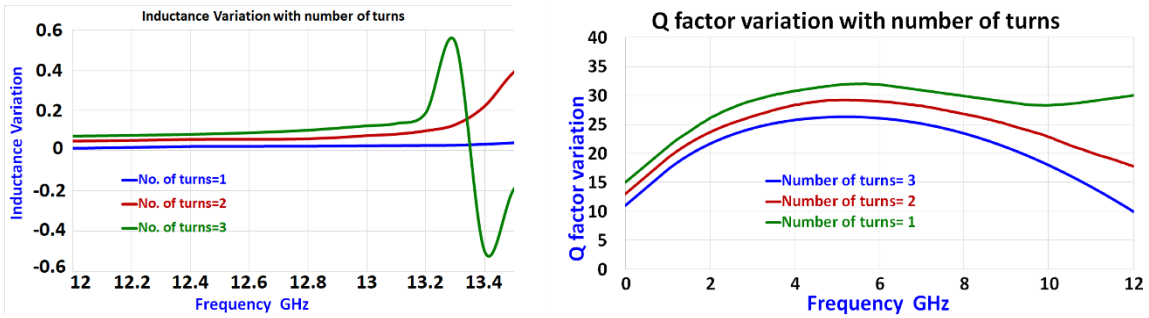


Figure 3.14 Inductance and Q factor variation of multilayer (N=3) Inductor with the number of turns

3.2.5.2 Process (Technology) Parameter Analysis

The process parameters also found to influence the performance of multilayer IPD inductors. The performance is studied by considering the substrate materials using low-K dielectric materials. The inductance and Q values of the ML inductor are analysed using different substrate material combinations. In this analysis, the dielectrics materials considered are: Modified Epoxy with $\epsilon 1$= 4.2, Quartz with $\epsilon 2$=3.8, Arlon with $\epsilon 3$=2.8. The prominently used silicon substrate has ϵSi=11.9. The combination of any two of these dielectric materials is placed in between the layers with the run of conductor placed on them [3]. Combination I is selected with Quartz glass and modified epoxy substrate materials. Combination 2 uses the Arlon and modified epoxy. The analysis finds the inductance and quality factor for the proposed multilayer IPD inductor for a typical material pair combination.

The simulation results to show the influence of selected process control parameters on inductance and Q values are shown in Figure 3.15 respectively.

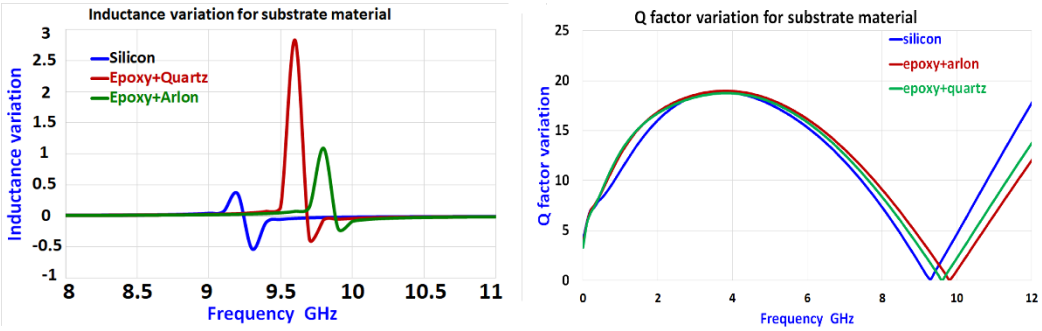


Figure 3.15 Inductance and Q factor variation of multilayer (N=3) Inductor with the substrate materials

The following conclusions are made out of this performance analysis for different geometry and process control parameters.

- Conductor width increases: Inductance, Q factor and SRF increases
- Conductor spacing increases: Inductance, Q factor and SRF increases
- Number of turns increases: Inductance increases, but Q value decreases
- Decreasing metal permittivity increases the oxide capacitance, inductor Q value, maximum Q frequency and SRF.
- Selection of thin oxide layer and thick substrate reduces the losses for on-chip passive components.

3.3 Novel Double-split IPD Inductor

Multilayer inductors became prominent due to their capability to reduce the parasitic capacitance and the induced substrate losses, since the adjacent paths possess different opposing magnetic field. This property helped them to achieve higher q factors and the SRF frequency. Recently, multi path techniques were researched to reduce the current crowding mechanism so that q factors are enhanced further [119]. Multi path mechanism experience small current crowding effect because the adjacent split conductor tracks have different opposing magnetic fields (current flows in opposite directions). This helps to reduce the opposing eddy currents yielding the increased skin depth, which reduces the series resistance (low loss also). Also the multi path structure reduces the parasitic capacitance and also the substrate loss. This produces higher Q factors and SRF for an on-chip inductor [72].

The skin effects and proximity effects dominate at higher frequencies, forcing the performance degradation for an on-chip passive device. The current flows near the skin of a

conductor, because non-uniform current flow caused by the increased magnetic field at higher frequency. This is referred to as skin effect, which depends the conductor skin depth. The skin effect decreases skin depth of a conductor and increases series resistance (Rs). A reduction in series resistance, increases the quality factor and series stacking helps to enhance the inductance for the equivalent on-chip area. The skin depth and series resistance for a given frequency (ω) are expressed as

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{3.6}$$

$$R_s = \frac{\rho l}{\omega\delta\left(1-e^{-\frac{l}{\delta}}\right)} \tag{3.7}$$

where ρ is the metal resistivity, l is the total length of inductor and μ is the free space permeability.

Finding such possibility, a novel constant width Double-split series stacked inductor is proposed as a multilayer IPD device to achieve increased impedance and high Q-factor values. The conventional single conductor run is split (partitioned) into two separated (parallel) conductor tracks (split paths) as per skin depth. Two conducting split paths have same width. Such a split path inductor is designed using a Double-splialong the entire conductor length with a spacing in between two conducting paths. Such path splitting is done in all the metal layers similarly. The inductance would increase now due to mutual coupling across two split paths. This novel IPD Double-split inductor has achieved excellent performance enhancements in terms of Inductance, SRF and high Q values compared to the standard ML inductor [116]. This proposed Double-split inductors are designed for different frequencies in the 5G spectral bands.

3.3.1 Novel Double-split inductor Structure

A novel series stacked Double-split multilayer IPD square spiral inductor is proposed, as shown in Fig. 3.16. **Novelty of proposed inductor:** conductor width of the metal layers is split into two parallel tracks in each layer from top layer to bottom layer. The spacing across conductors and different layers is uniform. These vertically stacked layers are arranged so that the divided tracks are not parallel to each other in the metal layer. This simple split spiral structure is chosen with an objective to obtain an enhanced device performance, design simplicity, ease of fabrication and minimizing the realization cost.

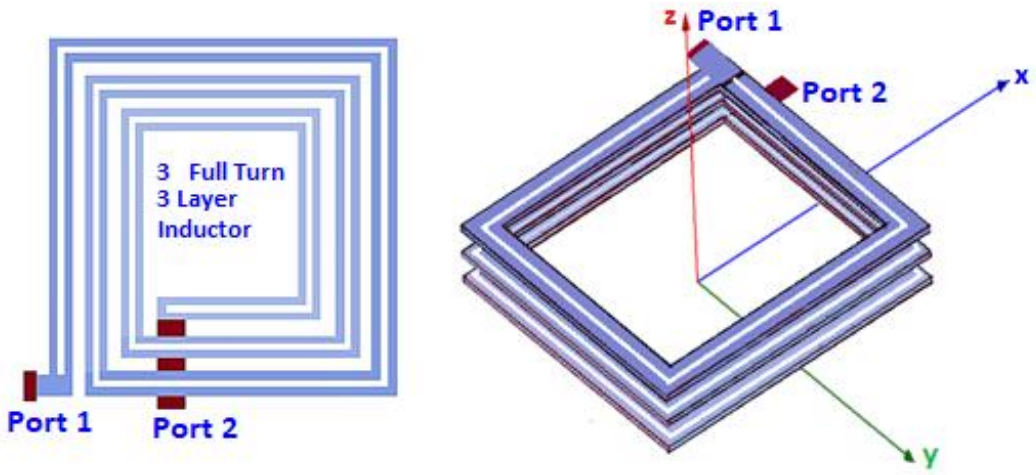


Figure 3.16 Proposed constant width series stacked Double-split multilayer IPD inductor

Such conductor path splitting doubles the conductor length. Also the two split paths are selected to have equal widths for design simplicity and ease of realizing. Variable widths also can be employed from outer turn to the innermost turns. But it increases the design difficulty and fabrication cost also. Larger widths increase the eddy current losses, which are proportional with path widths. Splitting would reduce the metal width of each track and thus further reduced series resistance and eddy current losses. Also, the hollow space of this inductor is larger than that of a standard spiral inductor. Increased hollow space reduces magnetic field penetrations into substrate and thus reduces the substrate losses. Hence, this proposed novel Double-split multilayer IPD inductor exhibits an increased Q factor, inductance and SRF values, as a result of decreased substrate loss and eddy current loss.

3.3.2 Double-split multilayer IPD Inductor at 3.5 GHz

The proposed 3.5 GHz multilayer IPD Double-split inductor runs a copper conductor on a thick Si substrate to minimize parasitic resistances to achieve an enhanced Q value. The opposite current carrying conductors are placed in different layers in order to increase the distance between conductors. This placement results in decreasing the negative mutual inductance and increasing the overall inductance. The proposed constant width Double-splithree-layer IPD inductor is designed and simulated in HFSS to obtain Q factor and the impedance [120].

Its design uses three turns (8 μm width) placed in 3 layers, which are connected by vertical vias at the end of every turn as shown in Fig. 3.17. Two conducting paths have same width, as shown. Its outer diameter is 100 μm with an occupied on-chip space of

100µm×100µm. The path spacing and widths are decided by the skin depth value of conductor material.

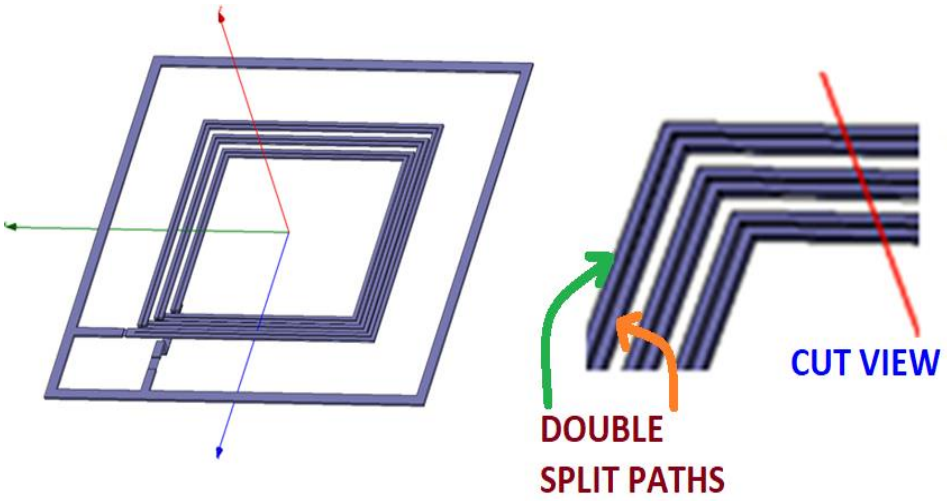


Figure 3.17 Double splitting of conductor path in each turn of a three-layer conductor

The conductor path width must be larger than the skin depth of copper, which is 1.16 µm at 3.5 GHz (from Eq.3.6). Thus, the path width is chosen as 4 µm. The total path width of 10 µm is now partitioned into two separate paths as shown in Fig. 3.17. Each track has a width of 4 µm with in between spacing of 2 µm. The dimensions of the Double-split series stacked multilayer inductor is as follows:

i) Conductor width is 4 µm.
ii) Thickness of each conductor is 2µm
iii) Spacing between two conductor tracks is 2µm
iv) Inter layer spacing is 2µm
v) Area of the inductor is 100 x 100 μm^2

The inductance, quality factor and SRF are calculated from Eq.1.5, Eq.1.7 and Eq.1.14, respectively. The HFSS simulation performance of the proposed Double-split inductor against the ML planar spiral (Fig. 3.4) and 3D inductor (Fig. 3.7) are shown in Fig. 3.18. this double-split ML IPD inductor shows an inductance enhancement of 140% over the planar ML spiral inductor and 36.5% improvement when compared with 3D spiral inductor, in the frequency range of 1 to 20 GHz. The Double-split IPD inductor exhibited 16.3% quality factor improvement over the planar ML spiral inductor and a 4.87% improvement when compared with 3D spiral inductor, due to current crowding reduction and minimizing the substrate loss.

Also observed that this novel Double-split inductor shows 54% increase in SRF over planar spiral inductor and 24.45% improvement against the 3D spiral inductor, due to reduced parasitic capacitance. Table. 3.8 gives the performance comparison for the proposed IPD inductor with proposed a planar ML inductor and 3D ML inductors.

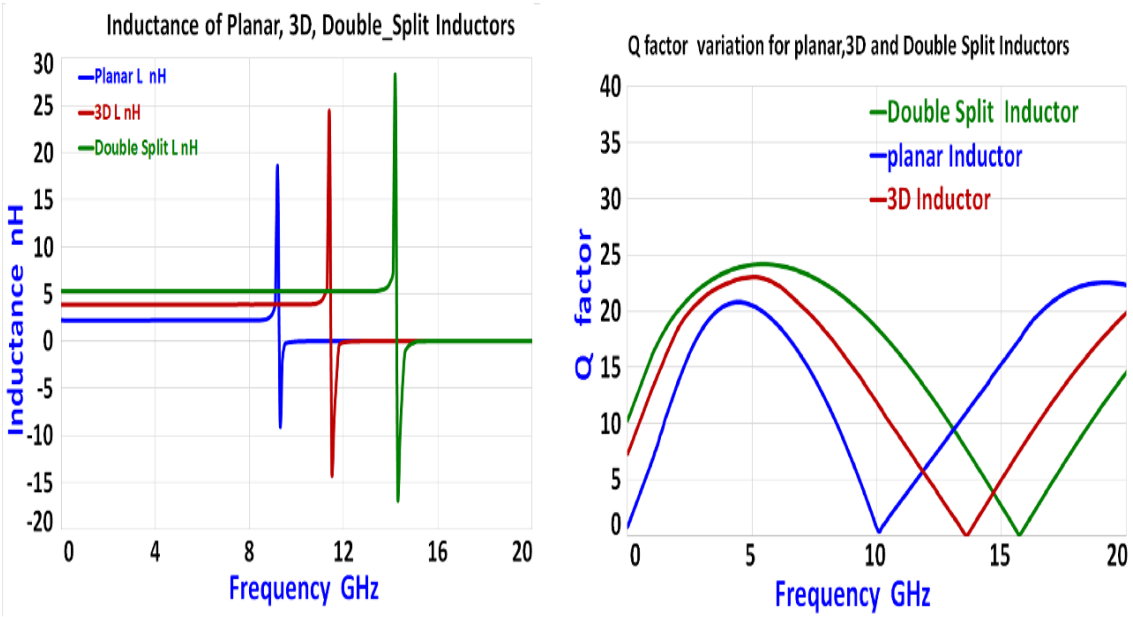


Figure 3.18 Inductance and Q factor variation for the Planar, 3D and Double-split IPD Inductors at 3.5 GHz

Table 3.8 Performance parameters of the Double-split series stacked multilayer IPD inductor

Inductor Type	Inductance (nH)	Q factor max.	SRF (GHz)	Area (µm x µm)	Width (µm)
Planar ML Inductor	2.194	20.79 at 4.5 GHz	9.25	100x100	10
3D ML Inductor	3.873	23.05 at 5.0 GHz	11.45	100x100	10
This Double-split multilayerInductor	**5.286**	**24.173 at 5.2 GHz**	**14.25**	**100x100**	**10**

Also presented here is the performance comparison of the proposed novel Double-split multilayer IPD inductor against the reported inductors cited in the references given in Table 3.9.

Table 3.9 Performance comparison for the proposed novel Double-split series stacked multilayer IPD inductor.

Inductor Type	Inductance (nH)	Q factor	SRF (GHz)	Area (µm x µm)	Width (µm)
Ref. [27]	0.133	400	50	250x250	3
Ref. [1]	5	6	2.4	200x200	6
Ref. [25]	2.5	1.5	12.5	500x500	15
Ref. [64]	1.4	19	4.1	200x200	40
Ref. [101]	5	12.5	39.5	100x100	8
Ref. [30]	3.2	400	13	200x200	30
Ref. [70]	0.1	7	70	50x50	15
This Double_Split Multilayer IPD Inductor	**5.286**	**24.173**	**14.25**	**100x100**	**10**

It is proven that the proposed double-split three-layer IPD inductor shown significant performance enhancements against the reported inductors in the reference cited in Table 3.8.

3.3.3 Double-split multilayer IPD Inductor at 5.0 GHz

The proposed Double-split multilayer IPD Inductor at 5.0 GHz uses copper conductor, thin oxide layers and a thick Si substrate and decreased metal permittivity, to reduce the parasitic capacitance and resistances. The component losses also reduce along with Q factor enhancement. Proposed inductors are designed to increase mutual inductance by splitting the conductor path width into two tracks by creating space between them. Inter layer spacing is selected properly to reduce the negative mutual inductance. The geometrical and process parameters of the inductors are optimized to result in significant inductance and Q value enhancements [120].

Its design uses three turns (8 µm width) running in each of 4 layers, which are connected by vertical vias at the end of every turn. It has an occupied chip footprint of 100µm×100µm. IPD inductor model uses a 250 µm thick Si substrate and 12 µm thin oxide layer to reduce losses and enhance the Q-factor. The total path width of 8 µm is now partitioned into two separate conductor tracks as shown in Fig. 3.19. The same path width of 3.5 µm with in between spacing of 1 µm is chosen for all the 3 turns. The dimensions of the four layer Double-split multilayer 5.0 GHz IPD inductor are as follows:

Conductor Width of split tracks : 3.5 μm

Conductor Spacing of split tracks : 1 μm

Conductor Thickness : 2 μm

Spacing between the Layers : 2 μm

On Chip Area of the Inductor : 100 x 100 μm^2

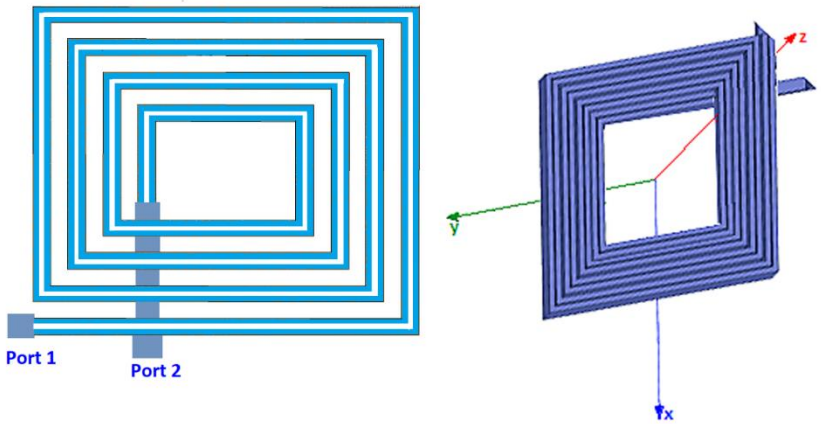


Figure 3.19 Four turn ML Double-spli5.0 GHz IPD Inductor planar view and HFSS structures

The inductance, quality factor and SRF are calculated from Eq. 1.5, Eq.1.7 and Eq.1.14, respectively. The HFSS simulation performance of the proposed Double-split inductor against the constant width ML Inductor (Fig. 3.4) are shown in Fig. 3.20.

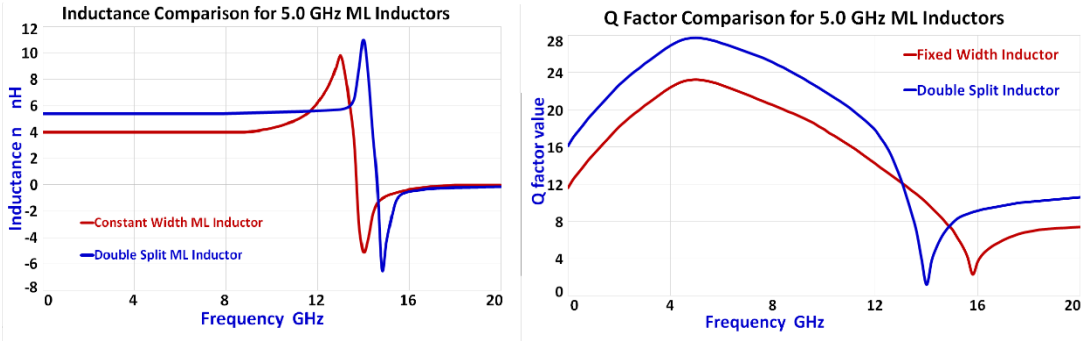


Figure 3.20 Inductance and Q factor comparison for the Constant width ML and Double-split IPD Inductors at 5.0 GHz

The inductance is 5.6 nH for the double-split IPD Inductor and 3.18 nH for the constant width ML inductor at 5.0 GHz. The SRF is 14.9 GHz. The quality factor is 27.76 for double-split IPD Inductor and 23.25 for constant width ML inductor. These results show that the double-split inductor improved the quality factor by 19.4% and inductance by 76% with respect to the constant width ML inductor. Both the inductors have equal chip area 0f 100x100 μm^2.

Table 3.10 summarizes the performance analysis of the proposed 5.0 GHz IPD inductors. It indicates that the double-split inductor has very high inductance and Q factor against the reported inductors in past literature. SRF is found to be 14.9 GHz, very much suitable for the present C band 5G location service applications.

Table 3.10 Performance comparison of the proposed novel Double-split multilayer 5.0 GHz IPD inductor.

Type of Inductor	Center Frequency f_0 GHz	Inductance nH	Quality Factor Q	SRF fR GHz	On chip area mm^2
Ref. [1]	5.0	4.9	5.8		---
Ref. [68]	5.2	3.46	7.09		---
Ref. [13]	5.0	10	15.12		---
Ref. [32]	5.0	3.23	9		---
Ref. [88]	5.0	0.4	22.7		---
constant width IPD inductor	5.0	3.18	23.25	13.6	0.0324
This Double-split IPD Inductor	**5.0**	**5.6**	**27.76**	**14.9**	**0.01**

3.3.4 Double-split multilayer IPD Inductor at 5.1 GHz

The proposed 5.1 GHz multilayer IPD Double-split inductor uses copper conductor, thin oxide layers and a thick Si substrate and decreased metal permittivity, to reduce the parasitic capacitance and series resistance. This also leads to reduced component losses along with enhanced inductor Q value. The mutual inductance is decided with the space between the tracks. The mutual inductance increases with the decreased space between the tracks, thereby enhancing overall inductance.

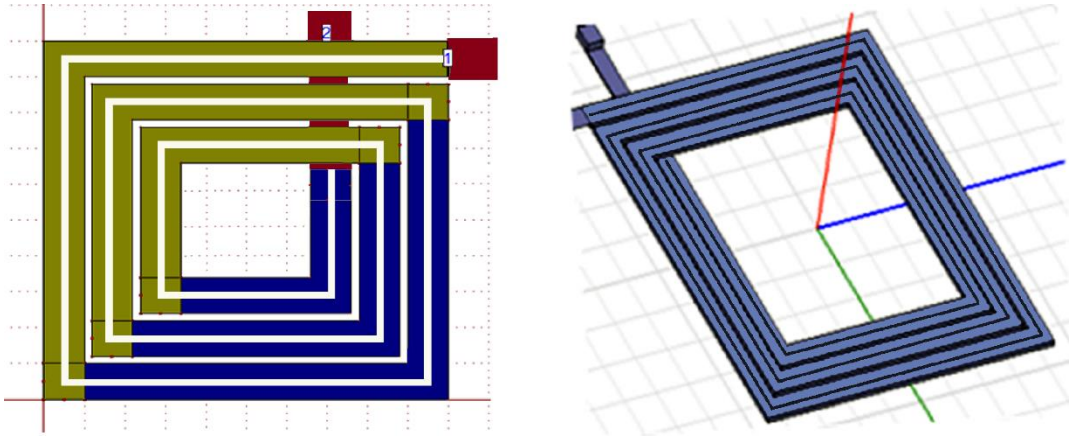


Figure 3.21 Three turn ML Double-spli5.1 GHz IPD Inductor planar view and HFSS structures

All the turns use equal conductor width. Inter layer spacing is selected to reduce the negative mutual inductance. The path width is chosen as 4.5 μm. The total path width of 10 μm is now partitioned into two separate paths as shown in Fig. 3.21. Each track has a width of 4.5 μm with in between spacing of 1 μm.

The dimensions of the double-split multilayer 5.1 GHz IPD inductor are as follows:

Conductor Width of split tracks : 4.5 μm

Conductor Spacing of split tracks : 1 μm

Conductor Thickness : 1 μm

Spacing between the Layers : 1 μm

On Chip Area of the Inductor : 160 x 160 μm^2

The inductance, quality factor and SRF are calculated from Eq.1.5, Eq.1.7 and Eq.1.14, respectively. The HFSS simulation performance of the proposed 5.1 GHz Double-split inductor against the ML planar spiral (Fig. 3.4) is shown in Fig. 3.22.

Inductance is 6.75 nH for this double-split inductor and 5.6 nH for square inductor at 5.1 GHz. The SRF is 13.5 GHz. The Q value is 16.177 for square spiral inductor and 24.173 for this double-split inductor. These results, show that the Double-split inductor has quality factor enhanced by 1.48 times than square spiral inductor. Similarly, this split inductor improved inductance by 1.21 times than square spiral inductor. Both these inductors have

equal chip space of 140x140 sq. µm. Table 3.11 gives the performance comparison for proposed 5.1 GHz IPD inductors.

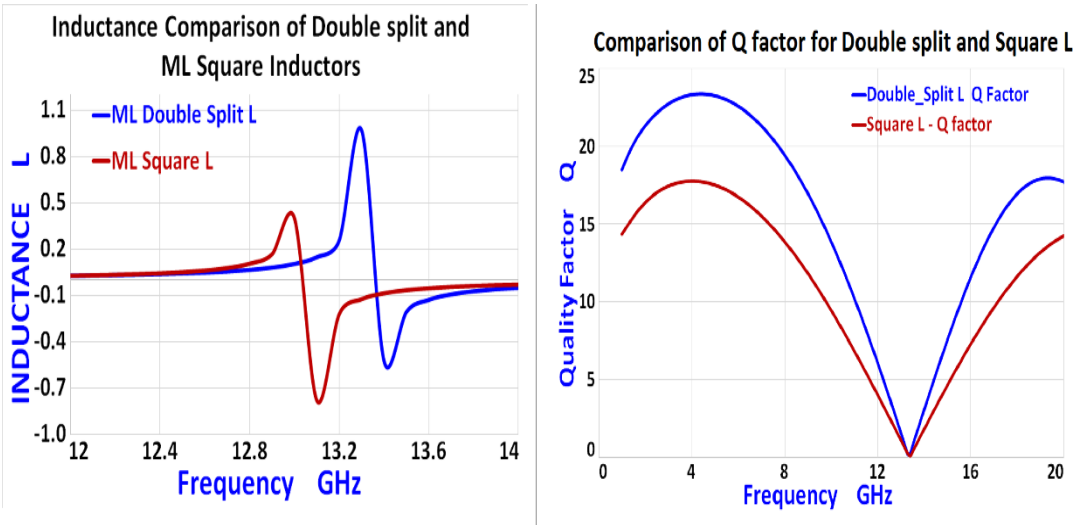


Figure 3.22 Inductance and quality factor variation of double-split IPD inductor and comparison with the ML square spiral inductor at 5.1 GHz

Table 3.11 Performance comparison of the proposed novel Double-spliML 5.1 GHz IPD inductor.

Inductor Type	Inductance (nH)	Q factor	SRF (GHz)	Area (µm x µm)	Width (µm)
Ref. [17]	5	6	2.4	200x200	6
Ref. [101]	2.5	1.5	12.5	500x500	15
Ref. [121]	1.4	19	4.1	200x200	40
Square Spiral IPD L	5.6	16.177	11.5	160x160	10
This Double_Split Multilayer IPD Inductor	**6.75**	**24.173**	**13.5**	**140x140**	**10**

3.3.5 Double-split multilayer IPD Inductor at 5.25 GHz

The proposed 5.25 GHz multilayer IPD Double-split inductor uses copper conductor, thin oxide layers and a thick Si substrate and decreased metal permittivity, to minimize the parasitic capacitance and resistance. This also leads to reduced component losses along with enhanced inductor Q value. The mutual inductance varies with the space in between the tracks. The spacing between the split paths is chosen small enough to increase the mutual inductance, thereby improving overall inductance.

The path width is chosen as 4.5 µm. The total path width of 10 µm is now partitioned into two separate paths as shown in Fig. 3.23. Each track has a width of 4.5 µm with in between spacing of 1 µm.

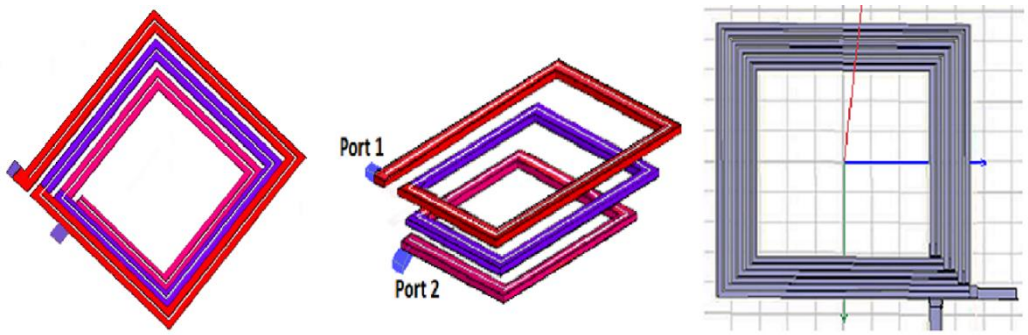


Figure 3.23 Three turn ML Double_Spli5.25 GHz IPD inductor planar, 3D, and HFSS structures

The dimensions of the Double-split multilayer 5.1 GHz IPD inductor are as follows:

Conductor Width of split tracks : 3.25 µm

Conductor Spacing of split tracks : 1.5 µm

Conductor Thickness : 1 µm

Spacing between the Layers : 1 µm

On Chip Area of the Inductor : 100 x 100 μm^2

The HFSS simulation performance of the proposed Double-split inductor against the constant width and variable width ML inductors is shown in Fig. 3.24.

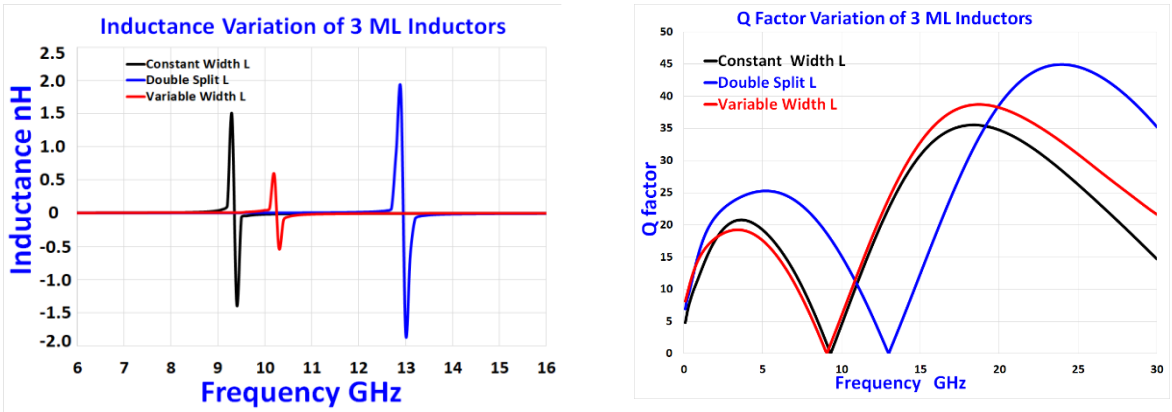


Figure 3.24 Inductance and Q factor variation and comparison for ML constant width, Double-spliand variable width IPD Inductors at 5.25 GHz.

The value of inductances for the Double-split IPD, variable width ML and constant width ML inductors are 5.458 nH, 4.052 nH and 3.891 nH correspondingly at 5.25 GHz. The SRF is 13.5 GHz. The quality factor for 2-split (Double-Split), variable width and constant width ML inductors are 23.858, 20.8516 and 19.2577 respectively. This Double-split inductor had increased the quality factor by 31.652% and the inductance by 40.27% against the constant width ML inductor. Both these inductors have equal chip area of 180x180 sq. µm. Similarly, Double-split IPD inductor had increased the inductance and quality factor by 34.7% and 21.59% respectively, against the variable width ML inductor. Table 3.12 presents the performance comparison of the proposed novel Double-split multilayer 5.25 GHz IPD inductor.

Table 3.12 Performance comparison of the proposed novel Double-split multilayer 5.25 GHz IPD inductor.

Inductor	Conductor Width, µm	Spacing µm	Thickness µm	Number of Turns	L, nH @ 5.25GHz	Q_{max}	Area, μm^2
Ref. [122]	15_15_15	1.5	2	3	2.5	1.5	500x500
Constant Width L	10_10_10	2	2	3	3.891	19.26	180x180
Variable Width L	10_12_14	2	2	3	4.052	20.85	180x180
Double Split L	**3.25_1.5_3.25**	**2**	**1**	**3**	**5.458**	**25.35**	**100x100**

These results have indicated that the three inductors designed here, will surely meet the requirements of 5G lower band (sub-6GHz) requirements as they possess higher Q values and minimal occupied chip space.

3.3.6 Double-split multilayer IPD Inductor at 8.0 GHz

The proposed 8.0 GHz multilayer IPD Double-split inductor uses copper conductor, thin oxide layers and a thick Si substrate to minimize the parasitic capacitance and resistance. This leads to reduced losses along with enhanced Q value. Smaller spacing is chosen between the split paths to increase the mutual inductance, which increases total inductance. The path width is chosen as 3.5 µm. The total path width of 9 µm is now partitioned into two separate paths as shown in Fig. 3.25. Each track has a width of 3.5 µm with in between spacing of 2 µm. The

layer spacing is 2μm and total area is 100 x 100 μm^2. The split path ML IPD inductor has one full split conductor turn per each layer.

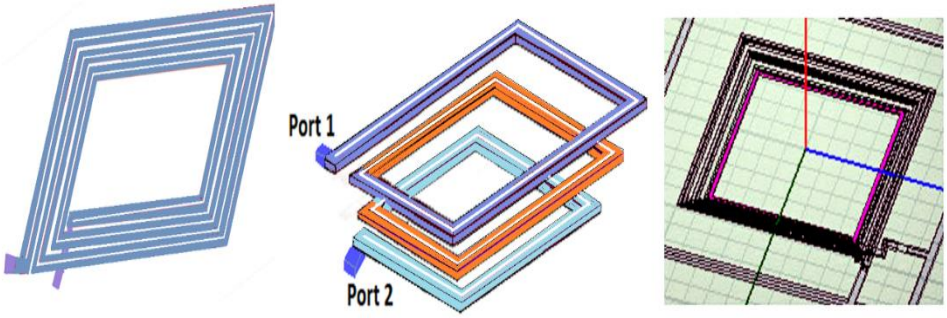


Figure 3.25 Three turn ML Double-spli8.0 GHz IPD inductor planar, 3D, and HFSS structures

HFSS simulation results of the proposed 8.0 GHz Double-split IPD inductor showing the inductance and quality factor (Q) variation are plotted in Figure 3.26.

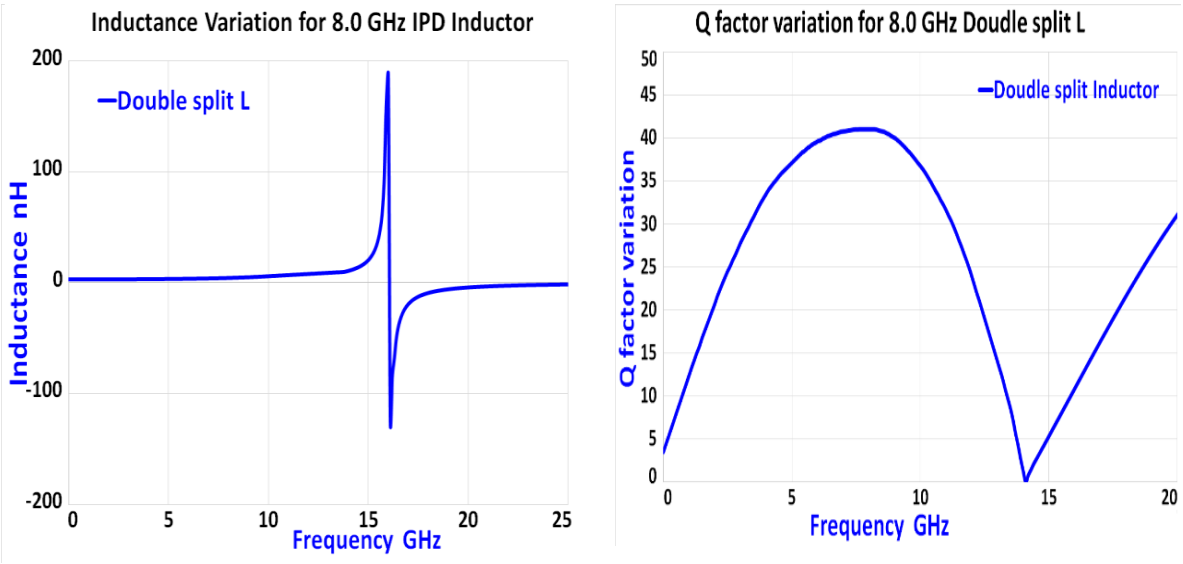


Figure 3.26 Inductance and Q factor variation of multilayer Double-spli8.0 GHz IPD Inductor

The simulated performance of this Double-split multilayer 8.0 GHz IPD inductor using 0.18 μm CMOS technology produced higher Q value of 41 and increased SRF of 14.2 GHz. Hence this split path inductor is suitable 8 GHz UWB and 5G RFIC applications chiefly due to its minimum on-chip space. Table 1 compares the simulation results of proposed 8.0 GHz IPD inductor with the similar on-chip inductors in literature cited.

Table 3.13 Performance comparison of the proposed novel Double-split multilayer 8.0 GHz IPD inductor.

Inductor	Conductor Width, μm	Spacing μm	Thickness μm	Number of Turns	L nH	Q_{max}	SRF GHz	Area, mm^2
Ref. [123]	15_15_15	1.5	2	3	0.35	1.5	9.0	1.68
Ref. [109]	10_10_10	2	2	3	1.623	30	8.36	0.35
Ref. [45]	10_12_14	2	2	3	0.43	5.5	12.5	0.056
Proposed 8.0 GHz IPD L	**3.25_1.5_3.25**	**2**	**1**	**3**	**3.5**	**41**	**14.1**	**0.01**

From above results, it is observed that the 8.0 GHz Double-split IPD inductor had increased the quality factor by 36.67% than the 7.6 GHz IPD inductor. Proposed double-split inductor had improved the inductance by 115.65% than the 7.6 GHz IPD inductor. Also the chip space of Double-split IPD inductor is 35 times smaller than that of the 7.6 GHz IPD inductor. Similarly, Double-split IPD inductor had increased the inductance and quality factor by 713% and 12.8% respectively, against the CMOS inductor.

3.3.7 Double-split multilayer IPD Inductor at 25.0 GHz

The proposed 25.0 GHz multilayer IPD Double-split inductor uses copper conductor, thin oxide layers and a thick Si substrate and smaller metal permittivity, to minimize the parasitic capacitance and resistance. This also leads to reduced component losses along with enhanced inductor Q value. The selection of smaller spacing enhances the overall inductance. The path width is chosen as 3.5 μm. The total path width of 10 μm is now partitioned into two separate paths as shown in Fig. 3.27. Each track has a width of 3.5 μm with in between spacing of 3 μm. The layer spacing is 2μm with total chip area of inductor is 100 x 100 μm^2. The split path ML IPD inductor has one full split conductor turn per each layer.

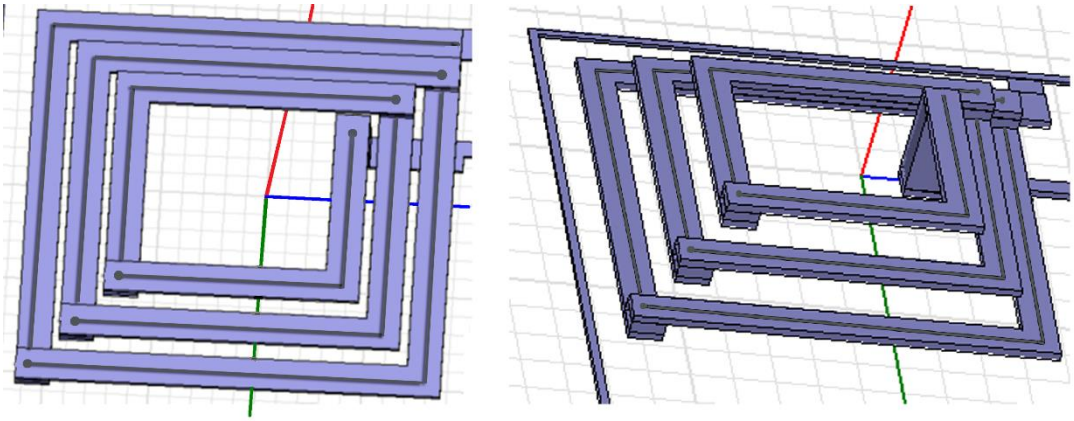


Figure 3.27 Three turn ML Double-spli25.0 GHz IPD inductor planar and 3D HFSS structures

HFSS simulation results of proposed ML Double_Spli25.0 GHz IPD inductor showing the inductance and Q factor variation with frequency are plotted in Figure 3.28.

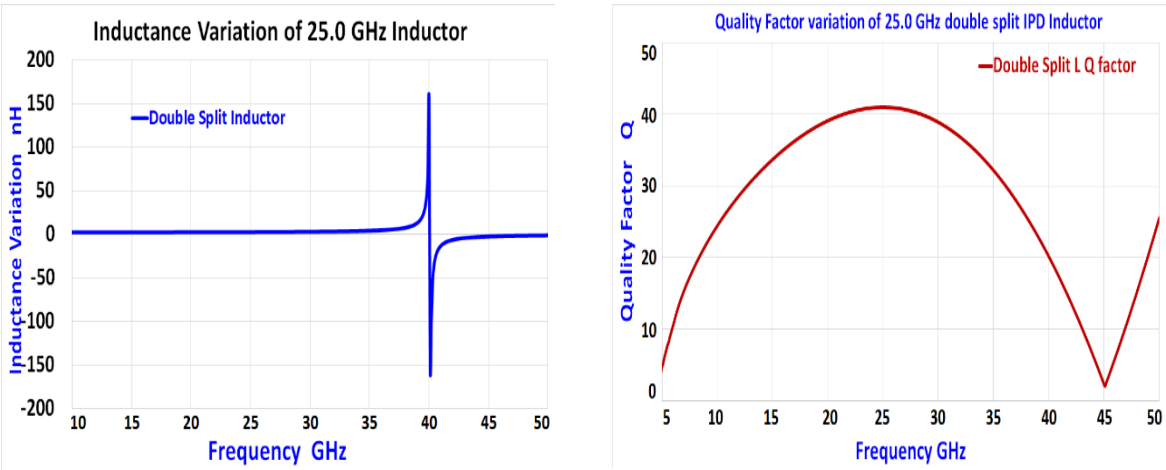


Figure 3.28 Inductance and Q factor variation of multilayer Double-spli25.0 GHz IPD Inductor

The simulated performance of this Double-split multilayer 25.0 GHz IPD inductor on 0.18 µm CMOS technology resulted with a higher Q value of 41.86 and an SRF of 40 GHz. Hence, this novel split inductor is highly suitable for 5G high band 25-30 GHz RFIC applications primarily due to its minimum on-chip space. Table 1 compares the simulation results of proposed 25.0 GHz IPD inductor with the similar on-chip inductors in literature cited.

Table 3.14 Performance comparison of the proposed novel Double-split multilayer 25.0 GHz IPD inductor.

Inductor	Conductor Width, µm	Spacing µm	Thickness µm	Number of layers	L nH	Q_{max} @25 GHz	SRF GHz	Area, mm^2
Ref. [3]	8	2	2	4.5	3.6	18	65	0.01
Ref. [32]	10	2	3	2	3.23	12.3	40	0.04
Ref. [124]	6	5	3	1	1.1	21.1	35	0.1
Proposed Double-spli5.0 GHz IPD	**3.5_3_3.5**	**2**	**2**	**3**	**2.86**	**41.86**	**40**	**0.01**

It is observed that the proposed 25.0 GHz Double-split IPD inductor had increased the quality factor by 98.38% than the single layer 25 GHz IPD inductor. The inductance is also improved by 160%. This Double-split IPD inductor occupied 10 times smaller chip space than single layer 25 GHz IPD inductor. Similarly, this inductor increased the Q factor by 240% and decreased the area by 300% respectively, against the Differential fractal inductor. Thus the proposed Double-split IPD inductor is highly suits 5G high band (Ka) communications.

3.3.8 Parametric Analysis of the proposed IPD Inductors

This research work on the miniature on-chip passive components for 5G applications implemented several IPD passive inductors as illustrated in sections 3.2 and 3.3. Different combinations of the layout parameters and process parameters were carefully studied to determine their high frequency influence on the proposed IPD inductors. The design involves finding the optimal combination of these parameters to obtain maximum possible inductance L, Q factor and SRF frequency values. Mainly the on-chip IPD planar and multilayer inductors were implemented at 5G frequencies of 3.5 GHz, 5.0 GHz, 5.1 GHz, 5.25 GHz, 8.2 GHz and 25.0 GHz. Their layout parameters and electrical performance are presented in Table 3.14.

These results have clearly established the superior performance of the proposed novel Double-split multilayer IPD inductor for different 5G frequencies, with highly enhanced inductance, quality factor and SRF values. A particular combination will optimize one or two design parameters at the cost of others, as observed from above results. Also the occupied on-

chip area is significantly reduced to realize highly compact miniature on-chip passives for 5G RFIC applications. Hence, the chief objective of miniaturizing the components has been successfully achieved apart from the performance enhancements by careful interplay between the device layout parameters and CMOS technology process parameters.

Table 3.15 The layout parameters and electrical performance of proposed IPD Inductors

Inductor type	No. of Turns, Layers	Conductor Width, μm	Spacing, Thickness μm	L nH	Qmax	f_{Qmax}	SRF	Area mm^2
Planar	3/1	8	2_2	4.195	15.8	3.6	9.28	0.048
constant width	1/3	10	2_2	5.42	26.3	5.1	14	0.0324
Bi-Directional	3/6	8	2_2	7.96	37.6	5.2	14.5	0.0144
Variable width	1/3	12_10_8	2_2	6.138	30.2	5.25	13.2	0.0324
Double-spli3.5 GHz	1/3	4_2_4	2_2	5.286	24.173	5.2	14.25	0.01
Double-spli5.0 GHz	1/3	3.5_1_3.5	2_2	5.6	27.76	4.90	15.4	0.01
Double-spli5.1 GHz	1/3	4.5_1_4.5	1_1	6.75	24.173	4.95	13.5	0.0196
Double-spli5.25 GHz	1/3	3.25_1.5_3.25	2_2	5.458	25.35	5.0	13.55	0.01
Double-spli8.0 GHz	1/3	4_2_4	2_2	3.5	41	8.1	14.1	0.01
Double-spli25.0 GHz	1/3	4_2_4	2_2	2.86	43	24.9	40	0.01

3.4 Planar and Multilayer IPD Spiral Capacitor

Capacitor is a very crucial passive component in electronic circuits and RF wireless communications. Capacitors are mostly employed in oscillators, tuned resonators, impedance matching networks, filters, tuned amplifiers, storage devices, sensors and dc blocking circuits. Miniaturized (size shrinking) capacitors are mostly sought to minimize the occupied die space for 5G RFICs. The IPD technology permits such size and weight reductions for successful integration of the high performance on-chip passives in a single Si CMOS chip. Happy

integration of low-cost CMOS process and miniature IPD technologies permit today, the global availability of small sized mobile devices and terminals. The modeling and design of low leakage and high-performance CMOS capacitors is still a challenging task in RFIC fabrication. Section 1.4.2 had illustrated the fundamental characteristics and generic structures of several state of art on-chip capacitors reported in literature.

The on-chip capacitor performance is measured by the capacitance per unit area, break down voltage, linearity and quality factor. At 5G frequencies, it is difficult to measure voltage and current as the signals act like traveling EM waves. At radio frequencies, the scattering or S-parameters represent the capacitor behavior, like that of an on-chip inductor [125]. Thus, device capacitance and Q factor values are calculated from S-parameters obtained from an EM simulator or a network analyzer. These S-parameters are converted to Y- parameters to calculate the capacitance value using Eq. 1.8 and Eq.1.9.

Typical performance for a Si spiral capacitor is judged by plotting its quality factor and its capacitance plots, which were shown in Fig. 1.14. The frequency at which the Q value is equal to zero, is the SRF (f_{SRF}) of the capacitor. The capacitive linear region generally exists up to three fourths (3/4) of the SRF value. In its nonlinear region, susceptance rapidly jumps up and drops down drastically near SRF value.

3.4.1 Planar Three Turn Spiral IPD Capacitor

Planar square spiral structures are simple to design and easy to fabricate to help on-chip passive component miniaturization. Large capacitance single or multilayer capacitors are easily designed and simulated in HFSS, by setting the CMOS process parameters of metal, dielectric and substrate layers. IPD process employs a high resistivity substrate for high quality passive capacitors. Several past designs were proposed to utilize the lateral fringe fields to obtain higher capacitance density. Planar capacitors are developed using a square spiral as the first metal turn, with the second trace formed in between the spiral loops of the first trace. Dielectric area separates these two spiral traces. Dielectric layer separates the metal turns (traces) in all directions. Metal turn spacing shall be minimized to increase the capacitance per unit area. Since the two spiral turns are orthogonal, the series resistance and the inductance get significantly reduced. The 2D geometrical layout and the HFSS structure of the proposed three turn planar (single layer) capacitor are shown in Figure 3.29. Its lumped element π-equivalent circuit model is shown in Fig. 3.30.

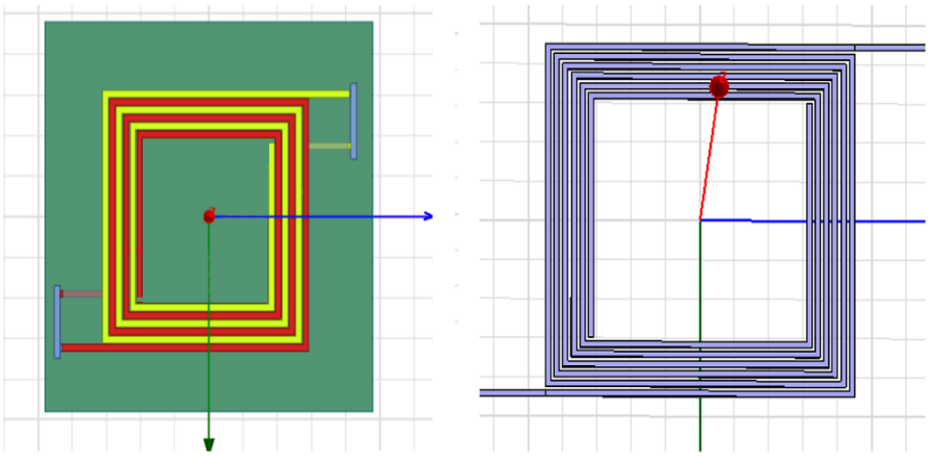


Figure 3.29. Single Layer three turn IPD capacitor Planar and HFSS Layouts

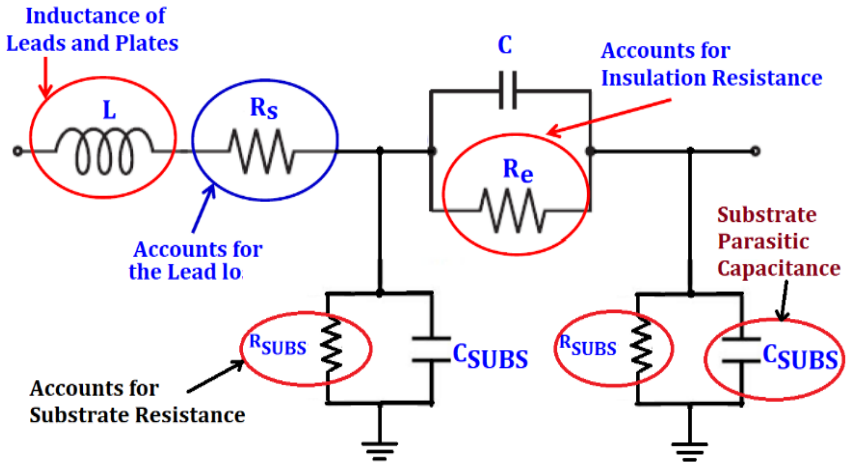
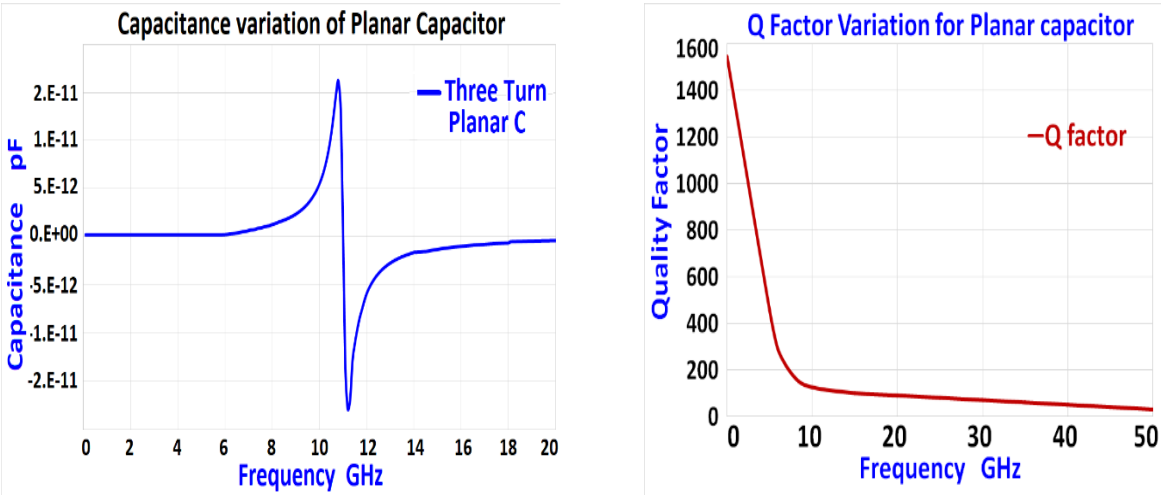


Figure 3.30 three turn planar spiral capacitor lumped element π-equivalent circuit model

The quality factor and capacitance for the three turn single layer planar spiral capacitor are calculated from Eq.1.8 and Eq.1.9. This proposed capacitor has an outer diameter of 50 µm. The conductor width is 5 µm with turn spacing of 1 µm. The on-chip area is 0.025 mm^2. The substrate thickness is chosen as 250 µm to reduce the parasitic effects. The HFSS simulation results of the proposed three-layer planar IPD capacitor showing its capacitance and quality factor (Q) variation with frequency are plotted in Figure 3.31.

The simulated performance of this proposed three turn planar IPD spiral capacitor modelled on 0.18 µm RF CMOS technology produced a higher Q value of 455 at 5.0 GHz. Its capacitance value is 0.226 pF in the operating frequency range of 0.1 to 6 GHz. Its self-resonance frequency is 11 GHz. Hence this planar IPD capacitor is highly suitable for 5G sub-6 GHz RFIC applications primarily due to its minimum on-chip space of 0.025 mm^2. This improved quality factor stems from the placement of entire metal trace in the top layers.

Therefore the substrate parasitic effects are significantly reduced as the electric flux lines terminate in adjacent metal traces in top layer far away from substrate. Table 3.15 compares the simulation results of proposed three turn planar IPD spiral capacitor with the similar on-chip capacitors cited in past literature. This proposed on-chip planar IPD capacitor satisfied the performance metrics like higher capacitance, higher Q value, linearity, high SRF and smaller chip space.



(a) (b)

Figure 3.31 (a) Capacitance (b) Q factor variation of three turn planar IPD spiral capacitor

Table 3.16 Performance comparison of the proposed three turn planar IPD spiral capacitor

Capacitor	Capacitance pF	Quality Factor Q	SRF GHz	Conductor width μm	Area mm^2
Ref. [112]	0.5	4	20	-	-
Ref. [103]	2.5	4	4	-	-
Ref. [126]	1.9	16	11	-	-
Ref. [127]	0.54	200	10	-	-
Ref. [41]	0.64	250	12	8	0.04
Proposed Planar IPD	**1.126**	**455**	**11**	**5**	**0.025**

It is observed that the proposed three turn planar IPD spiral capacitor had increased the Q factor and capacitance values by 82%% and 76% than the single layer fractal spiral capacitor.

Also, the chip space of planar IPD spiral capacitor is 60% smaller than that of the single layer fractal spiral capacitor. Similarly, planar IPD spiral capacitor had increased the quality factor and capacitance is increased by 127% and 138% respectively, against the conventional spiral capacitor. Thus, the proposed planar IPD spiral capacitor is a best suitable candidate for 5G sub-6GHz communications.

3.4.2 Multilayer (Two Layer) Spiral IPD Capacitor

Multilayer inductors achieved greater success in high frequency performance using IPD technology. A multilayer capacitor can increase the capacitance density per unit chip area. Multiple metal trace layers enabled the loss reduction. Like the conventional capacitors, silicon is used for substrate while copper is the conductor. Thickness of the lossy silicon substrate is selected high enough to reduce the losses for further enhancement of Q. High conductivity copper metal reduce the coupling losses so that capacitance is enhanced.

The design of multilayer capacitors is very similar to that of multilayer inductors. One can develop parallel metal paths by placing the conductor half turns in two adjacent layers, connected by vias. The constant conductor width is proposed. The spacing across vertical layers is selected, to increase the net capacitance value [4]. The design and performance simulation is performed in HFSS. The HFSS simulated planar 2D layout, HFSS 2D and 3D views of the proposed single turn multilayer (two) IPD capacitor are shown in Figure 3.32.

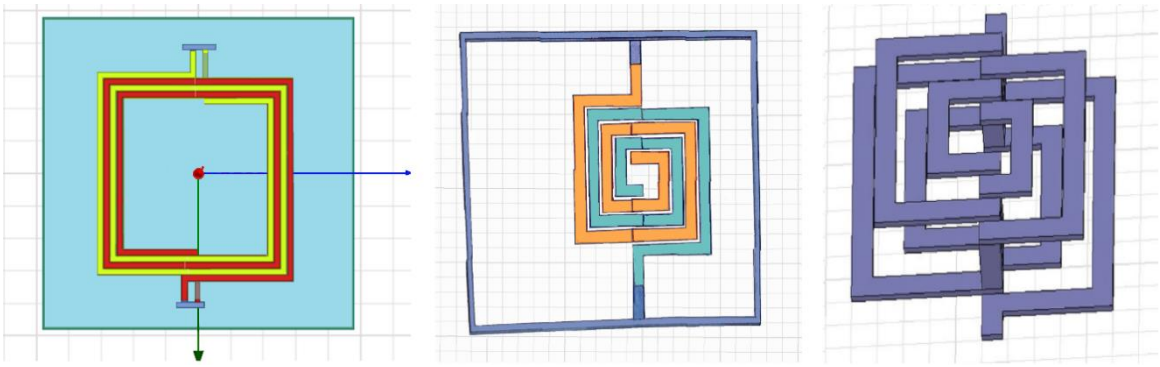
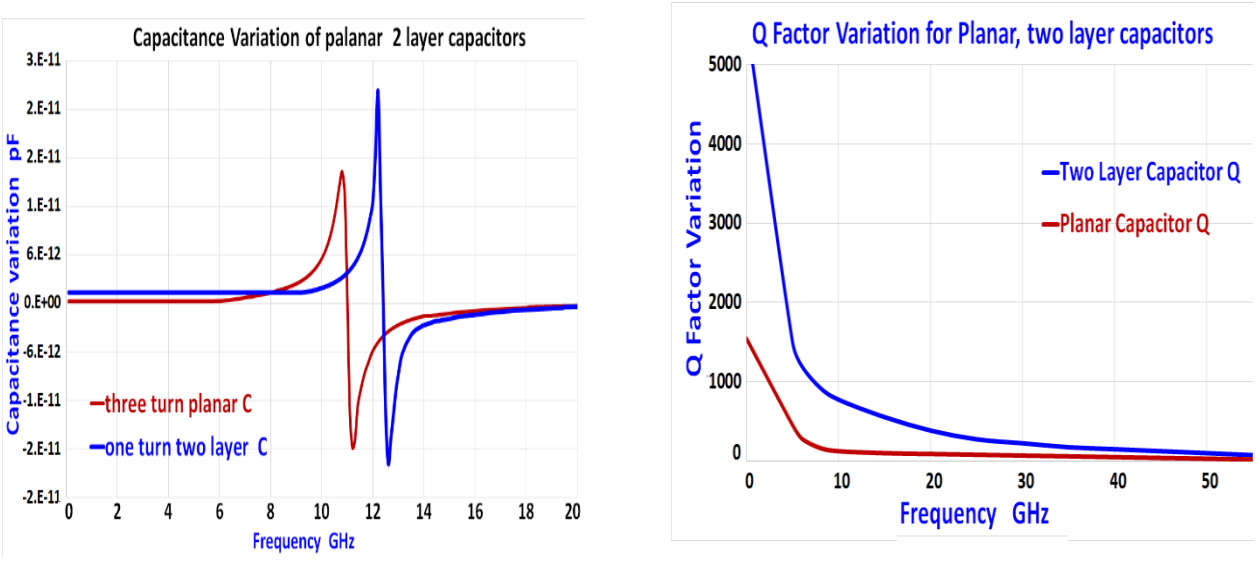


Figure 3.32. Two Layer one turn IPD capacitor planar, HFSS and 3D views

It shows two non-overlapping rectangular single port conductor traces run in different layers to form the capacitor structure. Two different colours are used to distinct the adjacent conductor runs in every metal layer. The alternate conductor runs are cross coupled to make the overall capacitance equal to the sum of metal layer vertical flux and the lateral flux of the

edges in between two metal traces in every layer as shown in Fig. 3.47. This arrangement increases the capacitance density due to lateral flux and reduces the parasitic capacitance of the bottom plate. Such cross-coupling mechanism can be extended to the bottom layers further, to increase the capacitance density.

This proposed capacitor has outer diameter of 50 µm. The conductor width is 4 µm with turn spacing of 1 µm. The spacing between two layers is 10 µm. The on-chip area is 0.025 mm^2. The substrate thickness is chosen as 250 µm to reduce the parasitic effects. The HFSS simulation results of the proposed two-layer IPD capacitor showing the capacitance and quality factor (Q) variation with frequency are plotted in Figure 3.33.



(a) (b)

Figure 3.33 (a) Capacitance (b) Q factor variation of planar and two layer IPD spiral capacitors

The simulated performance of proposed two-layer one turn IPD spiral capacitor based on the 0.18 µm CMOS process produced significantly high Q value of 1500 at 5.0 GHz. Its capacitance value is 1.3 pF in the operating frequency range of 0.1 to 6 GHz. Its self-resonance frequency is 12.5 GHz. Hence this planar IPD is suitable for 5G sub-6 GHz RFIC applications primarily due to its minimum on-chip space of 0.025 mm^2. Table 3.16 compares the simulation results of proposed two-layer IPD spiral capacitor with the similar on-chip capacitors cited in past literature. This proposed on-chip planar IPD capacitor had satisfied the performance metrics like higher capacitance, higher Q value, linearity, high SRF and smaller chip space.

Table 3.17 Performance comparison of the proposed two-layer one turn IPD spiral capacitor

Ref., From Nagesh, Akhendra	Capacitance pF	Quality Factor Q At 5 GHz	SRF GHz	Conductor width μm	Area mm^2
Ref. [112]	0.5	4	20	-	-
Ref. [103]	2.5	4	4	-	-
Ref. [126]	1.9	16	11	-	-
Ref. [127]	0.54	200	10	-	-
Ref. [41]	0.64	250	12	8	0.04
Ref. [101]	0.08	1200	100	4	0.025
Proposed Planar IPD Capacitor	1.126	455	11	5	0.025
Proposed Two Layer IPD capacitor	**1.3**	**1500**	**12.5**	**4**	**0.025**

It is observed that the proposed two layer single turn IPD spiral capacitor had increased the quality factor and capacitance by 229.7% and 15.5% respectively, against single layer planar IPD spiral capacitor. Both have equal chip space. Similarly, proposed two layer single turn IPD spiral capacitor had increased the quality factor and capacitance is increased by 25% and 138% respectively, against the two layer spiral capacitor. Thus the proposed two layer IPD spiral capacitor is a best suitable on-chip capacitor for the 5G sub-6GHz communications.

3.5 Summary

Spectacular progress in telecom research and rapid breakthroughs in VLSI technology led to the massive global proliferation of 5G networks provide a multitude of smart mobile services much to the joy of information hungry society today. The major building blocks of such 5G radio transceivers are optimally designed with high performance circuits like RFICs. Recently developed IPD technology is successfully integrating with low-cost CMOS device technology to provide small size and light weight mobile devices and terminals.

Still, the on-chip passive components occupy more than 60% of the chip space. Therefore heavy research is focused on design and development of highly miniaturized IPD passives yet possessing very good high frequency performance to meet stringent 5G service demands at affordable tariffs. Multilayer passives are popular choice for researchers as they exhibited good performance at 5G frequencies.

Hence, this work proposed the design and development of two key on-chip circuit performance deciders: passive inductor and capacitor. The optimal combination of the device layout parameters and the process control parameters is derived to design and simulate different multilayer on-chip passives using spiral structure. The simulation results had shown high performances at a selected 5G band, along with reduced on-chip area. A novel Double-split series stacked multilayer IPD inductor is proposed to further enhance the high frequency performance for minimal on-chip area occupied. These inductors are developed at 3.5, 5.0, 5.1, 5.25, 8.2 and 25 GHz for 5G applications. Also, planar and multilayer passive IPD spiral capacitors also are designed and implemented successfully with enhanced performance.

Chapter 4

Mathematical Extraction of Inductance

4.1 Introduction

Inductance extraction is a crucial step and plays a vital role in successful validation of different types of on-chip passive inductor structures. Simple approximate expressions to calculate the inductance for on-chip spiral inductors with different geometries were derived in the past using Greenhouse formulations, modified Wheeler formula, Current sheet approximation, Integral field solution, partial equivalent electrical circuit (PEEC) and data fitting algorithm methods. Basic analytical expression to extract the inductance of the metal lines, parallel conductors was given by Grover. Conventional inductor model proposed by Greenhouse, can precisely calculate the inductance [128]. This algorithm is very accurate, but employs large summation steps that depend on the number of interacting parallel conductor segments.

The analytical inductance extraction expressions are frequency independent and provide good results for the operating frequencies less than 2 GHz. Above this frequency, typical inductor tolerance value is of several percent order with the theoretical values largely deviating from experimental results. This is mainly due to the loss variation of the on-chip spiral at higher order frequencies. Modern wireless and mobile communications use SHF and millimetre wave circuits, where the frequency operation is from 3 -300 GHz. Frequency dependent accurate expressions are much need to extract the inductance value at the 5G frequency bands. Nevertheless, more accurate mathematical model to accurately predict inductance with different technology parameters is still an important research problem for the design and optimization of 5G RFICs.

The Greenhouse method calculates the inductance value as the sum of self inductance and mutual inductances of conductor segments (turns). It is a function of conductor spacing and segment dimensions. Total Mutual inductance is the difference between positive mutual inductance and negative mutual inductances. Mutual inductance is positive if the current flow in two conductor turns is in the same direction. It is negative if the current flow in two conductors is in opposite direction. The influence of conductor spacing on the negative mutual inductance gets decreased, if spacing between the opposite current flowing conductors is increased. Thus overall inductance gets increased, which further increase the Q value of the inductor [87]. Grover gave the numerical expressions for self and mutual inductance for different conductor structures. Conventional Greenhouse inductance extraction formula for rectangular cross-section involving both self inductance and negative mutual inductance.

4.2 Inductance Calculation

Consider a 3-turn spiral inductor rectangular cross-section, which has 12 conductor segments as indicated in the Fig. 4.1.

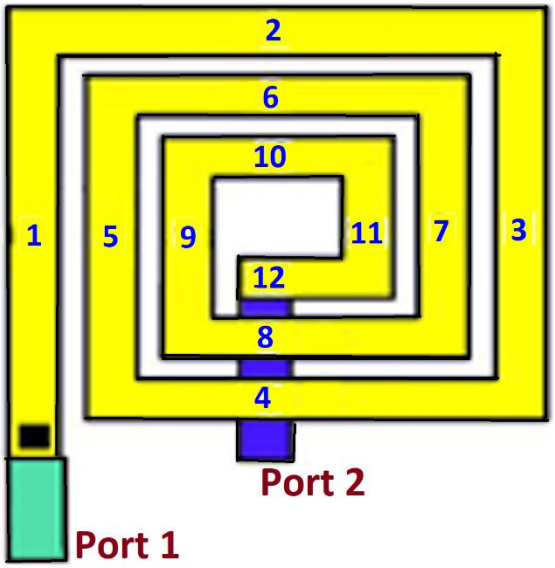


Fig 4.1 A three turn square shaped spiral inductor with inductances indicated

The expression for its self-inductance is given by

$$L_{self} = 0.2l_i\left\{ln\left(\frac{2l_i}{w+t}\right) + 0.5 + \left(\frac{w+t}{3l_i}\right)\right\}\mu H \qquad (4.1)$$

Where l_i is the i^{th} segment conductor length, w and t are conductor width and thickness (mtr) and μ is permeability of conductor metal. Total self-inductance for spiral inductor is thus

$$L_{self} = \sum_{i=1}^{12} L_i \tag{4.2}$$

Mutual inductance between any two adjacent segments is same with Mi,j=Mj,I [3]. Positive and negative mutual inductances for the three-turn spiral inductor are given as

$$M_{+ve} = 2\big(M_{1,5} + M_{1,9} + M_{2,6} + M_{2,10} + M_{3,7} + M_{3,11} + M_{4,8} + M_{4,12} + M_{5,9} + M_{6,10} + M_{7,11} + M_{8,12}\big) \tag{4.3}$$

$$M_{-ve} = 2\big(M_{1,3} + M_{1,7} + M_{1,11} + M_{5,3} + M_{5,7} + M_{5,11} + M_{9,3} + M_{9,7} + M_{9,11} + M_{2,12} + M_{2,4} + M_{2,8} + M_{6,4} + M_{6,8} + M_{6,12} + M_{10,4} + M_{10,8} + M_{10,12}\big) \tag{4.4}$$

Hence, the overall inductance is

$$L_{Total} = L_{Self} + \sum M_{+ve} - \sum M_{-ve} \tag{4.4}$$

The shunt and substrate capacitances of above planar inductor in hybrid lumped model are expressed as

$$C_{Subs} = C_{ox} \frac{[1+\omega^2(C_{ox}+C_{Si})C_{Si}R_{Si}^2]}{1+\omega^2(C_{ox}+C_{Si})^2R_{Si}^2} \tag{4.5}$$

$$C_{Shunt} = \frac{wlC_0}{2} \tag{4.6}$$

where, C_0 is substrate capacitance density (value in 0.01 to 0.001fF/μm^2), l is the total spiral length, n is the number of turns, W is metal width, t is metal thickness, t_{ox} is oxide thickness, ρ is the resistivity and δ is skin depth. The main objective of above layout is to achieve the desired inductance value with the smallest area possible, while keeping the parasitic capacitance lower enough to ensure SRF outside of the desired frequency band.

4.3 Analytical Inductance Extraction Method

Many frequency independent analytical expressions to extract the inductance for planar and multilayer inductors, were derived using the Greenhouse and Grover methods.

4.3.1 Greenhouse method:

The concept of negative mutual inductance influences the computation of the mutual inductance and also the total inductance for planar rectangular spiral inductors. Three major factors contribute to total inductance: Self-inductance of each segment; positive mutual inductance between line segments and the negative mutual inductance between line segments [128]. For an inductor with n turns and J segments, the number of +ve mutual inductance terms M_+ is equal to 4[n(n-1) + 2n(J-4n)].

Self-Inductance of Straight Conductor is given by

$$L = 0.002l\left\{ln\left(\frac{2l}{GMD}\right) + \frac{AMD}{l} + \left(\frac{\mu}{4}\right)T - 1.25\right\} \quad (4.7)$$

The Geometric Mean Distance GMD = 0.22352(w+t) and Arithmetic Mean Distance AMD = w/3. Total inductance of inductor is $L_{Total} = L_{Self} + M_+ - M_-$. The Q value of inductor is

$$Q = ln\left[\frac{l}{GMD} + \frac{GMD}{l} + \left\{1 + \left(\frac{l}{GMD}\right)^2\right\}^{\frac{1}{2}}\right] - \left[1 + \left(\frac{GMD}{l}\right)^2\right]^{\frac{1}{2}} \quad (4.8)$$

4.3.2 Modified Wheeler Formula:

The self inductance is calculated as a function of the number of turns using as a simple approximation to the Wheeler formula given by

$$L_{Mod.Wh.} = K_1\mu_0\frac{n^2 d_{avg}}{1+K_2\rho} \quad (4.9)$$

Where μ_0 is permeability of vacuum, K_1 and K_2 coefficients depend on inductor shape, n is the number of turns, d_{avg} is the average diameter and ρ is the filling ratio of the spiral. The values of K_1 and K_2 for a square shaped inductor are 2.34 and 2.75. A spiral inductor with more turns in a single layer, possess smaller inductance, as the innermost turns are closer to the spiral center. This reduces the positive mutual inductance and increases the negative mutual inductance. Hence, overall inductance is reduced. If central hollow space is increased, then total inductance increases. However, this makes the size of inductor bigger.

4.3.3 Current Sheet Approximation:

Inductance for a planar inductor is determined by considering the spiral segments as the current sheets of equivalent current densities. Pairs of parallel sheets contribute to mutual inductance (positive or negative), with each one having self-inductance. There are four identical current sheets for a square spiral inductor. The adjacent current sheets are orthogonal while the opposite ones are parallel. The self and mutual inductances are calculated using the geometric mean distance (GMD), arithmetic mean distance (AMD), and arithmetic mean square distance (AMSD) [129]. The self-inductance is evaluated as

$$L_{CSA} = \frac{\mu n^2 d_{avg} C_1}{2}\left(ln\left(\frac{C_2}{\rho}\right) + C_3\rho + C_4\rho^2\right) \quad (4.10)$$

where the layout coefficients C_1, C_2, C_3 and C_4 for a square spiral inductor are 1.7, 2.07, 0.18 and 0.03 respectively. ρ is the fill ratio and n is number of conductors. The error of this formula becomes large if the w/s ratio is large. The maximum error comes to 8% for s<3w.

4Inductance Extraction using Meander Inductors

Extraction of inductance for the multilayer inductors can be obtained from the concept of meander inductor based on the Greenhouse and Grover methods. Simple expressions for the self and mutual inductance are derived in terms of the conductor length, width and thickness parameters. The simplified analytical expression to determine the self inductance for an individual segment (turn) of a conductor is

$$L = 0.021\left[ln\left(\frac{2l}{w+t}\right) + \frac{w+t}{3l} + 0.50049\right] \quad (4.11)$$

where the layout parameters l, w and t are the w is the length, width and thickness respectively. The overall self inductance of an inductor is sum total of all the individual self inductances for each conductor segment. The conductor length, segment spacing between and the position shall be included in above analytical expression. The calculation of the mutual inductance based on meander inductance extraction is categorized into five cases . All these cases are based on above analytical expression of meander inductor.

Case-1: (Parallel filaments of equal length)

This assumes equal length for conductors, which are positioned at distance r in parallel as shown in Figure 4.2.

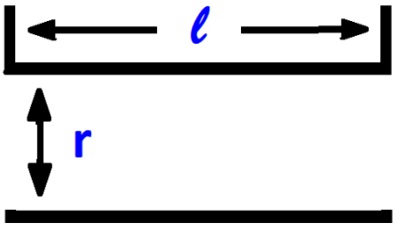


Figure 4.2. Parallel filaments of equal length

The calculation of the mutual inductance is given by the expression

$$M_{C1}(l,r) = \frac{\mu_0 l}{2\pi}\left[ln\left(\frac{l}{r}+\sqrt{1+\frac{l^2}{r}}\right)-\sqrt{1+\frac{r^2}{l}}+\frac{r}{l}\right] \quad (4.12)$$

Case-2: (Parallel filaments of unequal length with spacing)

This assumes unequal length for separated conductors, with a conductor spacing of s and a layer spacing of r as shown in Figure 4.3.

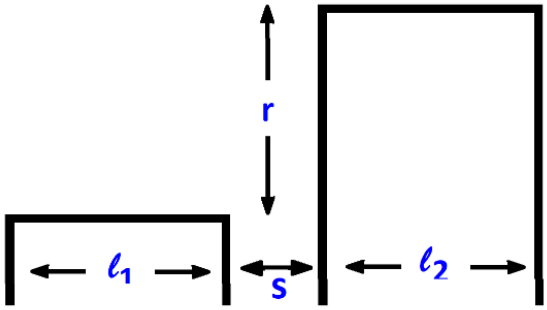


Figure 4.3. Parallel filaments of unequal length spaced apart by s

The calculation of mutual inductance for parallel filaments is given by the expression

$$M_{C2}(l_1,l_2,r,s) = 0.5\{M_c(l_1+l_2+s,r)+M_c(s,r)-M_c(l_1+s,r)-M_c(l_2+s,r)\} \quad (4.13)$$

Case-3: (Common end line perpendicular filaments)

This assumes unequal length for separated conductors that end in common perpendicular as shown in Figure 4.4.

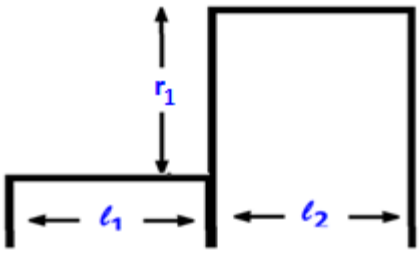


Figure 4.4. Conductor filaments of unequal length ending in common perpendicular

The calculation of the mutual inductance for common ending perpendicular filaments is given by the expression

$$M_{C3}(l_1, l_2, r_1) = 0.5\{M_c(l_1, r_1) + M_c(l_2, r_1) - M_c(l_1 - l_2, r_1)\} \quad (4.14)$$

Case-4: (Parallel filaments of unequal length without spacing)

Length is not same for parallel filament couple, which has no spacing as shown in Figure 4.5.

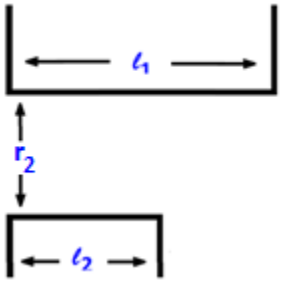


Figure 4.5. Conductor filaments of unequal length without spacing

The mutual inductance for conductor filaments without any spacing is given by the expression

$$M_{C4}(l_1, l_2, r_2) = 0.5\{M_c(l_1 + l_2, r_2) - M_c(l_1, r_2) - M_c(l_2, r_2)\} \quad (4.15)$$

Case-5: (Parallel segments of equal length with spacing on same axis)

Separated conductors lye on same axis, with conductor spacing of s as in Figure 4.6.

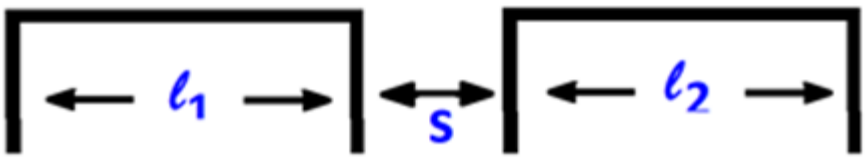


Figure 4.6 Parallel filaments of unequal length spaced apart by s

The calculation of the mutual inductance for conductor filaments on same axis is given by the expression

$$M_{C5}(l_1, l_2, s) = \frac{\mu_0}{2\pi}\left\{ \begin{array}{r} (l_1 + l_2 + s)\, ln(l_1 + l_2 + s) - (l_1 + s)\, ln(l_1 + s) \\ -(l_2 + s)\, ln(l_2 + s) + s\, lns \end{array} \right\} \quad (4.16)$$

The inductance values are extracted by using analytical expressions for the proposed Planar, 3D and multilayer inductors. HFSS simulation results obtained for these three inductors are compared with above analytical results to verify the accuracy. The performance comparison for above inductors is shown in Fig. 4.7, Fig. 4.8 and Fig. 4.9 respectively.

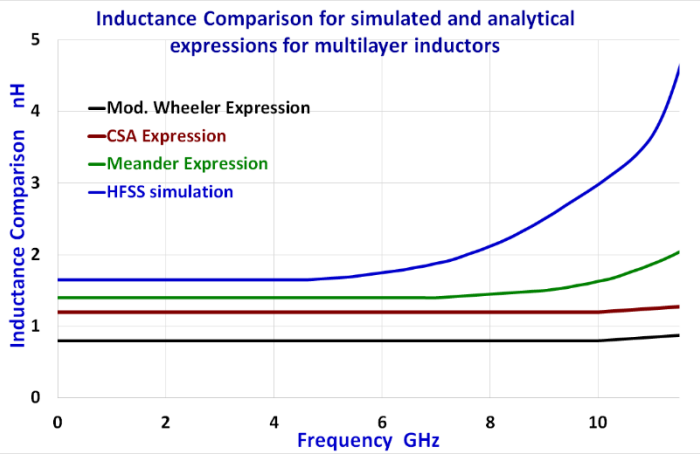


Figure 4.7 Inductance comparison of simulated and analytical expression results for a multilayer inductor.

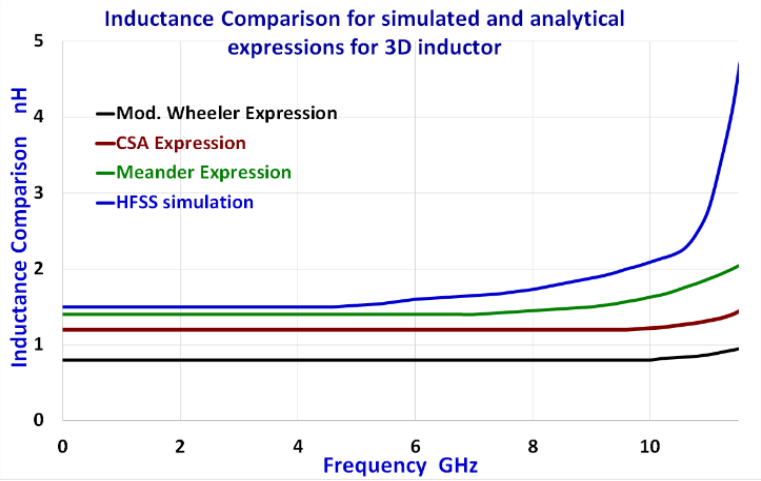


Figure 4.8 Inductance comparison of simulated and analytical expression results for a 3D inductor.

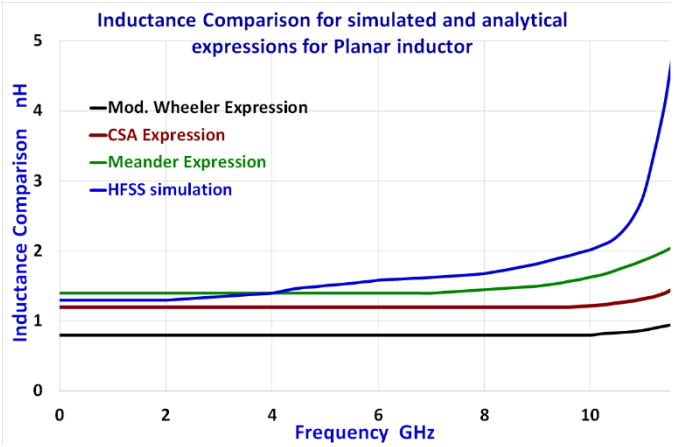


Figure 4.9. Inductance comparison of simulated and analytical expression results for a planar inductor.

It is observed that the inductance is deviating between the four extraction methods, as operating frequency increases. They are closely tallying below 6 GHz. The maximum percentage of error observed for the multilayer, 3D and planar inductors at 5.0 GHz is 108%, 90% and 87%, respectively. The inductance error between analytical and HFSS results for the multilayer inductor is larger than the 3D and planar inductors. This is mainly due to the increased parasitic losses caused by the skin and proximity effects.

4.4 Frequency Dependent Inductance Extraction using Integral method

The theoretical performance validation of the multilayer inductors proposed earlier, is derived from the fundamental electromagnetic (EM) field expressions. The inductance extraction for any design structure can be calculated by solving the Maxwell's equations. The magnetic force due to the magnetic field present in a conductor is used to derive the associated magnetic potential. This magmatic force by an EM field is through three main reasons:

i. current clement in the external magnetic field
ii. moving charged particles
iii. between two current elements.

Magnetic force present in the proposed inductors is due to current elements existing between the conductors. The magnetic potential for line, surface and volume currents is

$$A = \int \frac{\mu_0 I}{4\pi R} dl \quad \text{- line current} \tag{4.17}$$

$$A = \int \frac{\mu_0 K}{4\pi R} ds \quad \text{- surface current} \tag{4.18}$$

$$A = \int \frac{\mu_0 J}{4\pi R} dv \quad \text{- volume current} \tag{4.19}$$

Consider a 3-turn square inductor shown in Figure 4.1. It has totally 12 conductor segments numbered for easy identification. EM field appears between these conductors when they are parallel to each. Mutual inductance develops between these conductors with the presence of magnetic field. This mutual inductance may be positive or negative, depending on the current flowing direction. It is found that the positive mutual inductance is developed between the designated segment combinations {1,5,9}, {2,6,10},{3,7,11} and {4,8,12}. Negative mutual inductance is developed between the segment combinations {1,3,7,11}, (5,3.7,11), (9,3,7, 11}, {2,4,8,12}. {6, 4, 8, 12} and {10, 4, 8, 12}. Consider the depicted conductor pair as shown in Fig. 4.10 to calculate the value of mutual inductance.

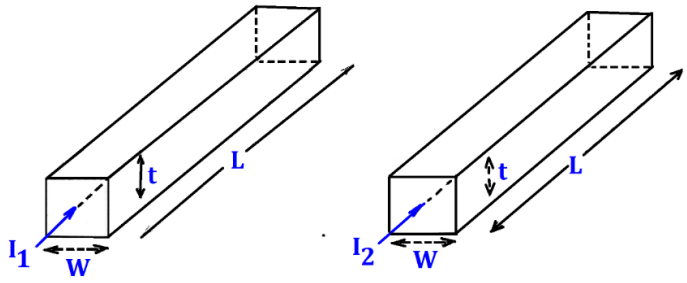


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Fig. 4.10 conductor pair structure to find current flow

Assume that the conductor current carried is in Z-direction. Now the two conductor currents are represented as $I_1 e^{-j\beta_1 z}$ and $I_2 e^{-j\beta_2 z}$. If conductor length is very less than wavelength, the phase associated with the conductor current flow is assumed to be zero over the full conductor length. The vector magnetic potential developed due to conductor current flow is given as

$$A_z(x,y,z) = \int \frac{\mu_0 I e^{-j\beta z}}{4\pi\sqrt{(x-0)^2+(y-0)^2+(z-0)^2}} dz \tag{4.20}$$

Assume that the conductor length is very less than wavelength. Then, the currents I1 and I2 with density J in volume v are uniformly distributed over throughout rectangular cross section. Hence $Jdv = \frac{l}{A} dAdl$. The expression for magnetic potential is

$$A_z(x,y,z) = \frac{\mu_0 I}{4\pi}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta z}}{\sqrt{(x-0)^2+(y-0)^2+(z-z^{|})^2}}\,dz \tag{4.21}$$

The magnetic field B is calculated as the curl of the magnetic potential A, expressed as

$$B = \nabla \times A \tag{4.22}$$

As the metal turns are closely placed, the flux passing through the center of conductor are linked. Magnetic flux is defined as the magnetic field penetrating the cross-sectional area of the second conductor, from the second conductor is given as

$$\varphi_{21} = \oint B\,ds = \mu \int H\,ds = \int (\nabla \times A)ds \tag{4.23}$$

Stokes theorem proved that potential A for a closed current path is determined as the surface integral of the curl of A over the bounded surface S. It is assumed that the potential A and its curl ∇xA are continuous on surface S.

$$\int (\nabla \times A)ds = \int A dl \tag{4.24}$$

Magnetic potential A between Consider the conductors are separated by distance d in x-direction. Now the magnetic potential A between the conductors is given from eqn. 4.21, as

$$A_z(x,y,z) = \frac{\mu_0 I}{4\pi}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta z}}{\sqrt{(d)^2+(z-z^{|})^2}}\,dz \tag{4.25}$$

Now the total φ_{21} flux in second conductor becomes

$$\varphi_{21} = \int A_z(d,0,z)dz \tag{4.26}$$

Substitute Equation 4.25 into Equation 4.22 to obtain the flux as

$$\varphi_{21} = \frac{\mu_0 I_1}{4\pi}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta_1 z^{|}}}{\sqrt{(d)^2+(z-z^{|})^2}}\,dz^{|}dz = \frac{\mu_0 I_1}{4\pi}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} \frac{e^{-j\beta_1 z^{|}}}{\sqrt{(d)^2+(z-z^{|})^2}}\,dzdz^{|} \tag{4.27}$$

Assume that $= \frac{z-z^{|}}{d}$. Now perform differentiation of flux w.r.t. z by considering $z^{|}$ as constant. Then dz = d.dt. The expression for flux becomes

$$\varphi_{21} = \frac{\mu_0 I_1}{4\pi}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}}\left\{\int_{\frac{-\frac{l_2}{2}-z'}{d}}^{\frac{\frac{l_2}{2}+z'}{d}}\frac{e^{-j\beta_1 z'}}{\sqrt{1+t^2}}dt\right\}dz' = \frac{\mu_0 I_1}{4\pi}\int_{\frac{-\frac{l_2}{2}-z'}{d}}^{\frac{\frac{l_2}{2}+z'}{d}} e^{-j\beta_1 z'}\left\{\int_{\frac{-\frac{l_2}{2}-z'}{d}}^{\frac{\frac{l_2}{2}+z'}{d}}\frac{1}{\sqrt{1+t^2}}dt\right\}dz' \quad (4.28)$$

$$\varphi_{21} = \frac{\mu_0 I_1}{4\pi}\int_{-\frac{l_1}{2}}^{\frac{l_1}{2}} e^{-j\beta_1 z'}\left\{sinh^{-1}\left(\frac{\frac{l_2}{2}+z'}{d}\right) - sinh^{-1}\left(\frac{-\frac{l_2}{2}-z'}{d}\right)\right\}dz' \quad (4.29)$$

Numerical integration method can be used to solve above expression, and ignore the higher order terms to obtain the flux as

$$\varphi_{21} = \frac{\mu_0 I_1}{\pi}\left\{aA\left(1 + \frac{\beta_1^2 a^2}{8} + \frac{\beta_1^4 a^4}{120}\right) - \frac{a^3 b B^3}{6}t_1\right\} \quad (4.30)$$

Where $a = \frac{t_1}{2}$; $b = \frac{t_2}{2}$; $A = log\left\{\frac{l_2}{2d} + \sqrt{1+\left(\frac{l_2}{2d}\right)^2}\right\}$ (4.31)

$$B = \frac{1}{\sqrt{d^2+\left(\frac{l_2}{2}\right)^2}} \qquad t_1 = 1 + \left\{\frac{6\beta_1^2 a^2 - 9B^2 a^2 + 15 b^2 B^4 a^2}{20}\right\} \quad (4.32)$$

$$\beta_1 = \frac{2\pi}{\lambda_{eff}} \qquad \lambda_{eff} = \frac{C}{f_0 \epsilon_{eff}} \qquad \epsilon_{eff} = \frac{(T_{Si}+T_{SiO2})\epsilon_{Si}\epsilon_{SiO2}}{T_{Si}\epsilon_{SiO2}+T_{SiO2}\epsilon_{Si}} \quad (4.33)$$

Where T_{si} is silicon thickness, T_{SiO2} is oxide thickness, ϵ_{Si} is silicon dielectric constant and ϵ_{Si} is oxide dielectric constant. The Equation 4.30 for the magnetic flux is solved using numerical integration and the solution obtained is substituted in mutual inductance equation.

Inductance is the ratio of total flux linkages to the current I. Self-inductance is L=φ/I. Mutual inductance developed on conductor turn 2 due to the impinging flux from another conductor turn 1 is given as

$$M_{21} = \frac{\varphi_2}{I_1} = \frac{\mu_0 I_1}{4\pi}\left\{\frac{\varphi_{21}}{I_2 e^{-j\beta_2 z}}\right\} = \frac{\mu_0 I_1}{4\pi I_2}\left\{\frac{\varphi_{21}}{e^{-j\beta_2 z}}\right\} \quad (4.34)$$

The current flowing in all the conductors will be equal if conductor loss is made zero. Thus the two conductor currents I1 and I2 in above equation cancel each other. Thus mutual inductance in simplified form is given as

$$M_{21} = \frac{\mu_0}{4\pi}\left\{\frac{\varphi_{21}}{e^{-j\beta_2 z}}\right\} \quad (4.35)$$

The performance of the numerical integral method are compared with the HFSS simulation results for the planar, 3D and multilayer inductors, as done in section 4.3. The results are given by comparison plots in following Figure 4.11, 4.12 and 4.13.

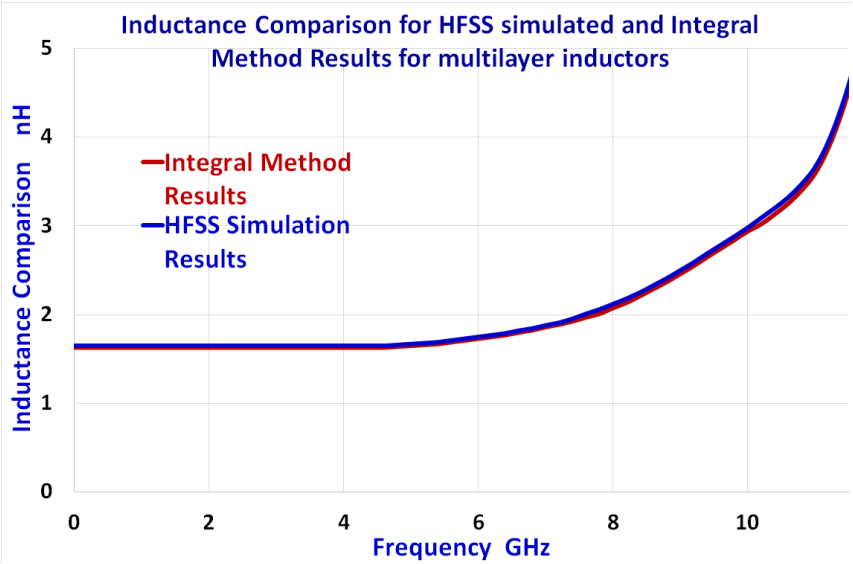


Figure 4.11. Inductance comparison of simulated and analytical expression results for a multilayer inductor.

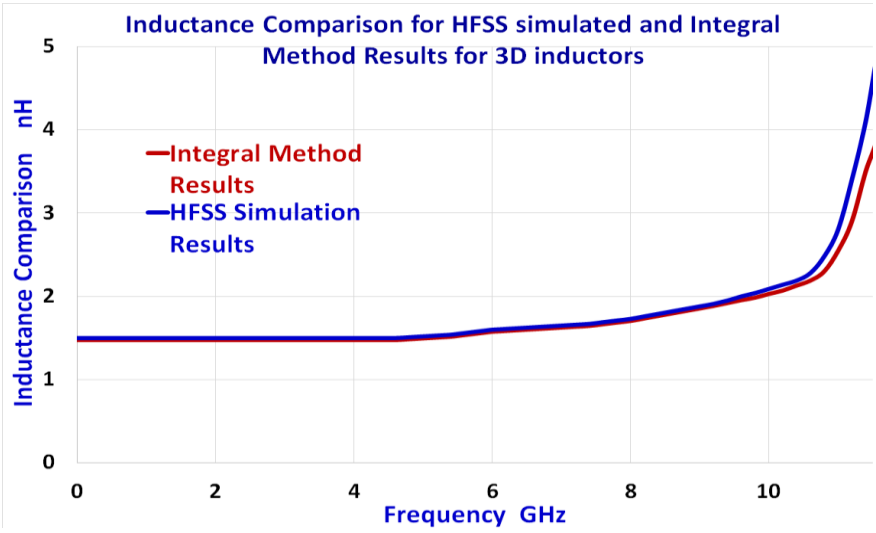


Figure 4.12. Inductance comparison of simulated and analytical expression results for a 3D inductor.

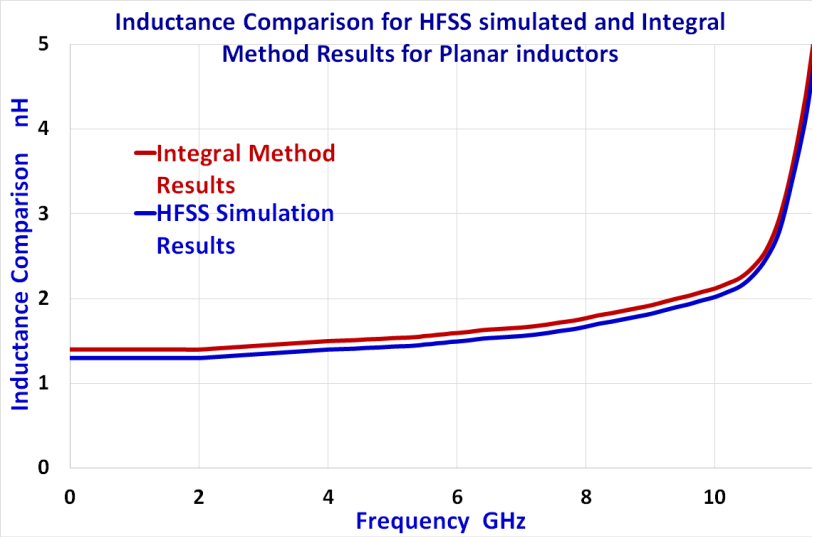


Figure 4.13. Inductance comparison of simulated and analytical expression results for a planar inductor.

The above results indicate that proposed integral model is more accurate in the inductance calculation, due to close agreement with the HFSS simulated results throughout the sub-6 GHz 5G band of operation. The maximum error percentage for the integral solving model w.r.t simulation results is 1.21%, 1.6%, and 2.3% at 5 GHz frequency, for the multilayer inductor, 3-D inductor and planar inductors correspondingly. The above results also indicated that the error percentages beyond the SRF, increasingly become larger. It can be concluded that the integral based inductance extraction is more accurate but needs complex numerical integration procedure. These results do closely tally with EM field solver like HFSS. Hence, the simulation results produced by HFSS are acceptable in practice to design and develop high performance 5G RFICs using the proposed IPD on-chip passive components.

4.5 Inductance Expressions:

The spiral inductance is represented as a function of: line segment width w, segment spacing s, its thickness t and number of segments n and the outer dia d_{out}.

$$L = f(w, s, t, N, d_{out}) \tag{4.36}$$

a) Bryan Formula

The Bryan inductance extraction equation is applicable to a planar square inductor.

$$L_{Bryan} = 0.141an^{\frac{5}{3}}ln\left(\frac{8a}{c}\right) \quad (4.37)$$

where the dimensions a and c are in centimeters.

b) Crols Formula

$$L_{Crols} = K_L \frac{d^2}{w^2}\left(\frac{conductor\ area}{total\ area}\right)^{\frac{5}{3}}\left(\frac{w}{w+s}\right) \quad (4.38)$$

w is width, s is spacing, d is outer dia, KL =1.3*10^{-7} H/m

c) Modified Wheeler's Formula

$$L_{mod.Wheeler} = 2.34\mu_0\left(\frac{N^2 d_{avg}}{1+2.75\rho}\right) \quad (4.39)$$

$d_{avg} = \frac{d_{in}+d_{out}}{2}$ d_{in}=inner diameter and d_{out}=d

$$Fill\ Ratio\ \rho = \frac{d_{out}-d_{in}}{d_{out}+d_{in}} \quad (4.40)$$

d) CSA Formula

$$L_{CSA} = \frac{1.27\mu N^2 d_{avg}}{2}\left\{ln\left(\frac{2.07}{\rho}\right) + 0.18\rho + 0.13\rho^2\right\} \quad (4.41)$$

e) Data Fitted Monomial Expression

This is the least square data fitting expression. All exponents are chosen to minimize the error over the family of inductors (19000 approx.). This fitting method results in only six constants.

$$L_{Monomial} = 1.62 \times 10^{-3}\, d_{out}^{-1.21} w^{-0.147} N^{1.78} s^{-0.03} \quad (4.42)$$

4.6 Summary:

This chapter discusses induction extraction methods to validate the simulation and experimental results for the proposed on-chip passive components. Available analytical expressions are like the modified Wheeler, Greenhouse, CSA and numerical integration models are used for this purpose. The performance comparison plots for three types of proposed IPD inductor structures (Planar, 3D and multilayer) is presented. They indicated accuracy deviations between the theoretical values and simulated results, especially at high

frequencies beyond 6 GHz. The maximum percentage of error observed for the multilayer, 3D and planar inductors at 5.0 GHz is 108%, 90% and 87%, respectively. But, maximum error percentage for the integral solving model w.r.t simulation results is 1.21%, 1.6%, and 2.3% at 5 GHz frequency, for the above three inductors correspondingly. Therefore, it can be concluded that numerical integral method-based inductance extraction is more accurate, as their values are closely tallied by field solver tool HFSS.

Chapter 5

Low Noise Amplifiers for 5G Applications

5.1 Introduction

Globally deployed ultra-speed low latency 5G standard offers eMBB, mMTC, D2D and V2V services to support mission critical communication services like: LTE, IEEE 802.11 WLAN, HIPERLAN II, UWB, massive IOT, M2M, D2D, smart city logistics, mobile HDTV, Accurate GPS location (5G wideband) etc. The Sub-6 GHz spectrum (1 to 6 GHz) is popular 5G industry choice, with NR N79 using 4.4 to 5 GHz and NR-U using 5.1 to 5.9 GHz spectrum.

The performance of the RF front end heavily influences the overall sensitivity, selectivity and fidelity of any mobile receiver or wireless transceiver. Being the first active gain component, the LNA is the direct influencer of overall receiver noise performance. It is still a big design challenge to simultaneously optimize the desired LNA parameters like minimum on-chip area (OCA), small losses, input and output matching, smaller NF, and higher gain, high linearity and unconditional stability. More recently, researchers are concentrating on highly miniaturized LNAs to enhance the sensitivity of low power and high QOS RFICs for smart 5G receivers. It is identified that the occupied die sizes are still very large.

This chapter reports and discusses, the design and fabrication of proposed multilayer on-chip IPD inductors successfully to develop high performance 5G CMOS LNAs with minimized die size [130]. The proposed novel series stacked double split multilayer IPD spiral inductor had shown excellent improvement of the performance metrics against planar and other multilayer inductors in 5G bands (sub-6 GHz low band and 25-30 GHz high band). Active components of LNA circuit are simulated with low-cost CMOS technology, while the proposed

passive inductors are realized in small size IPD technology. Thus, the power loss became smaller than CMOS process, but at highly reduced chip space.

This work proposes a compact LNA using constant width and double split multilayer IPD inductors designed and simulated in ADS at 5.0 GHz and 5.5 GHz. Section.5.2 explains the design, simulation, fabrication and testing of these two multilayer IPD inductors, successfully used to implement a narrowband degenerated cascode LNA at 5.0 GHz. The implemented LNAs yielded good impedance matching with reduced parasitic capacitance. Section.5.3 illustrates the design, simulation and fabrication of above two multilayer IPD inductors, successfully used to implement a narrowband degenerated cascode LNA at 5.5 GHz. The high frequency performance of these LNAs are compared with corresponding state of art LNA designs reported in literature.

5.2 Design and Implementation of 5.0 GHz LNA

Optimal system on chip (SOC) 5G LNA designs, primarily focus on minimal chip area via happy integration of low-cost CMOS process and high quality IPD passives. This work focuses to achieve best LNA performance by careful iterative trade-offs between all the process and geometry parameters of active parts and on chip passives. Specifically, active components of LNA circuit are designed and simulated on 90 nm CMOS technology, while the passive inductors are realized in IPD process.

Several research works in the past had employed LNA circuit designs selected from: CMOS processes (TSMC/UMC - 60, 90, 130 and180 nm); amplifier configurations (body floating and self-bias, current-reuse, CS cascode structures); Transistors (NMOS, PMOS, FinFET, pHEMT), Matching networks (gyrator, bridged T coil, fractal, IPD and active inductors [93]. Each work reported significant improvements in few parameters but had larger occupied chip area. In order to achieve above goal, salient characteristics employed in this work are: inductively degenerated first stage CS cascode amplifier, gain boosting peaking inductor, Constant K passive 50Ω input matching prefilter, isolating second stage output buffer amplifier and optimal NMOS transistor channel length and width, etc.

LNA Topologies and Challenges:

The LNA technologies employed the semiconductor processes are: microstrip, SAW, SiGe, Bipolar BJT, n-channel JFET, GaAs FET, MESFET, MMIC, CMOS, BiCMOS,

MOSFET, MODFET, BiFET, FinFET, HBT, HEMT and pHEMT Processes [131]. CMOS and BiCMOS are popular below 10 GHz, while HEMT is employed beyond 10 GHz [31]. Three popular topologies of LNA employed are: Inductive peaking topology (reduced roll-off and wider bandwidth), Noise and distortion cancellation topology (enhance linearity, narrowband, small NF, small IP3, high power consumption) and Gain (gm) boosting topology (high gain, reduced NF and power dissipation) [132].

A Common Gate (CG) amplifier and a shunt feedback amplifier can enhance overall transconductance gm. The current-reused use CS amplifier followed by cascode stage to obtain high power gain, good stability and decrease power consumption. The Peaking inductor technique reduces the roll-off, enhance the bandwidth and achieve flatter gain. The active inductor technique will make the LNA wideband. This is utilized to lower the output impedance, but may have low NF [133]. The filtering technique employs T match, Pie match, Constant K filter match for best impedance matching to enhance the gain and NF reduction. Inductive source degeneration technique provides simultaneous input impedance matching and smaller noise. Capacitive cross coupling technique with CS-CG cascade reduces miller effect for high gain and low NF.

5.2.1 On-chip 5.0 GHz LNA design using proposed IPD passives

Key LNA design parameters are: Process technology, center frequency, gain, loss parameters (S11, S22), noise figure, stability factor K, linearity (1dB compression P1, 3rd order Intercept IIP3), supply voltage, and on chip Area (OCA) [134]. The design specifications for proposed miniature 5.0 GHz C Band LNA are given in following Table 5.1

The proposed LNA is designed with three stages: Input matching network, Single stage cascode amplifier and an Output buffer stage. The source degenerated cascode LNA circuit is shown in Fig. 5.1. Second stage source degenerated cascode CS-CG amplifier offers high forward gain, high linearity, low power consumption and low NF by minimizing the gain reducing evil miller effect of drain overlap capacitance (Cgd). The gain of transistor M1 is stabilized with negative feedback provided by source inductor (Ls). Gate inductor (Lg) of input transistor M1 helps in power match to preceding stage [108]. Larger Lg reduces the NF also. Both M1 and M2 transistors use same DC current and reduce current consumption. The cascode transistor M2 provides good reverse isolation. The last stage CG buffer amplifier achieves good isolation, further gain and better output matching.

Table 5.1. Desired 5.0 GHz LNA Specifications

LNA Parameter	**Desired Specification**
Technology	90 nm CMOS
Center Frequency f_0 (GHz)	5.0
Bandwidth (GHz)	4.8 to 5.2
Gain G (dB)	> 25.0
Noise Figure NF (dB)	< 1.5
Stability K	2 to 5
Input Return Loss S11(dB)	< -25
Reverse Isolation S12 (dB)	< -30
Output Return Loss S22 (dB)	< -10
1dB Input Compression Point P1 (dBm)	> -10
IIP3 (dBm) ~ (P1+10)	> 0
P_{diss} (mW)	< 10
Supply Voltage (V)	1.5 to 2
On Chip Area OCA (mm^2)	< 0.1

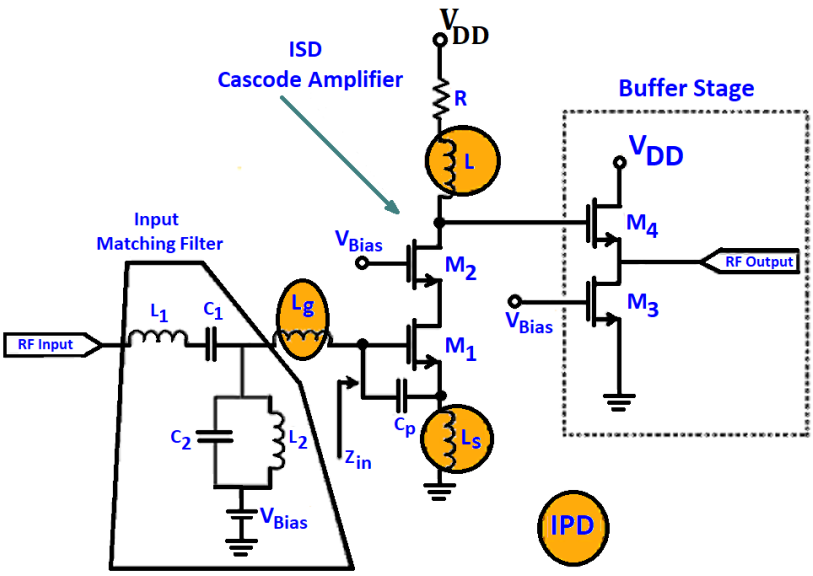


Fig. 5.1 The source degenerated cascode LNA circuit

We need to choose the value of 'Cgs' of M1 for noise matching such that,

$$C_{gs} = \frac{2G_{opt}}{2\pi f} \quad (5.1)$$

where G_{opt} is the optimum admittance of source. For lower NF, it is equal to 1/50. Thus Cgs shall be 1.21 pF. Input matching network consists of C_1, L_1, L_2, C_2, Lg and C_{gs}. Since the NMOS transistor has C_{gs} about 30 fF, we choose to add a parallel capacitance C_p of 1.2pF across the gate and the source. The value of R must ensure LNA stability. The drain peaking inductor L resonates with drain capacitance to achieve maximum gain at tuned resonance.

Degenerative inductor L_S sets the value of Z_{in} by tuning out gate-source capacitance C_{gs}. L_g tunes the input circuit at the desired resonance frequency. Inductance (L_g+L_s) and C_{gs} are resonated at 5.0 GHz center frequency to eliminate the imaginary part to achieve best input impedance Z_{in} match to 50Ω. Same IPD structure is used for the biasing inductors L_S, L_g, and L, to minimize the loss and facilitate ease of fabrication. LNA is simulated with body-contacted NMOS transistors in 90 nm CMOS process, using ADS 2016.01 software. The MOSFET has minimum gate length of 70 nm and a 0.3 V threshold voltage.

Design of input matching constant K bandpass filter:

The first stage is a constant K bandpass filter (BPF), which tunes the LNA to minimize input return loss (S11). Chebyshev Constant K filter is designed to simulate the 5.0 GHz BPF, as shown in Figure 5.2. The filter is matched to the 50 Ω source impedance (antenna). The inductors and capacitors L1 and C1 in series and L2 and C2 in shunt form an LC resonator. L_g and C_{gs1} are used to form a tank circuit at the source terminal of M1. All these tank circuits together form the 50 Ω impedance matching network.

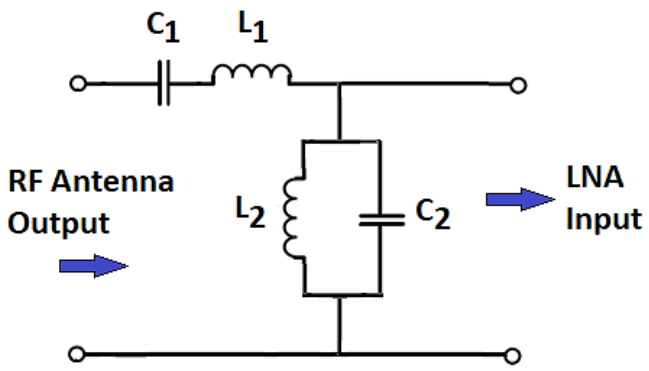


Figure 5.2. Input matching Constant K LC Bandpass Filter

Inductor and capacitor values are found with, f_0= 5GHz, f_2= 5.2 GHz; f_1= 4.2 GHz and Z_0= 50 Ω. The series and shunt reactive components are computed from following equations.

$$L_1 = \frac{Z_0}{\pi(f_2 - f_1)} \tag{5.2}$$

$$L_2 = \frac{Z_0(f_2 - f_1)}{4\pi f_1 f_2} \tag{5.3}$$

$$C_1 = \frac{(f_2 - f_1)}{4\pi Z_0 f_1 f_2} \tag{5.4}$$

$$C_2 = \frac{1}{\pi Z_0(f_2 - f_1)} \tag{5.5}$$

The computed BPF component values are:

L_1= 26.5 nH, C_1=38.3 nF, L_2= 0.095 nH, and C_2= 10.6 pF.

Design steps of the first stage cascode ISD amplifier components:

The inductive source degenerated (ISD) cascode CS LNA circuit and its input equivalent circuit are given in Figure 5.3. Its input impedance is ratio of input voltage (V_{in}) to input current (I_{in}) given in Equation 5.9.

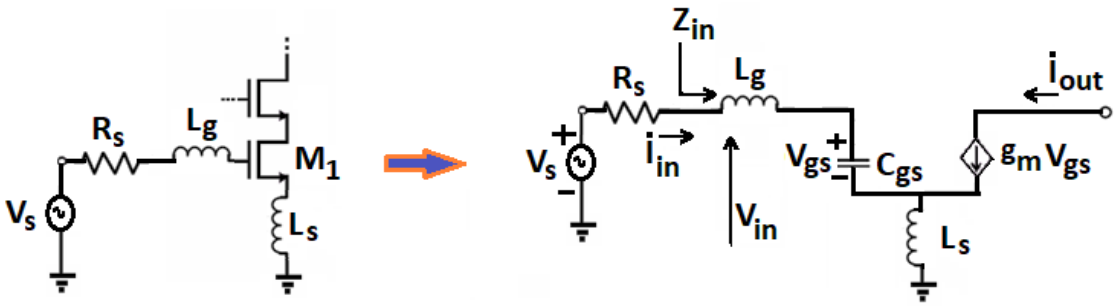


Figure 5.3. Inductive source degenerated LNA and its input equivalent circuit

$$V_{gs} = \frac{I_{in}}{sC_{gs}} \tag{5.6}$$

Assuming the parasitic resistances R_g, R_{Ls} and R_{Lg} as negligible, we have

$$V_{in} \cong I_{in}sL_g + I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m V_{gs})sL_s = I_{in}sL_g + I_{in}\frac{1}{sC_{gs}} + \left(I_{in} + g_m \frac{I_{in}}{sC_{gs}}\right)sL_s \tag{5.7}$$

$$V_{in} = I_{in}\left[s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{mL_s}}{C_{gs}}\right] \tag{5.8}$$

Here, s is complex frequency, L_g is gate inductance, L_s is source inductance, C_{gs} is gate to source capacitance and g_m is transconductance of M_1. Now, the input impedance is

$$Z_{in} = \frac{V_{in}}{I_{in}} = \left[s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{mL_s}}{C_{gs}}\right] \cong s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s \tag{5.9}$$

The condition for best input impedance matching, Re (Z_{in}) = R_{in}=50 Ω and Im (Z_{in})=0 at resonance f=f_0. Thus, Ls and Lg are chosen to satisfy above conditions [20].

$$j\omega_0(L_g + L_s) + \frac{1}{j\omega_0 C_{gs}} = 0 \implies \omega_0^2(L_g + L_s)C_{gs} = 1 \tag{5.10}$$

$$s(L_g + L_s) + \frac{1}{sC_{gs}} = 0 \implies \omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{5.11}$$

Re (Zin) must be equal to source resistance R_s, so that

$$Re[Z_{in}] = R_{in} = R_g + \frac{g_m}{C_{gs}} \cdot L_s = \omega_T L_s = R_s = 50\,\Omega \tag{5.12}$$

where R_g is gate resistance of NMOS transistor, which is negligible.

Source inductor L_s performs impedance matching. Gate inductor L_g sets input resonant frequency, as per Equation 5.11 and Equation 5.12.

$$Q_{in} = \frac{1}{wC_{gs}R_{in}} = \frac{1}{\omega_0(R_s + \omega_T L_s)C_{gs}} = \frac{1}{2\omega_0 R_s C_{gs}} = \frac{\omega_0(L_g + L_s)}{2R_s} \tag{5.13}$$

Therefore capacitor voltage at resonance is

$$V_{gs} = Q_{in}V_{in} \tag{5.14}$$

Thus, the effective transconductance g_{m1} of this cascode LNA topology, is given

$$g_{m1} = \frac{I_D}{V_{in}} = Q_{in} * g_m = \frac{g_m}{wC_{gs}R_{in}} = \frac{\omega_T}{\omega_0\left(1 + \frac{\omega_T L_s}{R_s}\right)R_s} \tag{5.15}$$

where Q_{in} is input matching network Q value, ω_0 and ω_T are the center and transition angular frequencies, respectively. Ls is chosen to determine ω_T using Equation 5.12. Now find

the value of C_{gs} using above ω_T by taking g_m= 25 mA/V. Gate inductor L_g is found by substituting f_o, Cgs, and Ls in Equation 5.10.

Computing the gain for LNA:

The gate-drain capacitance Cgd, and output resistance R_{ds}, of transistors M1 and M2 are neglected as per technology. For an ISD LNA in Figure 5.1, we put a lower bound on g_{m1} to ensure maximum gain.

LNA voltage gain is determined from Figure 5.3, as the ratio of output and input voltages:

$$A_v = G_m * Z_l(\omega) = \frac{-G_m L_s}{1-\omega_0^2(L_g+L_s)C_{gs}+sG_m L_s} \qquad \Longrightarrow G_m = \frac{I_{out}}{Vin} \tag{5.16}$$

$$A_v \cong Q_{in} g_{m1} Z_L = g_{m1} Z_{eq} = \left(\frac{1}{j\omega_0 L_s}\right)\left(\frac{j\omega_0 L}{1-\omega_0^2 L_1 C_0}\right) = \frac{L}{L_s}\left(\frac{1}{1-\omega_0^2 L_1 C_0}\right) \tag{5.17}$$

Relating eq. (10) and eq. (18), we find gain in simple form as

$$Gain\ in\ dB = 20\ log\frac{V_{out}}{Vin} = 20log\left(\frac{L}{L_s}\right) \tag{5.18}$$

Hence, the drain peaking inductor L must be chosen large enough to get maximum LNA gain. Maximum inductance achievable for 90 nm CMOS process is 10 nH. L is calculated to achieve the proposed 35 dB gain.

Noise Figure Evaluation:

Noise factor (F) is defined as ratio of input SNR to output SNR. Noise Figure (NF) is nothing but noise factor expressed in dB.

$$NF\ dB = 10\ logF = 10\ log\frac{SNRin}{SNRout} \tag{5.19}$$

Noise figure for an ISD cascode CS LNA at 5 GHz frequency (f_o) is expressed as

$$NF = 1 + \frac{\gamma}{g_m R_s}\omega_0^2\left(R_s C_{gs} + g_m L_s\right)^2 \tag{5.20}$$

Now substitute Equation 5.11 and Equation 5.17 into Equation 5.20 to obtain NF.

$$NF = 1 + \gamma\frac{4(g_m L_s)^2}{g_m R_s}\frac{1}{(L_g+L_s)C_{gs}} = 1 + \frac{4\gamma L_s}{(L_g+L_s)} \tag{5.21}$$

Here γ is the channel thermal noise coefficient whose value lies in the range [2, 3]. Lower NF is obtained by selecting small Ls and large Lg.

Stability Analysis:

Any LNA is designed to be unconditionally stable. The Stern stability factor is used.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2-|\Delta|^2}{2|S_{12}||S_{21}|} \qquad \text{with} \qquad \Delta = |S_{11}||S_{22}| - |S_{12}||S_{21}| \tag{5.22}$$

Any amplifier is stable if K>1 and $|\Delta|$<1. More recently K and Δ are equivalently replaced with parameter μ (with μ >1), defined as

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta conj[S_{11}]|+|S_{12}*S_{21}|} \tag{5.23}$$

Optimal width (W_{opt}) calculation for the LNA NMOS transistors:

The values of Vds and Vgs are predetermined for NMOS transistor. The desired I_{DS} is dependent on W/L ratio. For 90nm CMOS technology, minimum channel length (ℓ_{min}), is fixed at 90nm. The optimum channel width (W_{opt}) of input transistor M1 decides I_{ds} and NF. The maximum width of each transistor to obtain best noise performance is defined by

$$W_{opt} = W_{opt:F_{min}} = \frac{1}{3\omega_0 \ell_{min} C_{ox} R_s} \tag{5.24}$$

Here C_{ox} is gate oxide layer capacitance per unit area [F/m^2] defined as

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{K_{ox}\epsilon_o}{t_{ox}} \tag{5.25}$$

Where ϵ_{ox} and K_{ox} =3.9 are the permittivity in [F/m] and relative permittivity of the gate oxide SiO_2. ϵ_o is permittivity of the vacuum ($8.85*10^{-12}$) [F/m] and t_{ox} is gate oxide thickness t_{ox} =$3.45*10^{-11}$ [m]. We can find C_{ox} using Eqn. (25) and substitute it in Eqn. (24) to find optimal width W_{opt}. The gate to source capacitance is given by

$$C_{gs} = \frac{2}{3} W_{opt} \ell_{min} C_{ox} \tag{5.26}$$

Analysis of power dissipation:

Power consumption is minimized by using smaller bias voltage for input transistor M1. Gain boosting cascode transistor M2 is biased with higher voltage. Effective voltage V_{eff}

applied to transistor M1, is the difference between V_{gs} (gate -source voltage) and V_{th} threshold voltage. Bias current is found from

$$I_D = \frac{1}{2} \cdot g_m \cdot V_{eff} = \frac{1}{2} \cdot g_m \cdot (V_{gs} - V_{th}) \quad (5.27)$$

Threshold voltage for an n-channel MOSFET is expressed as

$$V_{th} = 1 + \gamma\left(\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F}\right) \quad (5.28)$$

Here, V_{SB} is source - body voltage, V_{t0} is threshold voltage for V_{SB}=0 and φ_F is process parameter lying in [0.3-2.4]. Power dissipation (P_D) is equal to $V_{DD}.I_D$. The transistor widths also are carefully adjusted to reduce power dissipation. Complete LNA circuit consumes about 600 μA from 1.8 V supply at power dissipation around 1.4 mW.

LNA Component Selections:

The design of proposed LNA is done in TSMC 90 nm CMOS technology. Thus, all the NMOS transistors have same minimal length of 90 nm. Width W_1 of Transistor M_1 is selected as 80 μm very close to the optimal width 80 μm. The width W_2 of cascode transistor M_2 is chosen as 70 μm (less than that of M_1) to minimize the parasitic capacitances 66]. Cascode amplifier gain is controlled by the load inductor L and resistor R_L. Inductor and the width of transistor are optimized for minimum noise figure. The 50 Ω load driving buffer stage uses two transistors M_3 and M_4 (under saturation), with widths W_3 and W_4 found as 65μm and 50 μm. Table 5.2 presents the list of optimized component values and technology parameters for the designed compact high performance 5 GHz LNA circuit. To accomplish the main goal of low cost, low power, low NF and least chip space, the design constraints used for the circuit components are listed below.

(1) $50 \leq W_1, W_2, W_3, W_4 \leq 100$ μm (2) $0.1 \leq Ls, Lg, L \leq 5$ nH

(3) $20 \leq C_p \leq 30$ fF (4) $50 \leq W_{opt} \leq 100$ μm

The optimized component values of proposed 5 GHz cascode CMOS LNA based on the technology parameters have been found as following constants:

Table 5.2. Optimized component values of proposed 5 GHz cascode CMOS LNA circuit

Component	Value
Input BPF – L1, L2, C1, C2	26.5 nH, 0.095 nH, 38.3 fF, 10.6 pF
Input Cascode – Ls, Lg, L	0.9 nH, 2.4 nH, 3.28 nH
Channel length ℓ_{min}	0.09 µm
Channel width W_{opt}	80 µm
W_1, W_2, W_3, W_4	80.16 µm, 70.25 µm, 68.23 µm, 57.95 µm
V_{bias} (input transistor)	816.5 mV
V_{bias} (cascode transistor), Vbias (buffer stage)	1.1 V, 545 mV
Supply Voltage V_{DD}	2.2 V
Capacitances C_{ox}, C_{gs}, C_p	8.42 nF/m^2, 141 fF, 30.96 fF
Resistances R, R_s, R_L	60 Ω, 50 Ω, 50 Ω
Substrate-bias coefficient γ	2

Cascode LNA Implementation:

Proposed LNA circuit is simulated in 90 nm CMOS with ADS 2016.01 software to operate at desired 5 GHz. LNA design and implementation is performed using both the on-chip and off-chip inductors and capacitors to compare their performances.

Input Matching BPF Simulation:

The reactive components L_1, L_2, C_1, and C_2 of the Chebyshev Constant K bandpass filter are calculated from the Equations 5.1 to Equation 5.4, using 4.8 GHz and 5.2 GHz as the upper and lower cutoff frequencies (Δf=400 MHz). The optimal values of L_1=26.5 nH, L_2=0.095 nH, C_1=38.3 fF and C_2=10.6 pF are used to obtain resonance at 5.0 GHz and also 50Ω input match. The simulated ADS filter circuit is shown below in Figure 5.4.

This proposed BPF exhibited a 3 dB bandwidth Δf=5.4-4.8= 0.6 GHz in C band, with a fractional BW of 12%.

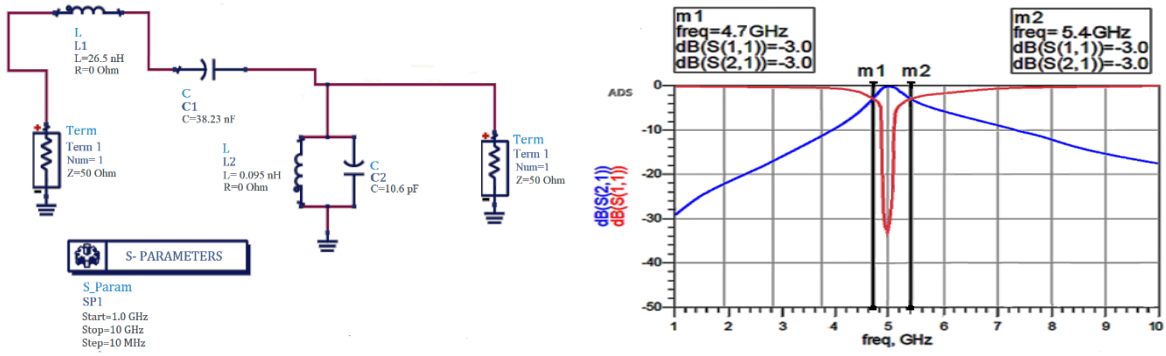


Fig. 5.4 Simulated 5 GHz Chebyshev BPF in ADS and the Passband of BPF in C band

Simulation of Cascode amplifier inductors:

Both the on-chip 90 nm CMOS inductors (microstrip line) and offchip IPD inductors (Ls, Lg, and L) of first stage CS amplifier are designed and simulated in ADS (L_Model) and HFSS respectively. Two types of on-chip IPD ML spiral inductors (constant width and a novel double split inductor) having same chip area are designed, simulated and fabricated. Their performance is tested to check for 5 GHz suitability.

The ratio of outer to inner diameter is chosen in range [3,5] to enhance the Q factor and inductance at higher frequencies. Overall inductance of spiral geometry is given by

$$L_{Total} = L_{Self} + \sum M_{+ve} + \sum M_{-ve} \tag{5.30}$$

The inductance of rectangular spiral is extracted using modified Wheeler's formula. The Q value of inductor is evaluated as.

$$Q = \frac{\omega L_S}{R_S} \frac{1}{1+\frac{R_S}{R_p}\left\{\left(\frac{\omega L_S}{R_S}\right)^2+1\right\}} \left[1 - \frac{R_S^2(C_S+C_p)}{L_S} - \omega^2 L_S(C_S + C_p)\right] \tag{5.31}$$

ADS inductor model uses copper conductor. IPD inductor model uses a 300 µm thick silicon substrate and 12 µm thin oxide layer to reduce losses and enhance the Q factor. The Process and layout parameters of the proposed inductors are given in Table 5.3. The mutual inductance is increased by splitting the conductor path width into two tracks by creating space between them.

Table 5.3 Process and Geometrical parameters of Spiral Inductors

Type of Inductor	Substrate	Number of turns	Outer dia l µm	Conductor Width (W) µm	Conductor spacing (S) µm	Number of tracks per turn	On chip area mm^2
ADS CMOS (Ind. Model)	Copper	Microstrip Line	-	-	-	-	0.0324
IPD Constant Width ML inductor	Si	4 (one full turn per each layer)	180	10	2	1	0.0324
IPD Double split ML Inductor	Si	4 (half turn per each layer)	180	4.5	2	2	0.0324

The L and Q values of these simulated inductors were found as

$$Q = \frac{Im\,[Y_{11}]}{Re\,[Y_{11}]} \qquad L = \frac{-1}{2\pi f\{Im\,[Y_{11}]\}} \quad \text{and} \quad R_s = \frac{1}{Real\,[Y_{12}]} \tag{5.32}$$

Planar view of geometrical structure for the two HFSS simulated inductors is shown in Fig. 5.6. The constant width and double split path of each conductor turn into two separate tracks with, in between spacing are reflected in this Figure 5.5.

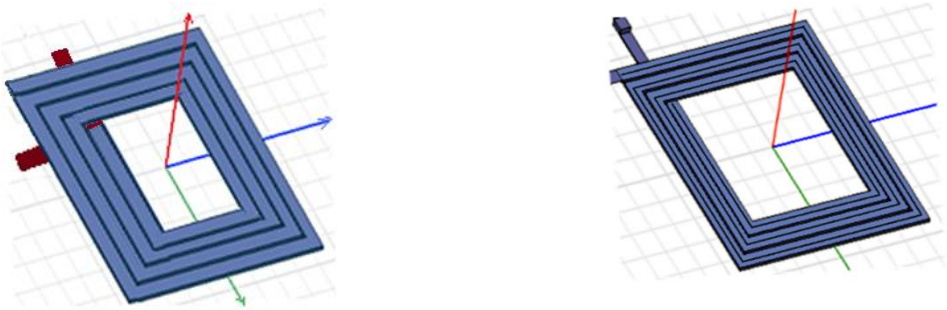
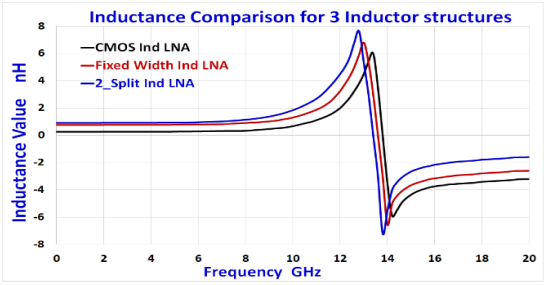


Fig. 5. 5. HFSS simulated structure of the constant width IPD Inductor and the multilayer (ML) double split IPD Inductor

Optimized planar L inductances are obtained as Ls=0.9 nH, Lg=2.4 nH, and L=3.28 nH. The inductance and quality factor comparison for two IPD spiral inductors is given in Figure 5.6. The novelty of our proposed split inductor structure is its higher inductance and higher Q compared to the other inductors. Simulation results exhibited that the double split

inductor showed 1.73 times improved inductance and 1.68 times enhanced Q value, compared to that of the constant width inductor.



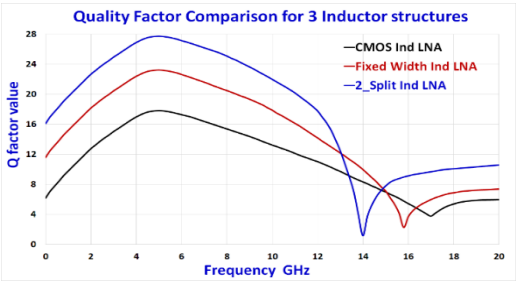


Figure 5.6. Inductance and Q factor comparison for CMOS Spiral Inductor (L_s), IPD ML Fixed width inductor L_s and IPD ML Double-split inductor L_s

Table 5.4 summarizes the performance comparison and indicates the superior performance of double split inductor compared with the reported inductors. SRF is found to be 13.4 GHz, very much suitable for the present C band 5G applications.

Table. 5.4 Performance comparison of CMOS inductor, IPD ML constant width and IPD double-split ML Inductor in 3-6 GHz C Band

Type of Inductor	Center frequency f_0 GHz	Inductance nH			Quality Factor Q			SRF f_{SRF} GHz	On chip area mm^2	Series Resistance Rs Ω		
		L_s	L_g	L	L_s	L_g	L			L_s	L_g	L
ADS CMOS Inductor (L_Model)	5.0	0.28	2.26	3.12	17.82	14.34	10.06	13.8	0.0324	50	50	50
IPD constant width inductor	5.0	0.78	2.39	3.18	23.25	20.46	15.85	13.6	0.0324	50	50	50
IPD Double Split Inductor	5.0	0.93	2.46	3.3	27.76	26.54	23.98	13.4	0.0324	50	50	50
Ref. [135]	5.0	4.9			5.8			---	---	8.5		
Ref. [40]	5.2	3.46			7.09			---	---	7.2		
Ref. [89]	5.0	10			15.12			---	---	5.0		
Ref. [63]	5.0	3.23			9			---	---	100		
Ref. [136]	5.0	0.4	3.7	2.2	7.8	22.7	20.2	---	---	---		

5.2.2 PCB fabricated IPD inductors and measurement results:

Fabrication of compact μm scale inductors on silicon substrate is not available. The only available fabrication facility is a millimeter scale PCB. Hence technology scaling is done from micrometers dimension to millimeters, but retaining the geometrical similarity. Thus, the inductor operating frequency is reduced from 5.0 GHz to 150 MHz range, for ease of fabrication. Proposed constant width and the novel double split IPD inductors are simulated and fabricated in the reduced mm scale to validate our model performance. The PCB fabricated Constant width IPD inductor and its experimental testing using network analyzer is shown in Figure 5.7.

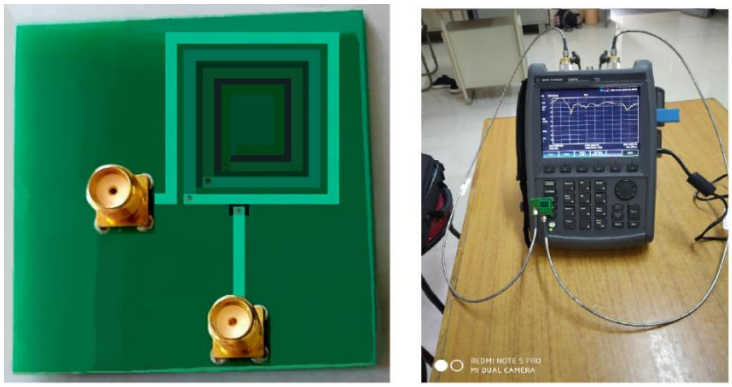


Fig. 5.7. PCB fabricated four-layer constant width Planar IPD Inductor and its experimental test setup using Agilent network analyzer.

The IPD inductors are fabricated on four-layer PCB with the FR4 substrate material. Its dielectric constant is 4.4 and area is 16 ×16mm2. The thickness of PCB is 1.60 mm with 0.15 mm copper thickness and metal layer spacing of 0.197 mm. The tested results are obtained using Agilent Technologies N9923A vector network analyser. The PCB fabricated double split IPD inductor and the corresponding measurement setup for experimentation is shown in Figure 5.8.

Performance comparison for HFSS simulated and PCB measured values of inductance and Q factors for the proposed double split inductor structure is shown in Figure 5.9.

These results clearly indicate that the experimental test results for the four-layer PCB inductor are in very good matching with the simulation results of same inductor. The inductance is 271 nH, Q_{max} is 53 at 70 MHz and SRF is 150 MHz. The error percentages are only 2.4% and 2.6% correspondingly. It is also observed that the inductance is stable from 0

to150 MHz. Hence the proposed four-layer double split IPD inductor can also successfully validate with the CMOS fabrication process at 5G bands

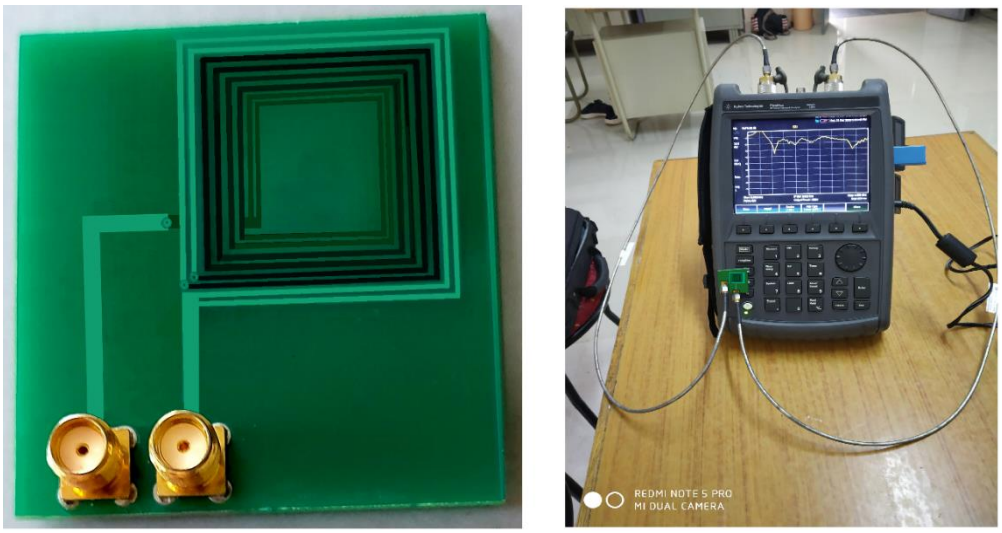


Fig. 5.8. PCB fabricated four-layer double split IPD Inductor and its experimental test setup using Agilent network analyzer.

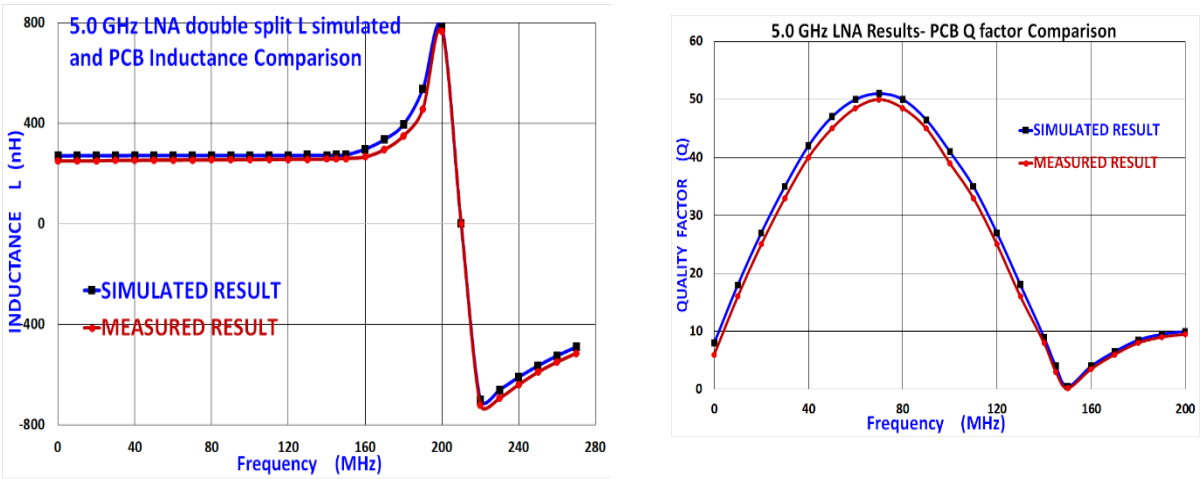


Fig. 5.9. Comparison of simulated and measured values of inductances and Q factors for the PCB fabricated four-layer double split IPD Inductor

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Table 5.5 presents the simulation and test results for the constant width and double split inductors implemented on the multilayer PCB. It is well proven that PCB measurement results are in close matching with IPD simulation results. These results proved supremacy of proposed four-layer novel split inductor to realize an easy to fabricate compact high performance on-chip inductors for 5G applications even at micrometer scale CMOS process.

Table 5.5. Simulated results vs. measured results for constant width and double split inductors

Parameter	ML constant width inductor		ML double split inductor	
	Simulation results	Measurement results	Simulation results	Measurement results
SRF f_0 (MHz)	150	155	150	153
Inductance L (nH)	250	240	270	264
Quality Factor Q	45	41	50	48
Area (mm^2)	16x16	16x16	16x16	16x16
Width W (mm)	4	4	2	2
Spacing S (mm)	2	2	1	1

5.0 GHz LNA simulation using CMOS and proposed IPD inductors:

The proposed 5.0 GHz LNA is implemented using ADS software with design specifications are given in Table 5.6.

Table 5.6. Design specifications of 5 GHz prefiltered cascode source degenerated LNA

LNA Para-meter	Center Frequency f_0 GHz	Return Loss S11 (dB)	Isola-tion S12 (dB)	Gain G (dB)	Noise Figure F (dB)	Stability Factor (K)	Input 1dB Compre-ssion P_{1in} (dB)	IIP3 (dBm)	Power Consu-mption (mW)	Supply Voltage V_{DD} (V)	On Chip Area (mm^2)
Range	5.0 (4.7-5.5)	< -20	< -20	> 25	< 2.0	2 to 5	-20	2-5	< 10	1.2 - 1.8	< 0.1

Implementation of LNA using on-chip CMOS Inductors (Ls, Lg, L):

The LNA implemented in ADS using the designed components with on-chip inductors (Ls, Lg, L) is shown in Figure 5.10.

All the inductors are simulated using same CMOS model. The simulated inductances for Ls, Lg, and L are 0.28 nH, 2.26 nH and 3.2 nH respectively. The inductors Ls, Lg, and L are also simulated in HFSS at layout level using IPD multilayer structures as shown in Figures 5.8 and 5.9. Their circuit level extraction is done by importing s2p file into ADS. The inductors Lg, Ls, and L shown in Figure 5.10, are replaced by a four-layer constant width and double split structures, respectively. The on-chip area is 180 µm × 180 µm. ADS layouts of source

degenerated 5 GHz LNA circuit using the proposed two IPD inductors are shown in Figure 5.11 and Figure 5.12.

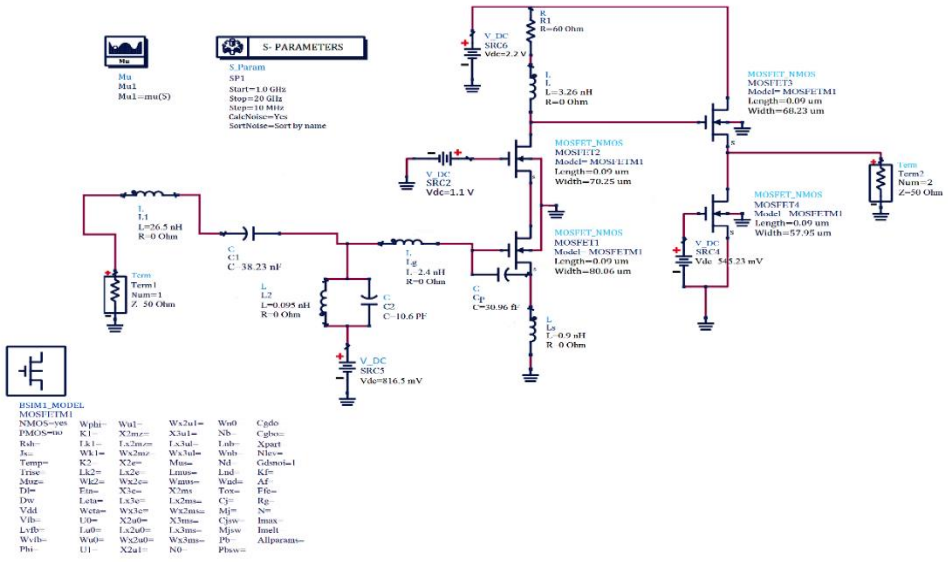

Figure. 5.10 ADS layout of the source degenerated 5.0 GHz LNA circuit using CMOS inductors.

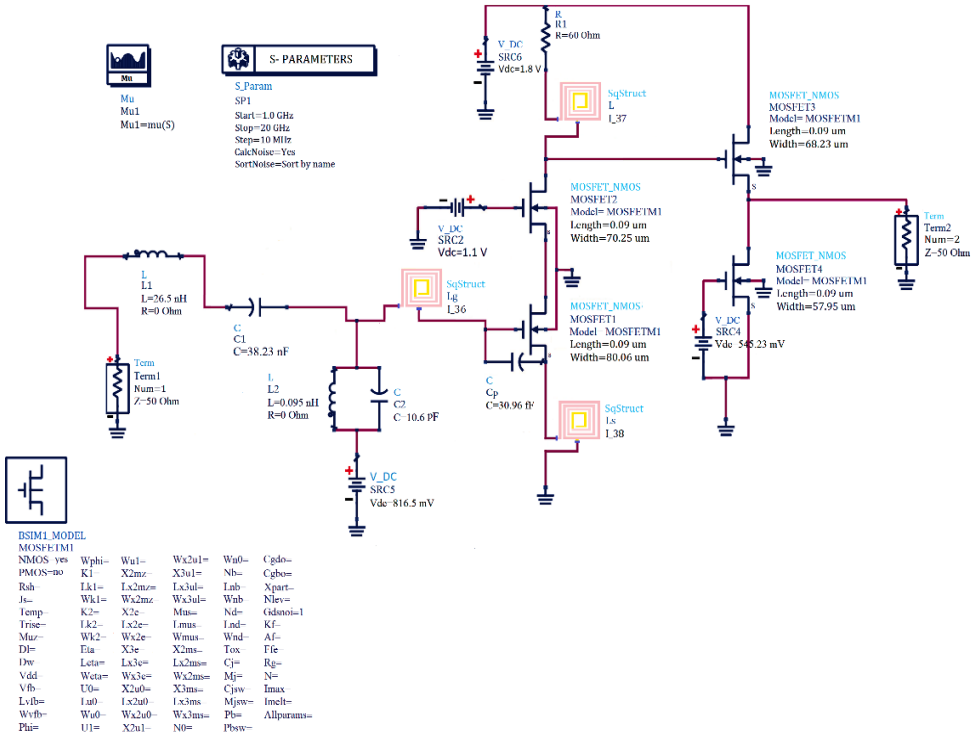

Figure 5.11. ADS layout of source degenerated 5 GHz LNA circuit using the constant width IPD inductor

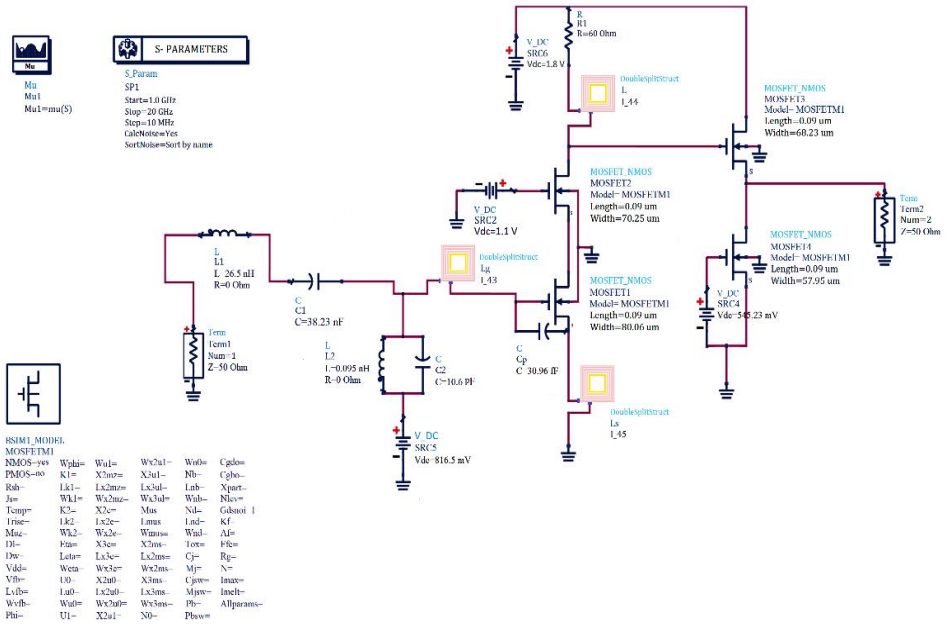

Figure 5.12. ADS layout of source degenerated 5 GHz LNA circuit using the double split IPD inductor

5.2.3 Results and Discussion

The inductance and quality factor performance of both type of IPD inductors exhibited similar response trends, like that of the ADS simulated CMOS inductor. The better performing double split IPD inductor results were shown in Figure 5.7 and Figure 5.12, at both µm and mm technology scales. The orthogonal geometry of multiple vertical metal layers produced superior inductor performances by reducing the negative mutual inductance and the series resistance (Table 4). Thus, the proposed LNA using the double split IPD inductor structure exhibited excellent input matching with very small input return loss (S_{11}) of -33.85 dB as shown in Figure 5.13. It also showed very small noise figure of 0.8 dB as shown in Figure 5.14. This is due to gate inductance (L_g) being larger than source inductor (Ls). LNA peak gain from simulation result is 28. LNA is stable throughout the range from 4.5 to 5.8 GHz as K>1, reflected in Figure 5.15. Also IIP3 is 5.6 dBm, which produced better linearity. This LNA has smaller power dissipation of 1.4 mW from 1.8 V supply voltage, as g_m is very small. Proposed LNA possessed the least occupied on chip area of 0.08 mm^2, when compared with the reported LNA literature. Its fractional bandwidth is 16% (<20%) and thus operates as a narrow band 5 GHz LNA [63].

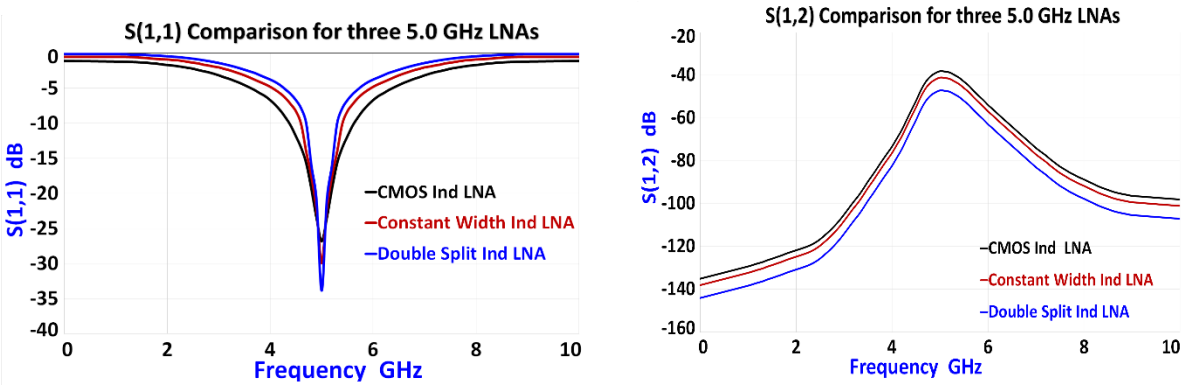

Figure 5.13. S Parameter Comparison of three proposed LNAs for input return loss S11 and reverse isolation S12

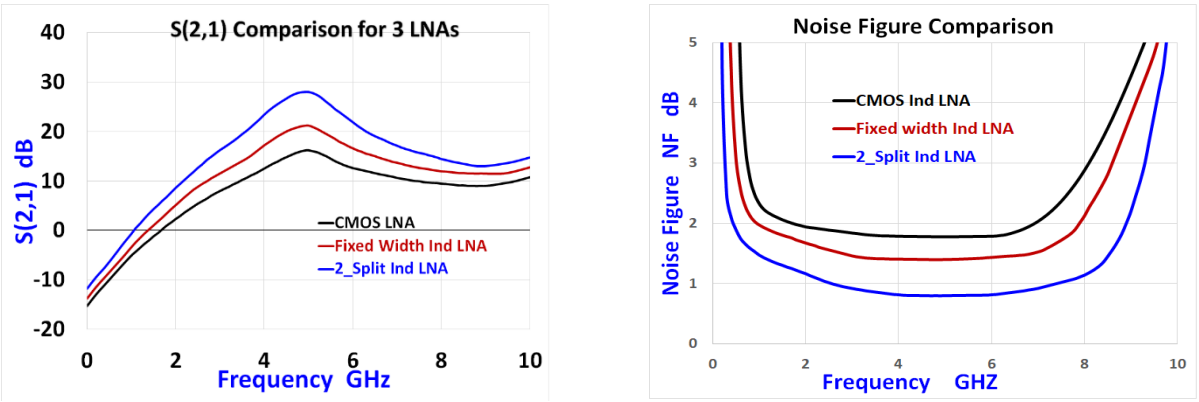

Figure 14. Gain S21 and Noise Figure comparison of the three proposed LNAs

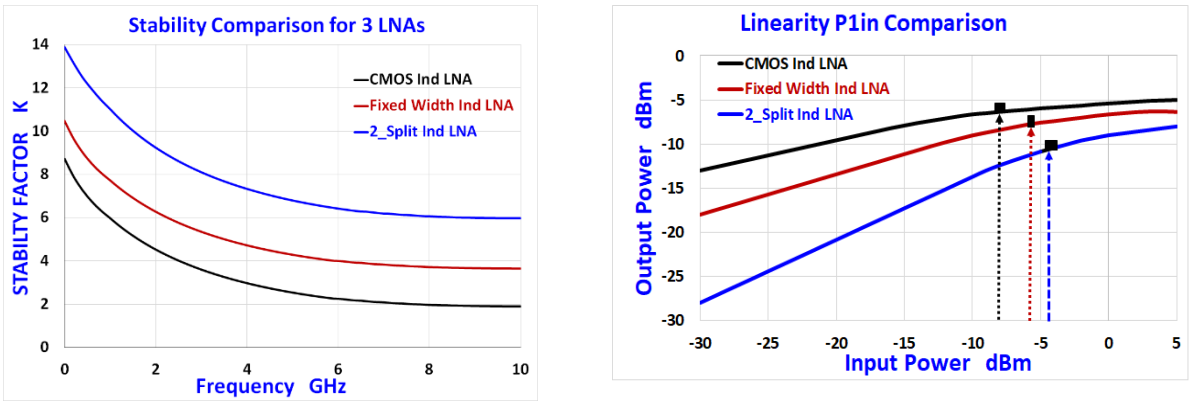

Figure 5.15. Stability K and compression point ($P1_{in}$) comparison of three proposed LNAs

The proposed novel double split (2_split) IPD inductor showed excellent inductance and quality factor improvements of 232.14% and 55.78% against the CMOS inductor. The PCB measured results are in very good agreement with simulation results, demonstrating the

superiority of proposed design. Especially the LNA using novel double split IPD inductor designed for three inductors (Ls, Lg and L) had outstanding performance by achieving high gain of 28 dB, low NF of 0.8 dB, excellent input matching of -33.85 dB, very low S12 of -45.15 dB, excellent stability of 6.08, higher IIP3 of 5.6 dBm, lower power dissipation of 1.4 mW with 1.8 V supply, and the least occupied chip space of only 0.08 mm^2. All such superior parameter enhancements clearly validate the suitability of proposed LNA for the popular Sub-6 GHz 5G wireless communications. Table 5.7 presents the performance comparison of the proposed 5.0 GHz LNAs with similar reported LNAs.

Table 5.7. Summarized performance comparison for three proposed LNAs with recent state of art LNAs @ 5.0 GHz

Technology	f_0 (GHz)	S_{11} (dB)	S_{12} (dB)	S_{21} (dB)	NF (dB)	Stability Factor (K)	1 dB $P1_{in}$ (dB)	IIP3 (dBm)	P_D (mW)	V_{DD} Supply (V)	Area (mm^2)	Topology
Proposed CMOS Ind.	**5.0**	**- 20.65**	**- 38.10**	**16**	**1.4**	**2.65**	**-7**	**2.6**	**2.5**	**1.8**	**0.08**	**NB, Cascode**
Constant Width Ind.	**5.0**	**- 29.92**	**- 42.25**	**19**	**1.2**	**3.26**	**-5**	**4.6**	**1.9**	**1.8**	**0.08**	**NB, Cascode**
Double Split IPD Ind.	**5.0**	**- 33.85**	**- 45.15**	**28**	**0.8**	**6.08**	**-4**	**5.6**	**1.4**	**1.8**	**0.08**	**NB, Cascode**
Ref. [136] **CMOS 180 nm**	**5.1-5.9**	**-**	**-**	**13.1**	**2.6**	**-**	**-**	**-7.4**	**14.2**	**-**	**0.52**	**NB, Cascode**
Ref. [133] **CMOS 65 nm**	**5.1-5.9**	**-10**	**-**	**18**	**2.4**	**-**	**-10**	**-14**	**7.2**	**-**	**0.56**	**WB, current reuse**
Ref. [137] **CMOS 140 nm**	**5.1**	**-8**	**-**	**9.6**	**1.4**	**-**	**-**	**-**	**5**	**-**	**38.4**	**NB cascade**
Ref. [138] **CMOS 180 nm**	**5.0**	**-17**	**-34**	**21.9**	**1.04**	**5**	**-4**	**9**	**0.944**	**0.9**	**-**	**NB, Cascode**
Ref. [93] **SISL pHEMT**	**5.15-5.85**	**-16**	**-35**	**23**	**0.8**	**-**	**-**	**-**	**34**	**-**	**52**	**NB, micro strip**
Ref. [139] **CMOS 180 nm**	**5.0**	**-12.2**	**13**	**-12**	**3.5**	**1.0**	**-**	**-**	**11**	**-**	**4**	**NB, ISD**
Ref. [90] **CMOS 180 nm**	**5.0**	**-33**	**28**	**-**	**1.9**	**-**	**-7**	**5**	**12**	**1.5**	**-**	**NB, cascode**
Ref. [89] **CMOS 180 nm**	**5.5**	**-16.1**	**22**	**-22**	**2.5**	**5.1**	**15.1**	**-3**	**16**	**-**	**10**	**NB, cascode**
Ref. [88] **CMOS 180 nm**	**5.2**	**-12.7**	**-14.1**	**10**	**3.37**		**-18**	**-17**	**1.68**	**1.8**	**0.6**	**WB, ESD**

5.3 Summary:

This chapter has briefly presented basic architectures and the design aspects of the key 5G RFFE building block LNA. Especially, this work focussed on using miniature IPD passive inductors to minimize the die sizes of 5G LNA. The area efficient constant width and double split IPD inductors are downscaled to millimetre level and fabricated on the FR4 PCB due to unavailability of the silicon fabrication difficulties at micrometre dimensions. The network analyser measurement results are in close concurrence with ADS simulation results. Thus, the performance of the proposed IPD inductors are successfully validated.

Chapter 6

Bandpass Filters for UWB and 5G Applications

6.1 Introduction

Today's information centric world is witnessing a massive mobile multimedia proliferation, with an explosion of smart mobile devices for wireless communication, navigation and sensing applications. This had spurred the need to design and develop very compact and yet high-performance on chip bandpass filters (BPF) for UWB and 5G RFIC and MMIC applications [140], [141]. RF BPF heavily influences the selectivity and interference rejection in any wireless receiver. High frequency miniaturized BPF design research favours IPD passive integrated Si CMOS technology due to: low power consumption; lower footprints, flexible bandwidths [142], [143]. Minimal on-chip area (OCA), lower insertion loss and high selectivity are still big challenges to design miniature BPFs [122], [144]. Passive LC resonator BPFs using Si IPD CMOS technology were proposed in recent past to suit UWB and 5G radio access applications [145], [146].

This work proposes to design and implement minimum chip space BPFs, using the proposed multilayer IPD inductors and capacitors for 5G Communications [6], [147]. Two passive BPFs are designed and simulated in HFSS at 8.2 GHz in UWB band and 25 GHz in 5G high band. To validate their results, the proposed BPFs are fabricated in mm scale on FR4 substrate PCB, due to the unavailability of CMOS fabrication facilities at μm dimensions. Both the simulation and measurement results are in very good concurrence to prove the success of proposed BPFs.

6.2 Design and implementation of miniaturized 8.2 GHz BPF

The proposed double split inductor and a planar capacitor showed excellent improvements of inductance, capacitance, quality factor and on-chip space respectively, against the nearest matching inductor in Table 6.1. A simple first order LC resonator BPF circuit is designed at 8.2 GHz. This IPD BPF demonstrated very small chip area of 0.144 mm^2. These IPD passives are fabricated by scaling down to mm scale, due to PCB fabrication difficulty at nm scale [141]. The mm level downscaled and fabricated LC resonator BPF is tested with a vector network analyser (VNA-N9923A). The PCB BPF measured results are in very good concurrence with simulation results. All these superior parameter enhancements clearly prove the high suitability of the proposed 8.2 GHz BPF for RFIC applications at 8 GHz UWB band.

6.2.1 On-chip 8.2 GHz BPF using proposed IPD Inductor and Capacitor

The presented BPF is simulated using a novel double-split multilayer IPD spiral inductor and a single layer capacitor. Square geometry is employed as it possess uniform distribution of current with easier fabrication [42]. The three-layer split inductor structure is a vertical stack of large substrate (Si), dielectric in between and 3 metal top layers. The dielectric layer (SiO2) is placed in between the top copper metal layer and 0.2 μm thick Cu/gold metal vias on the thick Substrate.

On-chip Multilayer Inductor

Typical inductor tolerance value is of several percent order, relaxing the necessity of "more accurate" expressions in practice [21]. On-chip inductors with line width variation yielded higher quality factors [36]. The total inductance of a spiral inductor is the net sum of self, positive and negative mutual inductances of a spiral structure [33]. Consider a typical three turn spiral inductor which has 12 conductor segments as indicated in Figure 6.1.

Analytical expressions to calculate self and mutual inductances for spiral inductors was discussed in section 4.2. Self-inductance L_{Self} of above three turn spiral inductor is given by

$$L_{self} == \sum_{i=1}^{12} L_i = 0.2 l_i \left\{ ln\left(\frac{2l_i}{w+t}\right) + 0.5 + \left(\frac{w+t}{3l_i}\right)\right\} \mu H \quad (6.1)$$

$$L_{Total} = L_{Self} + \sum M_{+ve} - \sum M_{-ve} \quad (6.2)$$

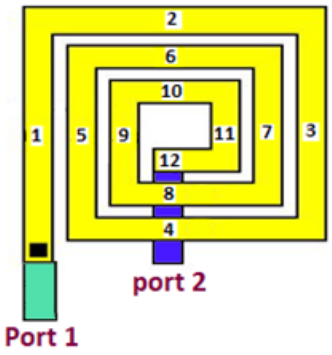

Fig. 6.1 A three turn square shaped spiral inductor with segment inductances indexed

The main objective of above layout is to obtain the desired inductance with smallest possible chip space, while keeping the SRF outside of the desired frequency band. The analytical evaluation is quite complex and cumbersome. A simple way is to calculate the inductance from the Y parameters that are found through HFSS S parameters. Inductance and Q factor are computed as

$$L = \frac{-1}{2\pi \times f_0 \times Im[Y_{11}]} \qquad Q = \frac{Im[Y_{11}]}{Re[Y_{11}]} \tag{6.3}$$

The quality factor of the inductor is found by

$$Q = \frac{\omega L_S}{R_S} \frac{1}{1+\frac{R_S}{R_p}\left\{\left(\frac{\omega L_S}{R_S}\right)^2+1\right\}} \left[1 - \frac{R_S^2(C_S+C_p)}{L_S} - \omega^2 L_S(C_S+C_p)\right] \tag{6.4}$$

The proposed three-layer IPD inductor is developed with copper conductor on a thick silicon substrate, with an outer diameter of 100 μm. The proposed novelty of splitting the conductor width by 50% all throughout, yielded large inductance (L). The proposed inductor is simulated in HFSS, to obtain values of impedance L and Q factor. These values are validated by comparing them with the values obtained by solving analytical methods. The geometry of the proposed double split IPD inductor is shown in Fig. 6.2.

The proposed double split IPD inductor has one full conductor turn per each layer. The inductance and quality factor (Q) variations are shown in Figure 6.3. The dimensions of the on-chip inductor: Conductor width, spacing and thickness are 4 μm, 2 μm and 2 μm. The spacing between adjacent layers is 2 μm and the overall occupied area is 100 x 100 μm^2. The performance of this simulated 0.18 μm CMOS IPD inductor yielded a higher Q value of 41 and an SRF of 14 GHz. Hence the proposed double-split IPD inductor is proved suitable for

miniature 8 GHz UWB and 5G ultra-wideband (5G UW) applications, primarily due to its minimum on-chip space.

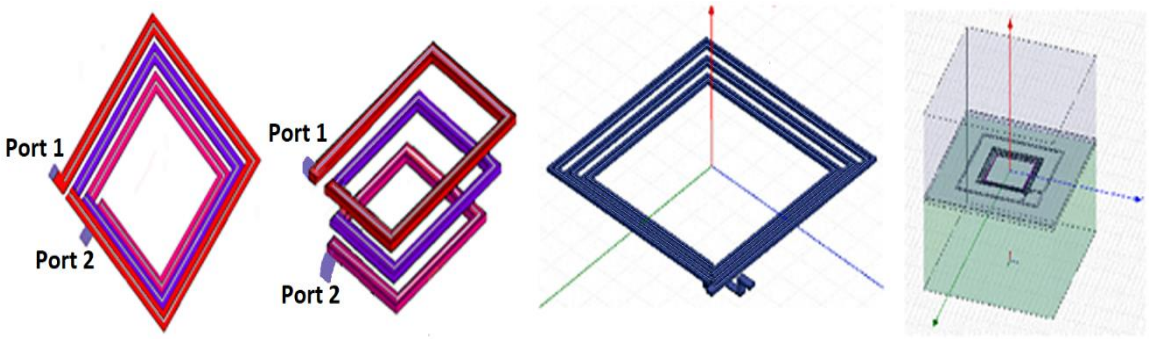

Figure 6.2. The planar, 3D, HFSS simulated split inductor and total geometry of the proposed double split three-layer IPD inductor.

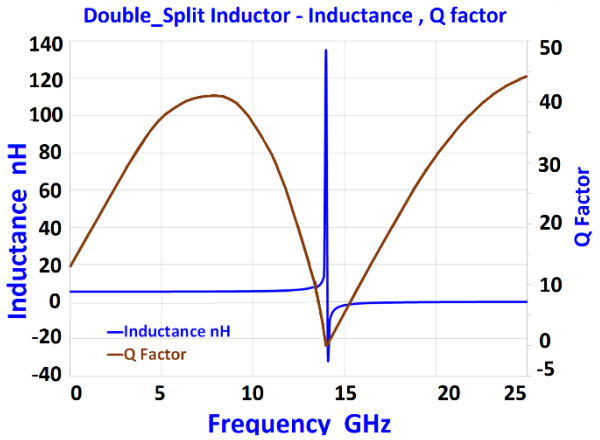

Figure 6.3. Inductance and Q Factor variation for the proposed Double Split IPD Inductor

On-chip Spiral Capacitor

A planar square spiral capacitor is chosen for ease of design, low-cost and miniaturization goal. It is simulated in HFSS for 8.2 GHz application. The conductor turns are placed in one single layer, with constant width. Inductance (L) and capacitance (C) values are influenced by material properties, conductor width, spacing and length, and also number of conductor turns. The dimensions of this two and half turn on-chip square capacitor are: Conductor width, spacing and thickness are 4 μm, 1 μm and 2 μm respectively. The overall occupied area is 50 x 50 μm^2. The capacitance C and Q values are found from S-parameters. The planar views of the on-chip spiral capacitor and its capacitance and Q factor responses are shown in Figure 6.4.

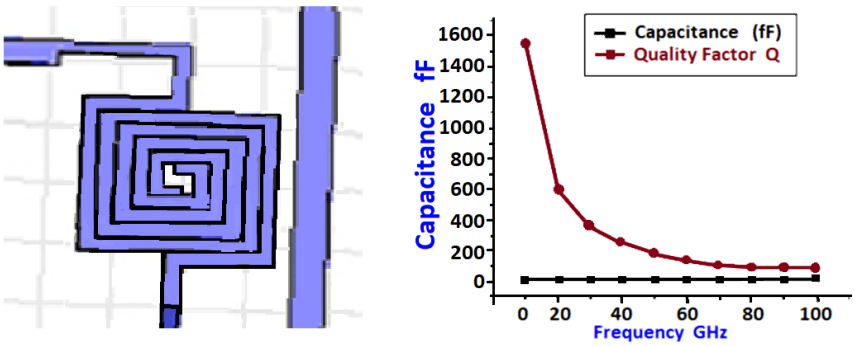

Figure 6.4. The HFSS simulated planar structure and the performance response of the two and half turn IPD Capacitor.

The capacitor had exhibited improvements in the capacitance C and Q factor values. Hence this proposed capacitor is highly suitable component for UWB and 5G RFIC applications, as it occupied very small area. Table 6.1 compares the simulation results of proposed 8.2 GHz IPD inductor and capacitors with the similar on-chip passives in literature.

Table 6.1. Performance comparison of IPD double split inductor and planar capacitor.

Type of Passive Component	Inductor			Capacitor			SRF GHz
	Inductance nH	Q_L, max	Area mm^2	Capacitance fF	Q_C	Area mm^2	
Ref. [8] 7 GHz BPF L, C	0.35	-	1.68	2.9	-	0.56	9.0
Ref. [148] 7.6 GHz IPD BPF L, C	1.623	30	0.35	7.789	70	0.25	8.36
Ref. [100] 5.8 GHz CMOS BPF L, C	0.43	5.5	0.056	3.4	-	0.056	12.5
Proposed 8.2 GHz IPD BPF L, C	**2.49**	**41**	**0.01**	**8.46**	**1745**	**0.0025**	**13.5**

The Proposed double split inductor produced an inductance value 2.49 nH and a Q_{max} of 41. Similarly, the capacitor showed a capacitance value 8.46 fF and a Qmax of 1745**.** Their superior performance is evident from above Table 1.

Circuit model and the BPF Resonator

Bandpass filter is the key performance decider for selectivity of any wireless receiver [149]. It is proposed a simple low-cost single stage LC resonator circuit to simulate and implement the proposed IPD BPF at 8.2 GHz. Circuit model and HFSS structure for the LC BPF is given in Figure 6.5. It consists of the double-split inductor and planar capacitor forming a LC resonator.

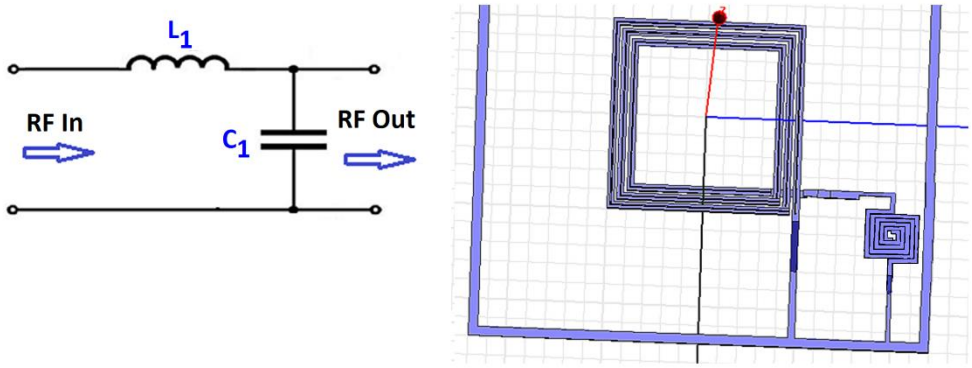

Figure 6.5. LC Resonator BPF circuit and HFSS simulated 8.2 GHz BPF.

Simulated Results for the BPF

The proposed LC BPF is simulated using the double-split multilayer IPD inductor and the single layer capacitor. The geometry and component optimization were carefully done in HFSS. Figure. 6.6 shows the return loss and insertion loss variations for proposed LC BPF.

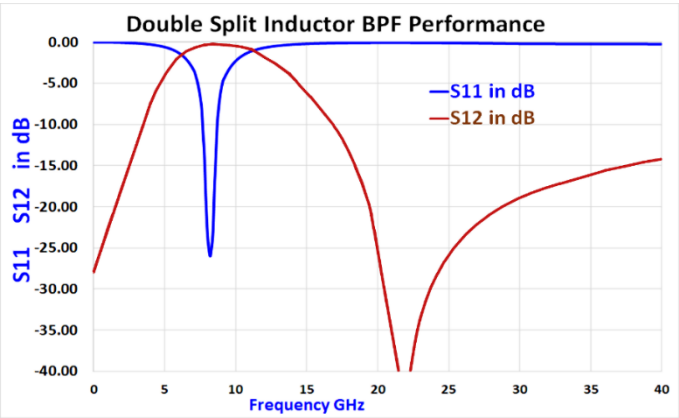

Figure. 6.6 Simulated 8.2 GHz LC BPF loss variations with double split IPD inductor

The proposed 8.2 GHz LC resonator BPF shows maximum of -26 dB return loss S_{11} and minimum insertion loss S_{21} of -0.25 dB at 8.2 GHz as shown above. These excellent results prove the best performance required by any UWB BPF. The BPF exhibits very narrow 600

MHz bandwidth from 7.85 GHz to 8.35 GHz, with center frequency of 8.2 GHz. Its loaded Q is13.68 and fractional bandwidth is 7.31%. This superior performance of BPF shown from the simulation results given in Table 6.2.

Table 6.2. Summary of the simulated 8.2 GHz IPD BPF parameters.

8.2 GHz BPF	Design Specifications	Simulation Results
Center Frequency f_0 – GHz	8.2	**8.2**
Bandwidth MHz	500	**600**
Fractional Bandwidth - %	5	**7.31**
Quality Factor Q	15	**13.68**
Return Loss S_{11} dB	< -25	**-26**
Insertion Loss S_{12} dB	< -1	**-0.25**
On Chip Area mm^2	**< 0.125**	**0.144**

The single stage LC BPF resonator simulated using the proposed novel double-split IPD inductor had produced smallest fractional bandwidth of 7.31%. The excellent insertion loss of -0.25 dB and least return loss of -41 dB will make this BPF to efficiently operate with larger selectivity. It possessed narrow bandwidth of 7% and also least occupied on-chip space of 0.144 mm^2. This narrow band response will surely satisfy the UWB spectral demands, to facilitate realizing the miniature UWB and 5G RFICs. The performance of the designed 8.2 GHz BPF is compared with similar researched BPFs around 8 GHz in Table 6.3.

Table 6.3. Performance comparisons of the designed 8.2 GHz IPD BPF.

Parameters	**f_0 GHz**	**Δf %**	**Q**	**S11 dB**	**S12 dB**	**Area mm^2**
Ref. [8]	8.0	25	4	-10.2	-1.6	15
Ref. [148]	7.656	6.89	14.5	-20	-0.3	1.667
Ref. [150]	8.0	12	8.3	-33	-0.8	0.394
Ref. [144]	6.2	15	6.7	-35	-0.5	452
Ref. [109]	6.1	13.6	7.35	-15	-0.6	152.5
Proposed BPF	**8.2**	**7.31**	**13.68**	**-26**	**- 0.25**	**0.144**

6.2.2 Implementation of the PCB based 8.2 GHz BPF

Fabrication of the double split inductor, capacitor and the IPD BPF

Fabrication facility for 180 nm scale inductors and capacitor on a silicon substrate is not available. The only available fabrication facility is a millimeter scale FR4 substrate. Hence technology scaling is done from 180 nm dimension to millimeters, but retaining the structural similarity. The proposed novel double split IPD inductor and planar capacitor are fabricated on a three-layer PCB with the FR4 substrate material. Its dielectric constant is 4.4 and the occupied PCB area is 40 ×36 mm^2. The thickness of PCB is 1.60 mm with 0.15 mm copper thickness and a metal layer spacing of 0.197 mm. The fabricated double split IPD inductor, planar capacitor and SONNET layouts for proposed 8.2 GHZ BPF PCB are shown in Fig. 6.7.

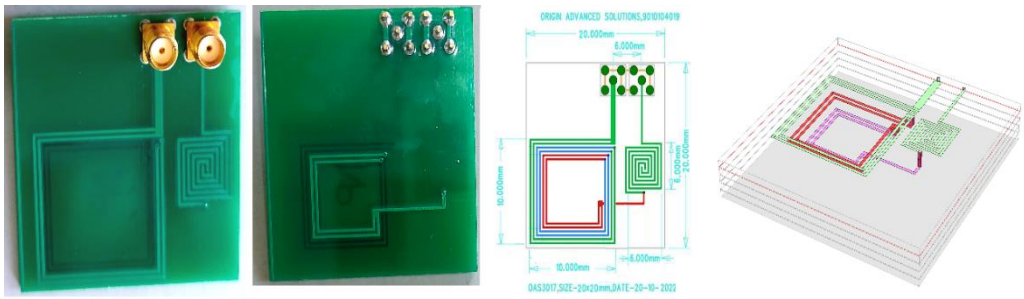

Figure 6.7. The PCB, Layout geometry and dimensional details of 8.2 GHz BPF

6.2.3 Results and Discussion

The comparison of the measured and simulated values of inductances and Q factors for the novel double split inductor structure used in 8.2 GHz PCB are shown in Figure 6.8. The corresponding test setup for experimental measurements is also are shown. The two plots clearly indicate that the measured inductances are in very good concurrence with simulated inductances about 271 nH with a maximum Q of 53 at 70 MHz with the SRF around 150 MHz.

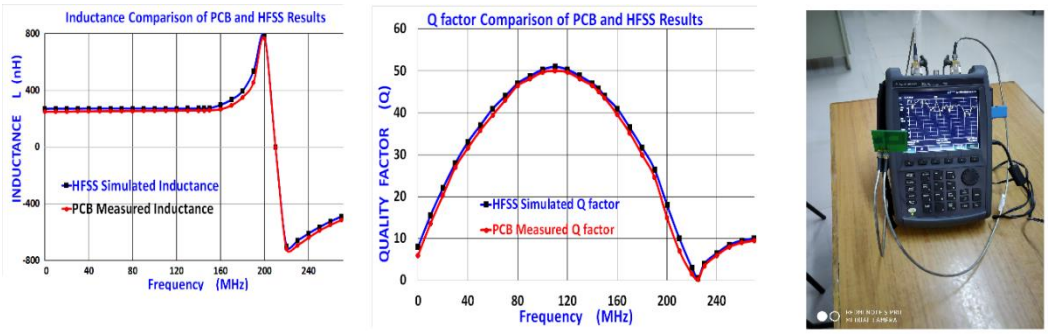

Figure 6.8. VNA measurement set up, the simulated and measured results of inductance values and Q factor values for the double split IPD inductor based PCB BPF

Table 6.4. presents the measured and simulated results for downscaled double-split inductor implemented on the three-layer PCB. It is observed that the PCB measurement results are in close concurrence with HFSS simulation results. These results prove the supremacy of the proposed novel double-split IPD inductor. Hence it is validated that proposed passive IPD inductor and capacitors can also show similar high performance for UWB and 5G applications even at 180 nm scale CMOS process.

Table 6.4. Simulated results vs. measured results for the three-layer double-split inductor.

Parameter	**Three-layer Double-split Inductor @ 120 MHz**		
	Design Specifications	Simulation Results	Measured Results
SRF f_0 (MHz)	**220**	**215**	**215**
Inductance (nH)	**270**	**271**	**264**
Q Factor Q	**50**	**48**	**46**
Chip Area (mm^2)	**10x10**	**6x6**	**6x6**
Width W (mm)	**2**	**2**	**2**
Spacing S (mm)	**1**	**1**	**1**

The HFSS simulation for mm scaled down multilayer LC IPD BPF and the measurement results for multilayer PCB BPF are validated experimentally using the Analyser VNA-N9923A as shown in Figure 6.8. The comparison of HFSS simulated results with the PCB Measurement results for the mm level scaled down PCB LC BPF using the proposed double split inductor and planar capacitor are given in Figure 6.9 and also in Table 6.5.

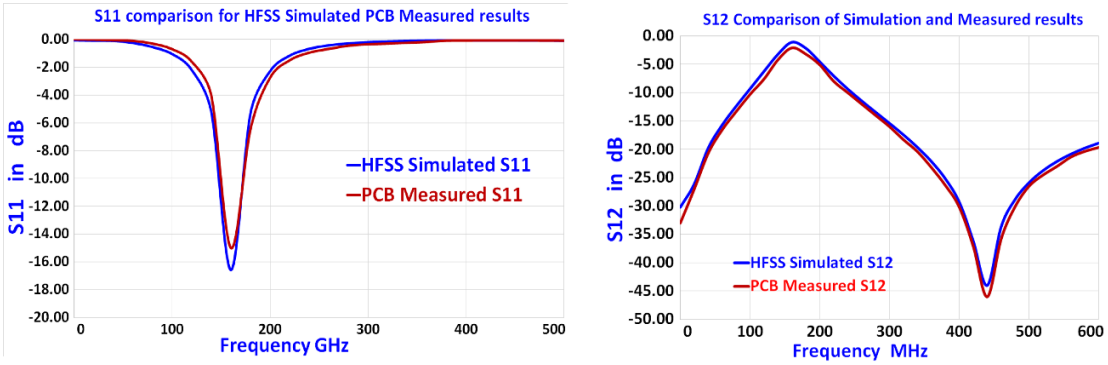

Figure 6.9. Simulation and measurement results for the proposed BPF fabricated in mm scale PCB.

Table 6.5. Performance comparison of the HFSS simulated and fabricated PCB BPFs.

Parameter	Simulation Results	Measurement Results
S_{11} - dB	**-16.58**	**-15.86**
S_{12} - dB	**-1.35**	**-1.89**
Occupied Chip Area - mm^2 (with pads)	**400**	**400**

The HFSS simulated results and fabricated three-layer PCB measured results are in close concurrency. Hence, the proposed low-cost LC BPF design can be validated even at 8.2 GHz in 180 nm CMOS process fabrication also. The proposed novel double split IPD inductor showed excellent improvements of 53% and 36.67% of inductance and quality factor respectively, against inductors of recent past. The proposed capacitor also showed capacitance and quality factor improvements of 8% and 24% respectively over the capacitors in literature.

Finally, the proposed 8.2 GHz BPF occupied least chip space of 0.144 mm^2 only. All such superior parameter enhancements coupled with least on-chip area, clearly prove that the proposed 8.2 GHz BPF design is highly suitable candidature for the UWB and 5G navigation applications. The objective to design and implement a miniaturized 5G BPF as a high performance RFIC component is achieved successfully.

6.3 Design and implementation of miniaturized 25.0 GHz BPF

A planar high-performance spiral capacitor and a multilayer spiral IPD inductor are designed to implement a simple low-cost first order LC resonator BPF circuit. This BPF design is concentrated at 25 GHz, as this band is being heavily investigated for licensed or unlicensed 5G radio access (5G NR-n258, K band) applications [94]. This 25 GHz LC resonator BPF is simulated using HFSS in 180 nm CMOS and fabricated on FR4 substrate PCB, yielded very good performance enhancements.

6.3.1 On-chip 25 GHz BPF using IPD Inductor and Capacitor

On-chip Multilayer Inductor

The proposed half turn six-layer IPD inductor is designed with a thick Si substrate and copper conductor. Its outer diameter is 100μm with a footprint of 100 μm×100 μm. The chip area is proposed very small to reduce losses to bring enhanced Q factor. The rectangular shaped planar and the 3D HFSS structures of this IPD spiral inductor are given below in Figure 6.10.

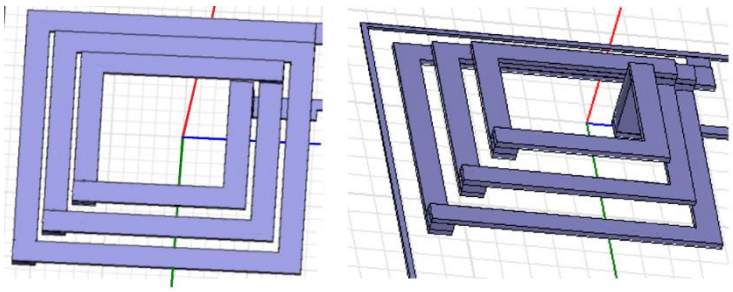

Figure 6.10. The planar and 3D views of HFSS simulated six layer 3D IPD inductor structure

Inductor topology employs one half turn in each of 6 layers. The first half conductor turn is placed in the layer 1. The next half conductor turn is placed in layer 2 and continues further, as shown above. This stacking concept is called as 3-D structure. The width, thickness and spacing for conductor paths are 4 μm, 2μm and 2μm. The layer spacing of 2μm is selected to minimize the negative mutual inductance. Inductance and Q factor variations for the proposed IPD inductor are given in Fig. 6.11.

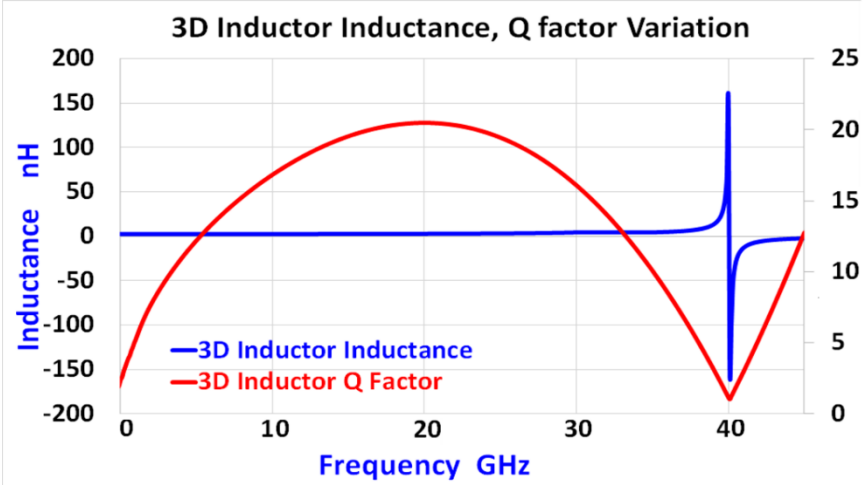

Figure 6.11. The inductance and Q factor variations of the six layer 3D IPD inductor

The inductor simulation results showed good value for Q being 22 and an SRF frequency of 40 GHz. Therefore, proposed 3D inductor is highly suitable for 5G 25 GHz band as it occupies very small chip area.

On-chip Spiral Capacitor

A planar spiral capacitor is designed and simulated in HFSS for 25 GHz 5G applications. The planar views of the on-chip spiral capacitor and its capacitance and Q factor responses are shown in Figure 6.12.

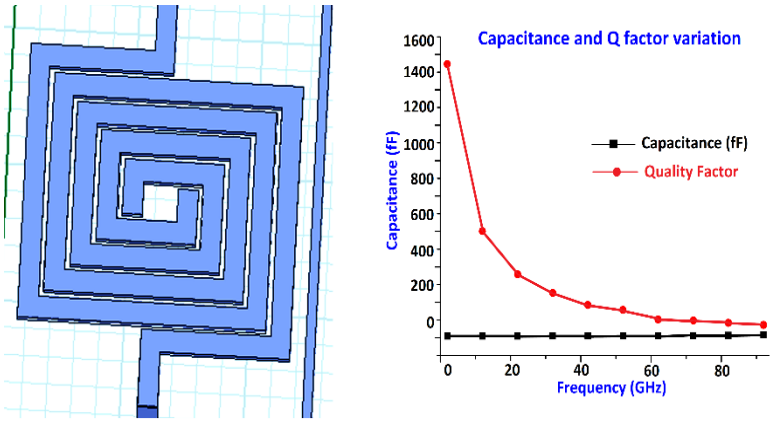

Figure 6.12. The HFSS simulated planar structure and the performance response of the one and half turn IPD Capacitor.

Onchip capacitor dimensions are: width--4 μm, thickness --2 μm and spacing --1 μm. The number of spiral turns is two and half. Net occupied chip area is only 50 x 50 μm^2. Its capacitance and Q factor values at 25GHz are 6.12 fF and 1755. Hence it definitely suits 5G radio band applications because of its minimal space occupied on the chip.

Circuit model and the BPF Resonator

It is proposed a simple low-cost single stage LC resonator circuit to simulate and implement the proposed 25 GHz IPD BPF. Circuit model and HFSS structure is given in Figure 6.13. It consists of the 3D spiral inductor and planar capacitor.

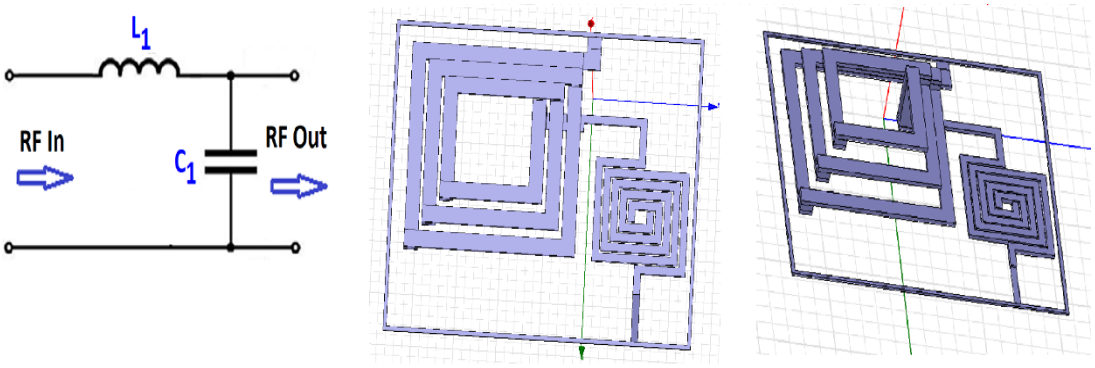

Figure 6.13 Planar view of series resonant 25 GHz BPF Circuit and its HFSS BPF structure

The HFSS simulation results for the return loss and insertion loss characteristics of this 25 GHz IPD LC BPF are shown in fig. 6.14. The performance parameters like the insertion loss S12 and return loss S11, Q factor, bandwidth, and fractional bandwidth produced by the filter simulation are summarily presented in the Table 6.6.

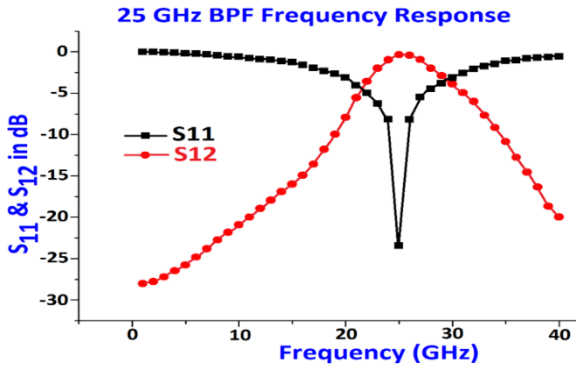

Figure. 6.14 The performance of proposed 25 GHz LC BPF in frequency range (1–40) GHz

Table 6.6. Summarized 25 GHz LC resonant BPF parameters

25 GHz BPF	Design Specifications	Simulation Results
Center Frequency F_0 - GHz	25.0	25.0
Bandwidth - MHz	1000	1500
Fractional Bandwidth - %	5.0	6.0
Quality Factor Q	15 - 20	16.67
Return Loss S_{11} - dB	< -20	- 23.43
Insertion Loss S_{12} - dB	< -1.0	- 0.36
On Chip Area - mm^2	< 0.05	0.032 (180x180 μm^2)

The performance of the designed 8.2 GHz BPF is compared with similar researched BPFs around 25 GHz in Table 6.7.

Table 6.7. Performance comparisons of the designed 25 GHz IPD BPF.

Parameters	f_0 GHz	Δf %	Q	S11 dB	S12 dB	On Chip Area mm^2
Ref. [101]	39	8	12.5	-18	-2.1	0.0256
Ref. [98]	26	4.2	11	-15	-5	0.202
Ref. [140]	28	16.3	5.1	-10	-4.5	0.8
Ref. [151]	33	18.2	5.5	-18	-2.3	2.0
Proposed BPF	**25.0**	**6.0**	**16.67**	**-23.43**	**- 0.36**	**0.032**

This low-cost single stage LC BPF resonator simulated using the proposed 6-layer IPD inductor had produced smallest fractional bandwidth of 6%, excellent insertion loss of -0.36 dB and least return loss of -23.43 dB. It possessed the least occupied on-chip space of 0.032 mm^2, many times smaller than above reported BPFs. Hence this narrow band filter will surely satisfy the stringent spectral demands to facilitate realization of miniature 5G RFICs.

6.3.2 Implementation of the PCB based 25 GHz BPF

Fabrication of the six-layer IPD inductor, capacitor and the IPD BPF

Fabrication of 180 nm scale silicon substrate inductors and capacitor is not available. The only available fabrication facility is a millimeter scale FR4 substrate. Hence technology scaling is done from 180 nm dimension to millimeters, but retaining the structural similarity [152]. The proposed on-chip passives are fabricated on a six-layer PCB. The thickness of PCB is 1.60 mm with 0.15 mm copper thickness and a metal layer spacing of 0.197 mm. The fabricated six-layer IPD inductor, planar capacitor and the SONNET layouts for the proposed 25 GHZ BPF PCB are shown in Figure 6.15.

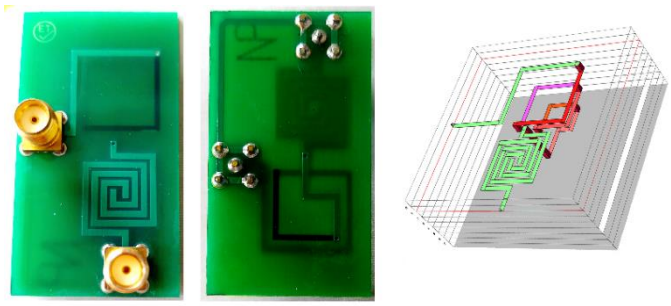

Figure 6.15. The PCB, Layout geometry and dimensional details for 25 GHz IPD LC BPF

6.3.3 Results and Discussion

Comparison of the measured and simulated inductances and Q factors for the proposed half turn six-layer inductor and planar capacitor for 25 GHz PCB BPF are shown in Fig. 6.16. The corresponding test setup for experimental measurements is also are shown. The two plots clearly indicate that the measured inductances are in very good concurrence with simulated inductances about 276 nH with a maximum Q of 53 at 70 MHz and an SRF of 150 MHz.

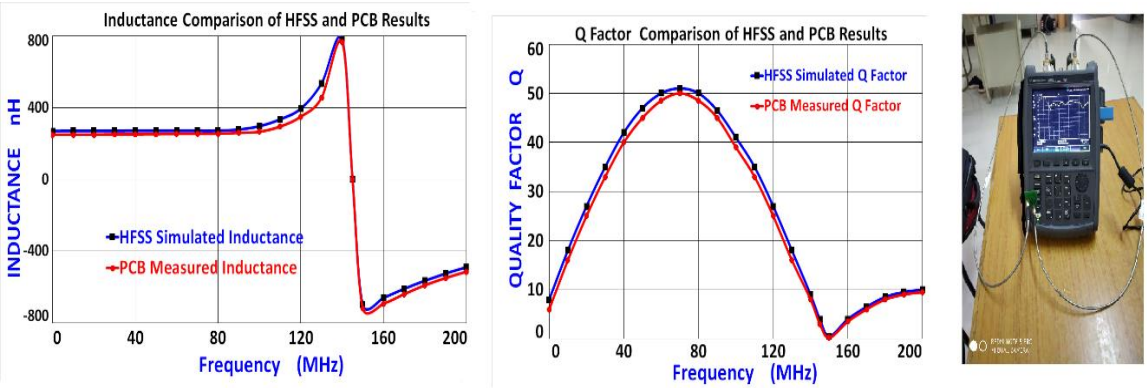

Figure 6.16. VNA measurement set up, the simulated and measured results of inductance values and Q factor values for the IPD inductor

Table 6.8. Simulated results vs. measured results for the three-layer double-split inductor.

Parameter	Six-layer IPD Inductor @ 120 MHz		
	Design Specifications	Simulation Results	Measured Results
SRF f_0 (MHz)	**150**	**155**	**155**
Inductance (nH)	**270**	**276**	**269**
Q Factor Q	**55**	**53**	**51**
Chip Area (mm^2)	**16x16**	**16x16**	**16x16**
Width W (mm)	**2**	**2**	**2**
Spacing S (mm)	**1**	**1**	**1**

The PCB measurement results are in close concurrence with HFSS simulation results as seen from Table 6.8. These results clearly prove the supremacy of proposed six layer IPD inductor. Hence it is validated that these IPD inductor and capacitors can also show similar high performance even at 180 nm scale CMOS process.

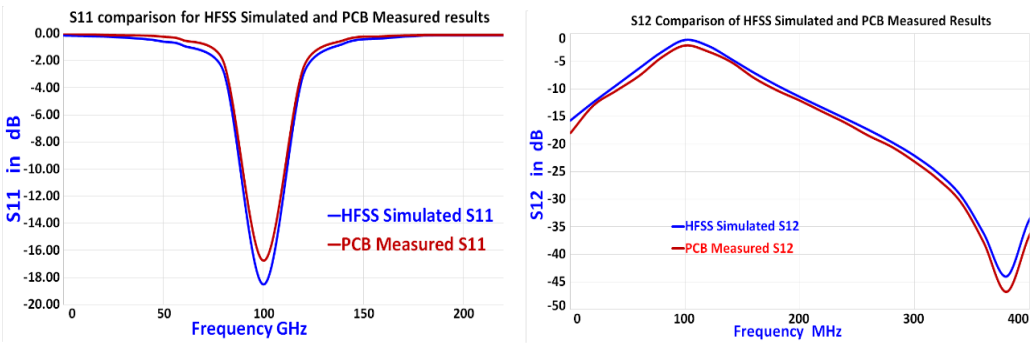

Figure 6.17. Simulation and measurement results for the proposed 25 GHz BPF fabricated in mm scale PCB.

The HFSS simulation for mm scaled down multilayer LC IPD BPF and the measurement results for multilayer PCB BPF are validated experimentally using the Analyser VNA-N9923A. The comparison of HFSS simulated results with the PCB Measurement results for the mm level scaled down PCB LC BPF are given in Figure 6.17 and also in Table 6.9.

Table 6.9. Performance comparison of the HFSS simulated and fabricated PCB BPFs.

Parameter	**Simulation Results**	**Measurement Results**
S11 - dB	**-18.58**	**-16.63**
S12 - dB	**-1.15**	**-1.29**
Occupied Chip Area - mm^2	**250**	**256**

The HFSS simulated results and fabricated three-layer PCB measured results are in close concurrency. Hence, the proposed low-cost LC BPF design can be validated even at 25 GHz in 180 nm CMOS process fabrication also. The proposed novel double split IPD inductor showed excellent improvements of 64% and 43% of inductance and quality factor respectively, against inductors of recent past. The proposed planar capacitor also showed capacitance and quality factor improvements of 10.5% and 25.8% respectively over the capacitors in literature.

Finally, the proposed 25 GHz BPF occupied least chip space of 0.032 mm^2 only. All such superior parameter enhancements, clearly prove the suitability of proposed 25 GHz BPF design for the UWB and 5G navigation applications. The objective to design and implement a miniaturized 5G BPF as a high performance RFIC component is achieved successfully.

6.4 Summary

Heavy research was done to develop high performance CMOS integrated BPFs for 5G applications. However, the chip space occupied for them is still high. This work has concentrated on developing low-cost easy to integrate BPFs using the proposed IPD on-chip passives for 8 GHz UWB and 25 GHz 5G access applications. Their HFSS simulation results and PCB measurement results had very close concurrence for all performance metrics. The double split inductor based 8.2 GHz BPF exhibited narrow 7% bandwidth, -0.25 dB insertion loss and -41 dB return loss. It had least occupied chip space of 0.144 mm^2. Similarly, the 6-layer inductor based 25 GHz LC BPF produced narrow 7% bandwidth, -0.36 dB insertion loss and -23.43 dB return loss. It had least occupied chip space of 0.032 mm^2. These tested results prove their supremacy and high suitability for UWB and 5G radio access applications.

Chapter 7

Conclusions and Future Scope

7.1 Conclusions

This thesis had concentrated on the design, simulation, fabrication and the performance analysis of miniature multilayer IPD on-chip passives to possess superior performance metrics for 5G RFIC suitability. The main objective is to minimize the occupied on-chip area for the proposed IPD passive components, as well as for proposed LNA and BPFs for UWB and 5G communications. The literature survey identifications motivated to choose the successful combination of low-cost CMOS technology and the minimum sized IPD technology to accomplish above goal. This chapter gives the summary of research work done and presents the possible future methodologies for further performance enhancements.

In the beginning, the design of multilayer IPD series stacked spiral inductor and IPD capacitor were proposed, with constant width, variable width and the novel double-split path techniques. These on-chip IPD passives have been designed and simulated in HFSS at 5G frequencies of 3.5, 4.5, 4.9, 5.0, 5.1, 5.25, 5.4, 8.2 and 25.0 GHz. All these IPD inductors attained higher inductance, higher Q factor, higher SRF and higher capacitance, against the past reported inductors and capacitors, respectively.

Chapter 2 presents an extensive literature review in this direction. It is found that, spiral inductor performance is enhanced by using the multilayer IPD process. Also observed that performance enhancements were achieved, but the on-chip area is still large. Also found that there is a great possibility to trade-off the layout parameters and process parameters to obtain their optimal combination, to reduce the die size. It is observed that the operating frequency

increases as the on-chip area decreases. Hence it is planned to focus on twin goal of component miniaturisation as well as performance improvement.

Chapter 3 discusses the optimal combination of the device layout parameters and the process control parameters to design and simulate multilayer on-chip IPD passives using spiral structure. A novel Double-split series stacked multilayer IPD inductor is proposed to further enhance the high frequency performance and minimizing the on-chip area at the same time. These inductors are developed at 3.5, 5.0, 5.1, 5.25, 8.2 and 25 GHz for 5G applications. Also, planar and multilayer passive IPD spiral capacitors are designed and implemented successfully with enhanced performances.

Chapter 4 discusses induction extraction methods to validate the simulation and experimental results for the proposed on-chip passive components. Available analytical expressions like the modified Wheeler, Greenhouse, CSA and numerical integration models are considered for this purpose. The performance comparison plots for three types of proposed IPD inductor structures (Planar, 3D and multilayer) is presented. The maximum error percentage for the integral solving model w.r.t simulation results is 1.21%, 1.6%, and 2.3% at 5 GHz frequency, for the above three inductors correspondingly. It is observed that the inductance extraction based on numerical integral method- is more accurate, as their values are closely tallied with field solver tool HFSS.

Chapter 5 has presented the design and implementation of 5G LNA using miniature IPD passive inductors for minimal die size. The proposed IPD double-split inductors are downscaled to millimetre level (low frequencies) and fabricated on the four layer and six-layer PCBs, because nm scale silicon fabrication facility is not available. These IPD inductors are successfully validated by very good concurrence between ADS simulation and PCB measurement results. These closely matched results validate that proposed inductors are best candidate as on-chip inductors even in nm scale CMOS process. The proposed 5 GHz LNA using double-split inductor produced excellent input matching with least return loss of -33.8 dB, NF of 0.8, gain of 28 dB, IIP3 of 5.6 dBm and very small chip space of 0.08 mm^2.

Chapter 6 had presented the development of easy to integrate LC resonator BPFs using the proposed IPD inductors and capacitors for 8 GHz UWB and 25 GHz 5G access applications. Like the LNA, the passives used in BPFs are also PCB fabricated and tested using VNA analyser. The 6-layer IPD inductor based 25 GHz LC BPF produced narrow 7% bandwidth, -0.36 dB insertion loss and -23.43 dB return loss. Also, its occupied area is a

meagre 0.032 mm^2. These tested results recommend their supremacy and high suitability as on-chip inductors in CMOS process, for UWB and 5G radio access applications.

The main research objective of the design, development and miniaturization of high performance 5G RFIC components like LNA and BPF have been achieved successfully. Fabricated passive components and RF circuits demonstrated excellent performance equivalence.

7.2 Future Scope

The global 5G RFFE Devices market (LNA and BPF) is anticipated to reach USD Trillion by 2030, which demand innovative 5G component development with enhanced performance metrics, and compact form factors. Efficient LNAs for broadband 5G NR FR1 Bands is mostly sought in future. The advanced 5G NR specifications coupled with new features place new burdens and create additional challenges for RFFE designers. Ultimately, new strategies and device design/development are needed to address these challenges, but these solutions must also be extremely compact, efficient and cost-effective. Rapid expansion of multi band 5G MIMO, carrier aggregation and UWB Wi-Fi 7 protocols increase filter counts, putting pressure on the RFFE designers to squeeze all the components into the agile design architecture.

There is a scope to enhance the Figure-of merits of the proposed on-chip inductors by using patterned ground shield, EBG (Electromagnetic band gap) structures, and magnetic materials as substrate. Machine Learning algorithms can be employed to select the optimum combination of the geometrical dimensions and process parameters to realize, the highly miniaturized 5G and 6G RFICs exhibiting high performance for developing SOC and SIP systems.

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List of publications

List of Published/Accepted Journals:

1. M.V. Raghunadh, N. Bheema Rao, “Design and Simulation of a Sub-6 GHz Low Loss Bandpass Filter Using Double Split Inductor for 5G Radio WLAN applications”, Springer LNEE Vol. 686, pg. 275-284, https://doi.org/10.1007/978-981-15-7031-5_26. (/journal/858448) (SCOPUS Indexed)

2. M.V. Raghunadh, N. Bheema Rao, “Design of Three Super Compact 5G Bandpass Filters with Integrated Passive Device Technology for 802.11a Wireless LAN”, GRENZE International Journal GIJET, Volume 7 Issue 1, Jan 2021, Netherlands. Scopus Indexed NOV 2021. Grenze ID: 01. GIJET.7.1.15© Grenze Scientific Society, 2021, ISSN: 2395-5295. **(Peer Reviewed)**

3. V Raghunadh Machavaram, Bheema Rao Nistala, “High Performance Double Split Series Stacked Multilayer On Chip Inductor For 5G Applications”, International Journal For Innovative Engineering Research (IJIER), Volume 2, Issue 1 (January) 2023), PP. 13-17. (Peer Reviewed).

4. Venkata Raghunadh Machavaram and Bheema Rao Nistala, Design and implementation of an ultra-compact high performance prefiltered cascode 5 GHz LNA in 90 nm CMOS using a novel double split on chip IPD inductor for 5G Communications”, SCOPE JOURNAL, Volume 13 Number 1, 2023ISSN: 11775653 (P), doi: 10.54880 (SCOPUS index)

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1. M.V. Raghunadh, N. Bheema Rao, “A compact IPD based on chip Bandpass Filter for 5G Radio Applications”, Chapter in Springer LNEE, Vol. 722, Laxminidhi T., P. Srihari Rao, VV. Mani, et al: ADVANCES IN COMMUNICATIONS, SIGNAL PROCESSING, AND VLSI,), https://doi.org/10.1007/978-981-33-4058-9_14. doi.org/10.1007/978-981-15-7031-5_26. (SCOPUS Indexed).

2. M.V. Raghunadh, N. Bheema Rao, “A High Performance Miniaturized on chip 25 GHz Narrow Bandpass Filter for 5G Radio Access Applications”, INSPEC Accession Number: 19472723, IEEE doi: 10.1109/ICRAIE47735.2019.9037771., (SCOPUS Indexed)

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4. M.V. Raghunadh, N. Bheema Rao, “A compact low loss on-chip bandpass filter for 5GnR N79 radio front end using IPD technology”, Springer Nature 2020, Modelling, Simulation and Intelligent Computing, N. Goel et al (eds.), Springer LNEE, Vol. 659, https://doi.org/10.1007/978-981-15-4775-1_50. (SCOPUS Indexed)

5. M.V. Raghunadh, N. Bheema Rao, “Design and Simulation of a Sub-6 GHz Low Loss Bandpass Filter Using Double Split Inductor for 5G Radio WLAN applications”, Springer Lecture Notes in Electrical Engineering Volume 686, pg. 275-284, https://doi.org/10.1007/978-981-15-7031-5_26. (Published: 23 (/publisher/10.1007/journal/858448). (SCOPUS Indexed).

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3. M.V. Raghunadh, N. Bheema Rao, “A High Performance Miniaturized on chip 25 GHz Narrow Bandpass Filter for 5G Radio Access Applications”, 4th IEEE Intern. Conf. ICRAIE 2019, University of Kedah, Malaysia, 27 - 29 NOV. 2019. (SCOPUS Indexed)

4. M.V. Raghunadh, N. Bheema Rao, “A Compact Low Loss on chip BPF for 5G Radio Front End using IPD Technology”, IEEE International Conference, ISMAC 2019, SCAD Institute of Technology, Coimbatore, 12-14 DEC 2019. (SCOPUS Indexed)

5. M.V. Raghunadh, N. Bheema Rao, “A compact low loss on-chip bandpass filter for 5GnR N79 radio front end using IPD technology”, Springer International Conference, MOSICOM 2020, BITS Dubai, 29-31 JAN 2020, Springer Nature 2020, Modelling, Simulation and Intelligent Computing. (SCOPUS Indexed)

6. M.V. Raghunadh, N. Bheema Rao, “Design and Simulation of a Sub-6 GHz Low Loss Bandpass Filter Using Double Split Inductor for 5G Radio WLAN applications”, Springer International Conference, ESIC 2020, National Institute of Technology, Itanagar, 4-6 MAR 2020. (SCOPUS Indexed)

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