An Efficient Architecture for H.264 Intra Prediction Mode Decision Algorithm

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Abstract— **The paper presents an intra prediction hardware architecture where it exploits parallelism in predicting the pixels and pipelining is implemented during the calculation of the cost function. The parallelism feature includes an optimized data path which calculates only 24 unique pixel values and the former are assigned to the current macro block depending on the equations for different modes as defined in the H.264 standard. Synthesis results confirmed that the proposed architecture is able to process SD 1280x720P @ 50 fps when operating at 57 MHz for ASIC platforms.**

Keywords-intra prediction, spatial redundancy, modedecision, video frame,macro block,optimized data path.

I. Introduction

H.264 audio video coding is the latest standard which is the result of the collaboration between ISO/IEC MPEG and the ITU-T video coding experts group. Intra prediction feature of H.264 reduces the spatial redundancy present in a frame, which adds to the improvement in compression ratio. Current macro block in a video frame is either predicted by the neighboring pixels of the neighboring macro blocks within the same frame (intra prediction to reduce spatial redundancy) or by a macro block in the previous frame (inter prediction to reduce temporal redundancy).The first frame is always intra predicted because it has no reference frame. Intra prediction serves as an alternative when the motion estimator fails to provide a good matching block which results in high residue and low encoding quality.

II. H.264 Intra Frame Prediction

H.264 intra prediction uses the spatial correlation with neighboring macro blocks i.e. a current macro block is predicted from the neighboring pixels of the previously reconstructed macro blocks. In H.264 intra prediction is performed for two different block sizes (4x4 and 16 x 16) for luma prediction and 8x8 block for chroma prediction. Each 4x4 block is predicted using nine directional prediction modes and the 16x16 and 8x8 blocks are predicted using 4 modes (dc, horizontal ,vertical ,plane).

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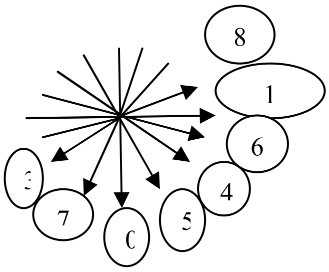
A. Algorithm

For the luma component of the macro block each frame is divided into a number of 16x16 macro blocks and prediction is performed for one 16x16 macro block and sixteen 4x4 macro blocks. A mode decision algorithm is used to compare the predictions of 4x 4 and 16 x16 blocks and select the best luma prediction mode based on the cost function of the macro block.

M	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**
I	a	b	c	d				
J	e	f	g	H				
K	I	j	k	l				
L	m	n	o	p				

Fig 1.a. 4x4 luma block and neighboring pixels



Mode0:vertical mode1:horizontal
Mode2:dc mode3:diagonal down left
Mode4:diagonal down right mode5:vertical right
Mode 6:horizontal down mode7:horizontal up
Mode 8:vertical left

Fig 1.b. Prediction modes and directions

The pixels A to M in Fig 1.a. belong to the neighboring blocks and are assumed to be already encoded and reconstructed and thus available for the prediction of the next macro block.

The pixels a to p represented in Fig 1.a are the current macro block pixels which are later predicted using the thirteen reconstructed pixels of the neighboring macro blocks. Each 4x4 macro block generates 16 predicted pixels and each 16x16 macro block generates 256 predicted pixels using some or all of the neighboring pixels. The best predicted mode is assigned to the mode with minimum sum of absolute differences(sad). For a 16 x 16 macro block the best predicted mode is generated as follows:

If the sad value of the 16 x16 macro block is less than the sum of sixteen 4x4 blocks sad values then the best predicted mode is one of the four directional modes for 16x16 macro block.

(16x 16 sad)<sum of 16(4x4 sad's)

Else the best predicted mode is one of the nine directional modes for each of the sixteen 4x4 macro blocks based on the cost function of each directional mode(considering the minimum sad value).

Fig 1.b. represents the eight directional modes for the 4x4 macro block .Each pixel is assigned values for all the modes depending on the equations as defined in the standard [1].

B. *Architecture*

Intra prediction process consists of the following steps :
1) prediction equation generation for each pixel in the macro block , based on the neighboring samples
2) calculate the cost of each predicted mode and to choose the block with minimum cost based on the sum of absolute differences.[2]

Flow diagram:

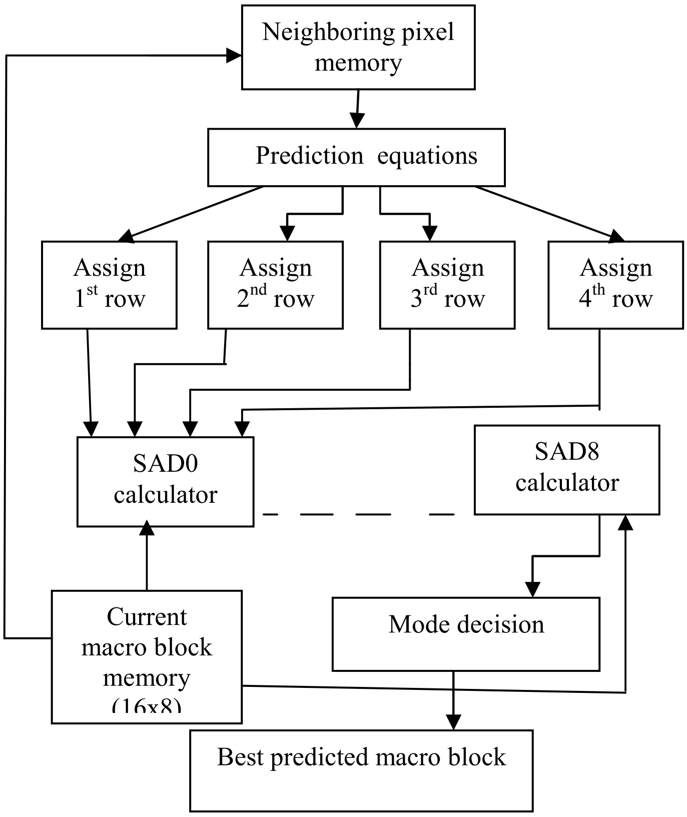


Fig. 3. Architectural flow diagram of intra prediction process for a 4x4 macro block.

1. *Neighboring pixel memory*

The first block in the flow diagram is the neighboring pixel memory as shown in Fig 3. The neighboring pixels belong to the previous macro block and are used to predict the current macro block pixel values. All the thirteen pixels are required for the prediction of nine modes. So all the pixels are read from the memory in one clock cycle(4 pixels in one clock cycle). Every time a new macro block is predicted, the left and the top most original samples replace the neighboring pixels memory. The prediction scheme uses original pixels instead of reconstructed pixels as boundary pixels for next predictions [3].

2. *Prediction equations*

The standard formulae for different modes are transformed into pixel processing equations specified in h.264 standard draft[1]. Usually for horizontal and vertical modes the neighboring reconstructed pixel values are directly assigned(Here the neighboring original pixel values are assigned.). DC mode is a simple average of the neighboring reconstructed pixels(Here it is the simple average of the neighboring original pixels.). For the remaining six modes all the equations are sorted to find out the unique set of equations which result in 24 equations only [2].The computational order of these equations is rearranged to achieve an optimized data path[2].

Unique equations:

D1<=L ; D2<=(K+L+L+L+2); D3<=(K+L+1);

D4<=(J+K+K+L+2);D5<=(J+K+1);D6<=(I+J+J+K+2);

D7<=(I+J+1); D8<=(M+I+I+J+2); D9<=(M+I+1);

D10<=(A+M+M+I+2); D11<=(M+A+1);

D12<=(M+A+A+B+2); D13<=(A+B+1);

D14<=(A+B+B+C+2); D15<=(B+C+1);

D16<=(B+C+C+D+2); D17<=(C+D+1);

D18<=(C+D+D+E+2); D19<=(D+E+1);

D20<=(D+E+E+F+2);D21<=(E+F+1);

D22<=(E+F+F+G+2);D23<=(F+G+G+H);

D24<=(G+H+H+H+2);

3. *Assignment*

In this block four pixels in a row are assigned the prediction equations in one clock cycle for all the nine prediction modes. The assignment is done in parallel for each row and hence the 4x4 macro block is predicted in one clock cycle for all the nine modes.

4. *Current macro block memory*

The current macro block memory of Fig 3. stores the 16 original pixels of the 4x4 luma block .These pixels are necessary for the mode decision as the predicted pixels are subtracted form the original pixels to generate the sad based on which the best predicted mode is generated. The neighboring pixels of the current block are updated to the neighboring pixel memory for every block since we are considering the original pixels instead of reconstructed pixels for prediction [3].

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5. SAD calculator

There are nine SAD calculators working in parallel for each mode which subtract the four predicted samples from the current block samples and the differences are accumulated to generate the SAD for one predicted 4x4 block line. The SAD calculator works in pipeline with the assignment block, so that after the first predicted line is generated the SAD calculator starts to accumulate during the next 4 clock cycles[2]. As shown in Fig 4 the calculator has an additional adder for accumulation.

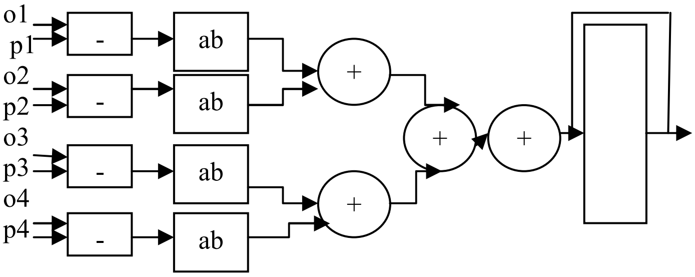

Fig. 4. Sad calculations for a 4x4 macro block

In the Fig 4. o1, o2, o3, o4 represent the current macro block original pixels and p1, p2, p3, p4 represent the predicted pixels.

6. Mode decision

The mode decision is the last block. As shown in Fig 3 nine sad values are generated. Mode decision gives the best predicted mode based on the minimum SAD value. The best predicted block is actually reconstructed (transformed ,quantized , inverse quantized and inverse transformed) to get the exact predicted block whose boundary pixels are used as neighboring pixels for the next macro block. However an open loop intra prediction scheme is proposed to use original pixels instead of reconstructed pixels as reconstructed pixel values are close to original pixel values [3].

III. IMPLEMENTATION

The architecture is defined in a hardware description language (VHDL) and synthesized by the Synopsys Design Compiler with 0.18µm standard cell library. The design contains a total of 36k gates (The gate count is restricted as such because of the use of the optimized data path and non implementation of the reconstruction path.) and runs at a frequency of 57 MHz . The design specifications are shown in Table 1.

Table1: Design Specifications

Algorithm	Fast mode algorithm	
Memory requirement	(16x8) 16 pixels of each 8 bits to store the current macro block and the predicted macro block.	(13 x8) 13 pixels of each 8 bits to save the neighboring pixels for each block.
technology	0.18 µm	
Gate count	36K	
Maximum frequency	57 MHz	
Throughput (4x4 macro block)	193 kMb/s	

The performance analysis after compilation using the Synopsys Design Compiler is given in Table 2.

Table 2: Performance Analysis

Critical path	16.87µm
Critical path clk period	17.20ns
Operating conditions	5V
Total dynamic power	440.02 µW

IV. EVALUATION AND RESULTS

The proposed architecture supports all baseline /main intra prediction features calculates the SAD cost and decides the best mode for 4x4 MB. This architecture does not implement the reconstruction path (T/Q/IQ/IT). The whole process for 4x4 MB in this architecture takes 9 clock cycles.

The architecture takes three clock cycles to read the neighboring pixel values from the memory (four pixels in one clock cycle)and one clock cycle for the parallel assignment of each row of pixels(all the nine modes are assigned in one clock cycle for each row of pixels) as discussed in section II.B.3 and four clock cycles for the SAD calculation as discussed in section II.B.4 and one clock cycle for the mode decision. So a 4x4 macro block takes 9 clock cycles for its prediction. A 16x16 macro block on a whole takes 300 clock cycles for its prediction without considering the pixel reconstruction.

In each of the previous approaches either a parallel or a pipeline approach with reconstruction is considered. In our approach all the features of the previous works are included without reconstruction and it is observed that use of both parallel and pipeline approaches enhances the speed of processing with a reduction in area .

For full mode intra prediction one macro block takes 300 clock cycles considering 4 pixel parallelism. Therefore at 57 MHz the approach can process 193798 Mb/s i.e. 1920 x1080 (HD 1080p) at 24 fps(frames per second). The required frequency for 1280 x720 pixel resolution is 27.6 MHz for 30 fps . So at 57 MHz for 1280x720 resolution 54 frames per second can be processed. This implies that the above design specifications are applicable for (1280x720) application.

Table 3 shows the comparison of our approach with other designs. The operating frequency of our approach is 57 MHz Which processes 193 KMb/s using parallelism feature and this approach is observed to be faster(1.6 time faster with respect to [7] and 1.16 times faster with respect to [8]).

Table 3:Comparison with previous designs

Design feature	Our approach	[7]	[8]
Maximum operating frequency	57MHz 1280x720@54 fps	125MHz 1280x720@ 30 fps	61MHz 1280x720 @30fps
Maximum throughput	193 KMb/s	115KMb/s	165KMb/s
Pixel parallelism	4 pixel	4 pixel	8 pixel

V. CONCLUSIONS

The proposed hardware architecture for h.264 /AVC intra prediction supports all the intra modes, calculates the blocks costs and decides the best intra 4x4 predicted macro block. Synthesis results confirmed that the proposed architecture is able to process HD 1080p at 24 fps when operating at 57 MHz for ASIC platforms and is observed to be faster than the previous works.

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