Zero Voltage Switching Floating Output High Gain Interleaved DC-DC Converter

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***Abstract*—This paper proposes a non-isolated high efficiency high gain DC-DC converter using zero voltage switching for renewable/green power supply system with photovoltaic (PV) cell or fuel cell. Proposed topology uses interleaved structure of boost converter with winding coupled inductor to offer higher power handling capacity, lower ripple for input current and lower semiconductor voltage stress. The power switches are turned on using zero voltage switching (ZVS) and the switch turned off voltage spike is suppressed by using boost type active clamping technique. This enables the use of lower voltage and $R_{DS\text{-}ON}$ MOSFET switch with low switching and conduction losses. Diode turn off current falling rate is controlled by the leakage inductance of coupled inductor and by choosing proper value of leakage inductance, diodes can be turned off using zero current switching (ZCS) and diode reverse recovery problem is alleviated. The significant feature of the proposed topology includes continuous input/output current operation with rid of extreme duty cycle and limited reactive components size. The proposed converter operating modes are analyzed and theoretical waveforms are validated through simulation results.**

Keywords— soft switching technique, interleave, winding coupled inductor, active clamping circuit.

I. INTRODUCTION

High performance and high step up dc-dc converters are required in many applications such as electric vehicles, uninterrupted power supplies (UPS) and high intensity discharge (HID) lamp for automobile head lamps. Nowadays, more and more renewable energy sources are promoted around the world, such as photovoltaic (PV) cells and fuel cells which are characterized by low voltage, high current output and have strict current ripple requirement [1, 2, 3]. Consequently, as an important interface, dc-dc converter with high step up gain, low input current ripple, high efficiency and nonisolation is required [4].

Though conventional boost converter can theoretically give infinite voltage gain when duty cycle is close to one, in practice the actual output of boost converter is restricted due to current stress of main switch and diode, diode reverse recovery problem and parasitic elements associated with the converter components which do not allow high voltage gain. Also it is not feasible to use conventional boost converter with high duty cycle due to great variations in output voltage caused by small variation in the duty cycle, leading the boost converter to instability and slow transient response. Hence the boost converter with higher duty cycle degrades the overall conversion efficiency and also increases the electromagnetic interference (EMI). Therefore, practically realizable voltage gain of basic boost converter is not higher than six [5, 6].

To improve the conversion efficiency and achieve high step up voltage gain, many topologies based on the boost converter have been proposed [7]; the cascaded boost converter proposed in [8] requires two sets of power devices, a magnetic core and control circuits; they thus increase voltage gain at the expense of the higher cost and complex control circuit. The converters using switched capacitors technique with high step up gain presented in [9] is suitable for low power applications, since current stress on semiconductor devices is high because of the charging characteristics of capacitor.

Therefore, to provide high gain voltage support as well as reduction in switching voltage stress, coupled inductors are utilized in [10, 11]. It also efficiently alleviates the reverse recovery problem of the output voltage. However the energy associated with the leakage inductance of the coupled inductor is large due to large input current. Hence, the main switch experiences a high voltage spike across the switch during turn off due to occurrence of resonance between leakage inductor and output capacitor of the switch. This necessitates the use of higher voltage range MOSFET switches and snubber circuit with added cost of converter and also degrades the overall efficiency. Also the single phase single switch topology leads to large input current ripple and limited power handling capacity [12].

Therefore, in this paper, the design of a new high efficiency high voltage gain interleaved dc-dc converter is presented. In this structure, winding coupled inductor is used as both forward and flyback converter. This thus allows the use of switched capacitor technique by charging the capacitor when the coupled inductor behaves like forward converter and discharge in series with the secondary of the coupled inductor when the coupled inductor behaves like flyback converter.

Active clamping technique is used to achieve zero voltage switching (ZVS) turn on of main switches. The leakage inductance of coupled inductor controls the diode turn off current falling rate, turning them off by zero current switching (ZCS) and alleviating the reverse recovery problem. Hence the switching losses are reduced greatly which enable us to go for higher switching frequency and smaller reactive components. The voltage rating of the components is lower than half of the output voltage which adds to reduced cost and smaller size of converter. The active clamping circuit is not connected to input

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side but the output side [13] which eliminates the need of extra power diode and clamping capacitor as compared to converter in [14]. The two interleaved converter modules are operated with interleaved PWM technique, i.e. gating pulses is shifted by half of switching time period (T).

II. PROPOSED TOPOLOGY

Fig. 1 shows the circuit configuration of the proposed ZVS floating output interleaved input converter. This converter uses boost converter with interleaved input structure and voltage doubler switched capacitor with coupled inductor to achieve high gain and lower input current ripple [12, 15]. ZVS is realized in this converter by using boost type active clamping technique which also recycles the leakage energy of inductor. All the four active switches are turned on using ZVS while the rectifiers are turned off using ZCS. Besides, instead of using two winding coupled inductors, three winding coupled inductors [16] are used with one of the secondary windings of each inductor cross coupled with another phase of interleaved structure. The coupling method of winding coupled inductors is marked by a dark circle and an open circle as shown in Fig.1.

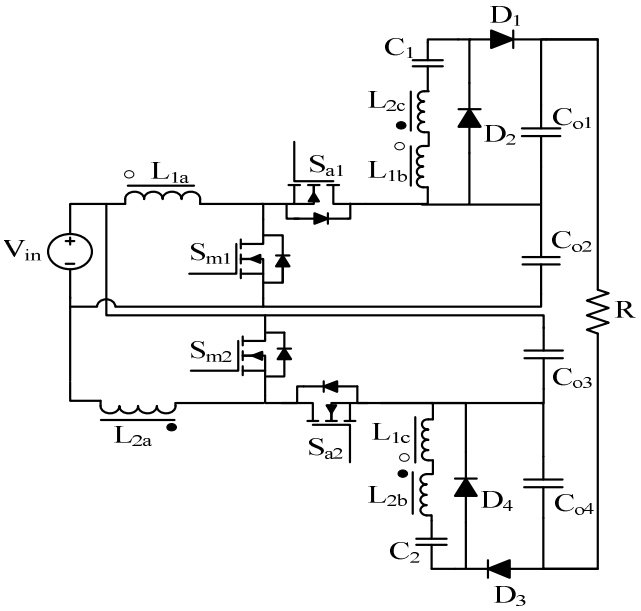

Fig. 1. Circuit configuration of proposed converter.

III. OPERATION PRINCIPLE

Fig.2 shows the equivalent circuit configuration of the proposed converter. L_{m1} and L_{m2} are magnetizing inductors. L_{lk1} and L_{lk2} are leakage inductors. S_{a1} and S_{a2} are the active clamp or auxiliary switches. Gating pulses of auxiliary switches are complementary to that of main switches. C_s is the parallel combination of output capacitance main and auxiliary switch. C_s and L_{lk} are resonant to achieve ZVS turn on of S_m and S_a.

The following assumptions are made to simplify the circuit analysis.

1. $L_m >> L_{lk}$.
2. Winding coupled inductor turns ratio $N = n_2/n_1$.

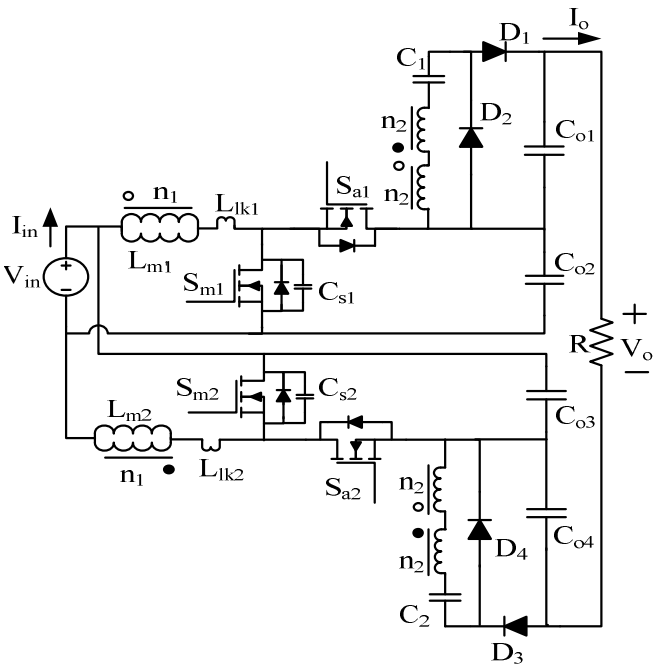

Fig. 2. Simplified circuit model of proposed converter.

3. All the switches are ideal except their output capacitance and anti-parallel diode.
4. Capacitor voltages V_{co1}, V_{co2}, V_{co3}, V_{co4}, V_{c1} and V_{c2} are almost constant.

Fig. 3 gives the time sequence of key waveforms of the proposed converter. There are 20 stages in one switching period. Due to symmetry of switching waveforms, only ten stages are analyzed and their corresponding equivalent circuit for each operation stage is highlighted as shown in Fig. 4.

When switch S_m is closed, the voltage across magnetizing inductor is given by

$$V_{lm} = k * V_{in} \tag{1}$$

Where,

$$k = \frac{L_m}{L_m + L_{lk}}$$

The $L_{lk} << L_m$ hence k can be considered unity to simplify the analysis.

Mode1. [t0 - t1]: In this mode, the main switches S_{m1}, S_{m2} are closed and the auxiliary switches S_{a1} and S_{a2} are off. The diodes D_1, D_2, D_3 and D_4 are reverse biased, hence no current flows through secondary winding. Magnetizing and leakage inductor are charged linearly by the DC input source V_{in}.

$$i_{Lm1}(t) = \frac{V_{in}}{L_{m1} + L_{lk1}} t + I_{Lm1}(t0) \tag{2}$$

$$i_{Lm2}(t) = \frac{V_{in}}{L_{m2} + L_{lk2}} t + I_{Lm2}(t0) + I_o \tag{3}$$

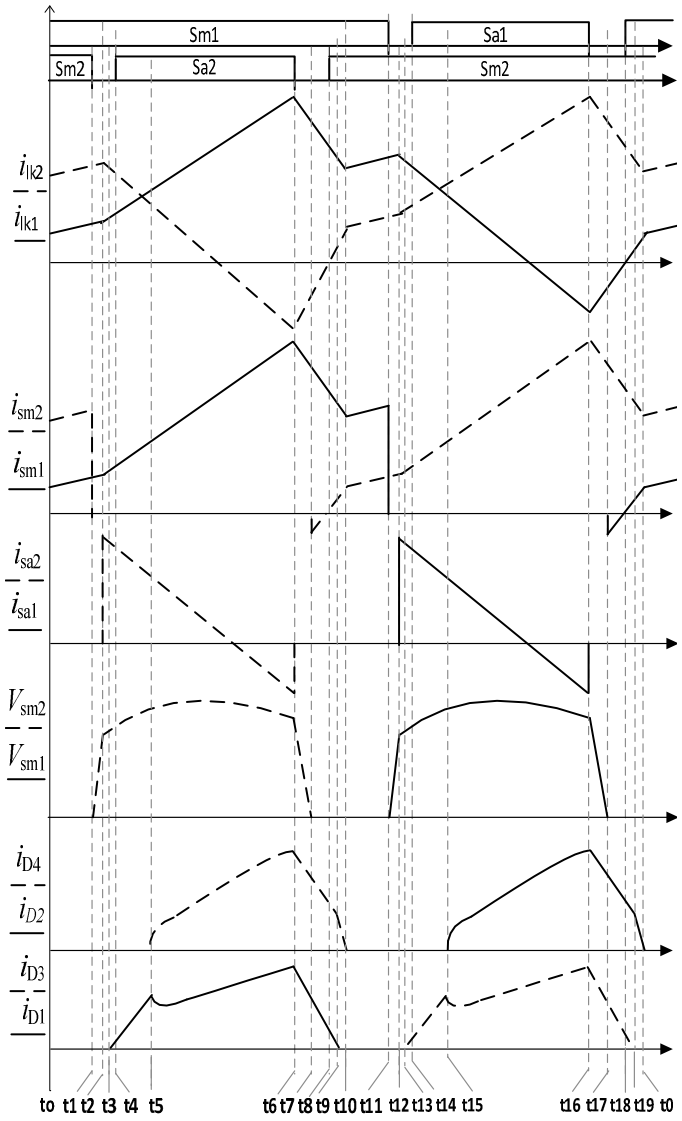

Fig. 3. Key waveforms of proposed converter.

Mode 2. [t1 – t2]: In Fig. 3 at t1, main switch S_{m2} is turned off. Since the value of C_{s2} is very small it is charged linearly by magnetizing current which is also equal to current through the leakage inductor. In this mode, V_{cs2} is less than V_{co3} and anti-parallel diode of S_{a2} is off. Due to the presence of parallel capacitor C_{s2}, the main switch S_{m2} is turned off using ZVS condition. The capacitor voltage is expressed as

$$V_{cs2} = \frac{\left[I_{Lm2}(t1) + I_o\right]}{C_{s2}}(t - t1) \tag{4}$$

Mode 3. [t2- t3]: At t2, C_{s2} is charged to V_{co3}, since C_{s2} is smaller all the magnetizing current is diverted to C_{o3} resulting in anti-parallel diode of S_{a2} to start conduct; consequently the voltage appearing across the magnetizing inductance V_{Lm2} decreases as V_{co3} increases according to voltage divider action

$$V_{Lm2} = \frac{L_{m2}}{L_{m2} + L_{lk2}}(V_{in} - V_{co3}) \tag{5}$$

The switch S_{a2} should be turned on before i_{lk2} becomes negative for ZVS turn on.

Mode 4. [t3 – t4]: At t3, the magnetizing voltage V_{Lm2} is sufficient to induce coupled inductor secondary voltage to forward bias D_1. Diode D_4 is still reverse biased. Current through leakage inductor i_{lk} is a summation of the magnetizing current i_{Lm} and reflected current i_{D1} through output diode D_1.

$$I_{lk1}(t) = i_{Lm1}(t) + N * i_{D1}(t) \tag{6}$$

$$I_{lk2}(t) = i_{Lm2}(t) - N * i_{D1}(t) + I_o \tag{7}$$

Mode 5. [t4 – t5]: At t4, the auxiliary switch S_{a2} is turned on using ZVS condition because its anti-parallel diode is on. Current paths are same as that of previous mode except S_{a2} is conducting instead of its body diode.

Mode 6. [t5 – t6]: At t5, the V_{Lm2} is decreased to the value sufficient to forward bias D_4. As the rate of change of secondary current is controlled by leakage inductance and the voltage across it which is almost constant, the rate at which diode current i_{D1} was increasing in earlier mode is divided between i_{D1} and i_{D4} equally in this mode.

Mode 7. [t6 – t7]: Auxiliary switch S_{a2} is turned off at t6 terminating resonant circuit between i_{lk2} and C_{o3}, and switch capacitance C_{s2} starts discharging in a resonant manner due to the leakage inductance L_{lk2}. The auxiliary switch is turned off using ZVS condition due to C_{s2}.

Mode 8. [t7 – t8]: At t7, capacitor C_{s2} is discharged completely and anti-parallel diode of S_{m2} prevent C_{s2} voltage from going negative. In this interval S_{m2} can be turned on using ZVS condition.

Mode 9. [t8 – t9]: S_{m2} is on, and the transformer secondary current decreases as leakage inductor current i_{lk} increases. At t9 the current through diode D_1 decreases to zero while D_4 is still conducting. The falling rate of diode current is controlled by the leakage inductance and the voltage across it which can be expressed as

$$\frac{di_{D1}(t)}{dt} + \frac{di_{D4}(t)}{dt} \approx \frac{V_{co3}}{2N * L_{lk}} \tag{8}$$

From (8) it is observed that, as the secondary current is divided between two diodes, a small value of leakage inductance is sufficient to achieve ZCS turn off of diodes.

Mode 10. [t9 – t10]: At t9, the transformer secondary current is flowing through D_4 which is decreasing linearly and almost at twice rate as compared to previous mode. At t10, secondary current decreases to zero and D_4 is reverse biased, and the current through L_{lk2} is equal to current through L_{m2}.

$$\frac{di_{D4}(t)}{dt} \approx \frac{V_{co3}}{2N * L_{lk}} \tag{9}$$

A similar operation is repeated in the remaining ten stages of a switching period. Hence the input current ripple has a frequency twice that of the operating frequency. Fig. 4 shows the equivalent circuit of each operating mode in the half cycle of switching period.

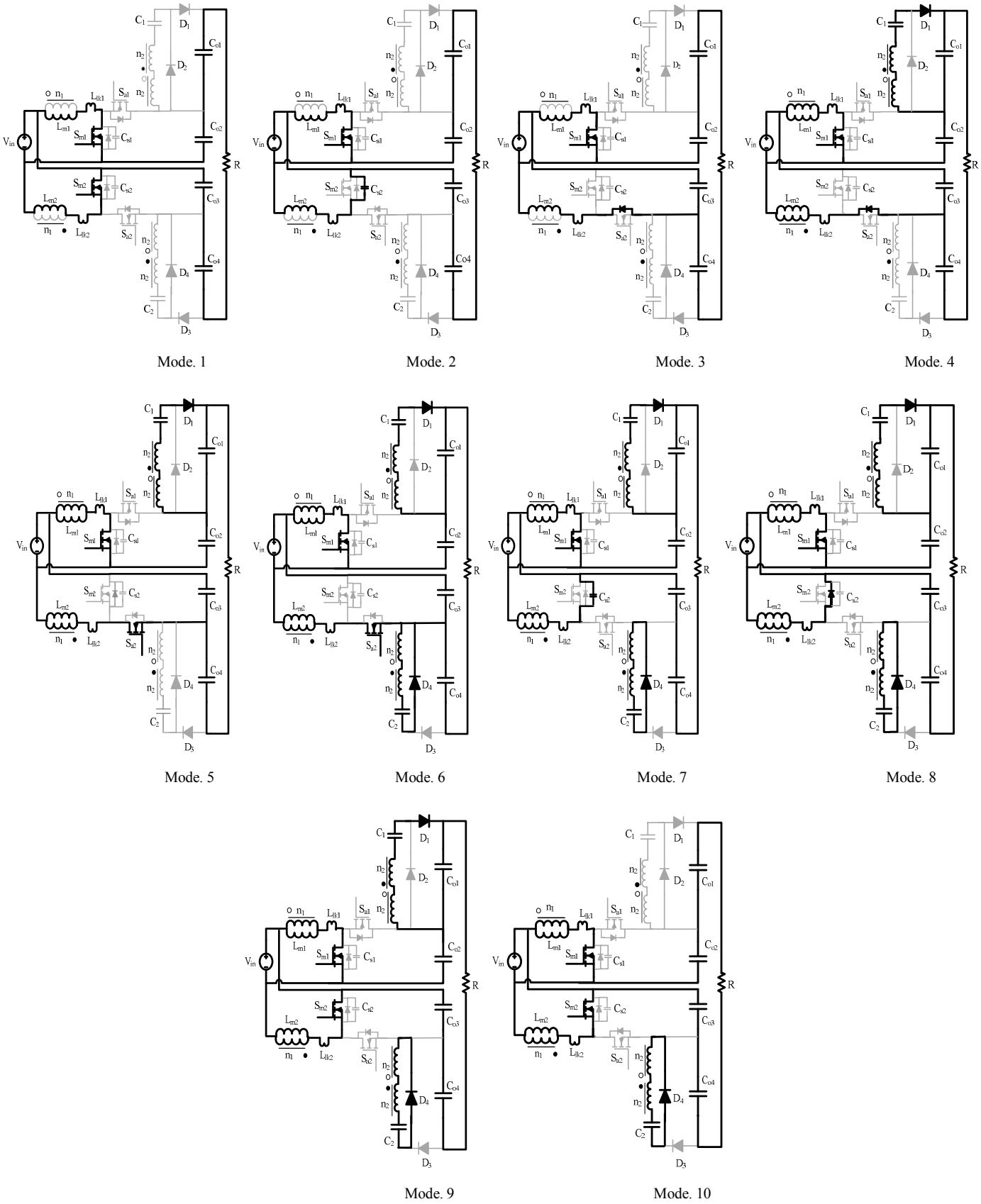

Fig. 4. Operating modes of proposed converter for half of a switching period.

IV. CHARACTERISTICS

A. DC Conversion Ratio

The output voltage at any given moment can be expressed as

$$V_o = V_{co1} + V_{co2} + V_{co3} + V_{co4} - V_{in} \quad (10)$$

By applying voltage-second balance to the magnetizing inductor and ignoring the effect of leakage inductance, the voltages V_{co1}, V_{co2}, V_{co3} and V_{co4} are given by

$$V_{co2} = V_{co3} = \frac{1}{1-D} V_{in} \quad (11)$$

$$V_{c1} = V_{c2} = N * V_{co3} \quad (12)$$

$$V_{co1} = V_{co4} = 2N * V_{co3} \quad (13)$$

Substituting (11) and (13) in (10) the expression for voltage gain can be obtained as presented in (14)

$$M = \frac{V_o}{V_{in}} = \frac{4N + 1 + D}{1-D} \quad (14)$$

From (14) the voltage gain is large even if N=1. So, moderate duty cycle (D) can be used in proposed converter as compared to conventional boost converter which can reduce input and output current ripple.

B. Voltage Stress of Semiconductor Devices

The filter capacitor of a conventional boost converter itself acts as clamping capacitor, which is large enough to suppress the switch turned off voltage spike.

The normalized voltage stress of active devices is given by

$$V_{sm1,\,stress} = V_{sm2,\,stress} = V_{co2} = \frac{1}{1-D} V_{in} \quad (15)$$

$$V_{sa1,\,stress} = V_{sa2,\,stress} = V_{co2} = \frac{1}{1-D} V_{in} \quad (16)$$

From (15) and (16) voltage stress of power switches can be controlled by controlling duty cycle and transformer turns ratio. So, low voltage and high performance device can be used to reduce switching and conduction losses.

C. Soft Switching Performance

Because of auxiliary active clamping circuit all semiconductor switches are turned on with ZVS due to which switching losses are reduced. Also, all the diodes are turned off using ZCS due to presence of leakage inductance in coupled inductor.

$$\frac{di_{D1}(t)}{dt} + \frac{di_{D4}(t)}{dt} \approx \frac{V_{co3}}{2N * L_{lk}} \quad (17)$$

$$\frac{di_{D2}(t)}{dt} + \frac{di_{D3}(t)}{dt} \approx \frac{V_{co2}}{2N * L_{lk}} \quad (18)$$

V. SYSTEM DESIGN

A. Turns Ratio Selection

In this converter, turns ratio selection determines the voltage stress of power devices, diode current falling rate and duty ratio. Hence turns ratio should be chosen carefully. We assumed that the effective maximum duty cycle of S_{m1} and S_{m2} is D_{max}. The turns ratio for minimum input voltage V_{in} is given by

$$N = \frac{n2}{n1} = \frac{1}{4}\left[\frac{V_o}{V_{in,\,\min}}(1 - D_{\max}) - 1 - D_{\max}\right] \quad (19)$$

B. Power Device Selection

Assuming the clamp capacitor is large enough to suppress the voltage spike caused by the leakage inductor, the voltage stress of main and auxiliary switch is given by

$$V_{sm1,\,stress} = V_{sm2,\,stress} = \frac{1}{1-D} V_{in} \quad (20)$$

$$V_{sa1,\,stress} = V_{sa2,\,stress} = \frac{1}{1-D} V_{in} \quad (21)$$

From (20) & (21) voltage stress of switches is less than one fourth of output voltage, which makes it suitable for high performance switch with low voltage stress and R_{DS_ON}.

C. Leakage Inductor Design

The leakage inductance has a direct influence on the diode turn off current falling rate; as the diode reverse recovery charge depends on diode turn off current falling rate, L_{lk} is selected to alleviate diode reverse recovery problem.

$$L_{lk} \approx \frac{V_{co3}}{2N\left[\frac{di_D(t)}{dt}\right]} \quad (22)$$

Where, $i_D(t)$ is the total secondary current flowing through output diodes.

From (22) a small amount of leakage inductor is also sufficient to keep lower current falling rate.

D. Capacitors Selection

In this converter, the clamp capacitor and filter capacitor of conventional boost are integrated. This capacitor is designed to minimize output voltage ripple and suppress the switch turn off voltage spike and to avoid excessive resonant ringing [17] due to parasitic elements of the power switch and transformer. A capacitor of minimum capacitance value is selected so that one half of resonant period exceeds the maximum turn off time of main switches, which is given by

$$C_{o2} \geq C_{o3} \geq \frac{(1 - D_{\min})T^2}{\pi^2 * L_{lk}} \quad (23)$$

VI. Simulation Results

The proposed converter is developed in MATLAB/ SIMULINK environment for 600 watt capacity to verify the theoretical waveforms using simulation results in steady state condition. The nominal input voltage is 40V and the minimum and maximum input voltages are 35 and 48V respectively. Output voltage is maintained constant at 400V. Selected switching frequency is 100 kHz and duty cycle (D) range is from 0.5 to 0.65. It should be noted that to achieve ZVS on main switches, the duty cycle must be greater than 0.5. Table I summarizes the converter specifications and the values of components used. Key simulated waveforms of proposed converter at full load condition are shown.

TABLE I. Converter Specifications

Parameters	***Value***
Input voltage (Vin)	35 - 48V
Output voltage (Vo)	400V
Output power (Po)	600 W
Switching frequency (f)	100 kHz
Transformer turns ratio (N)	0.7
Capacitors: Co1,Co4	30µF
Co2, Co3	17µF
C_1, C_2	20uF
Cs	1.5nF
Magnetizing inductance (L_m)	47µH
Leakage inductance, L_{lk}	1.15µH

Fig. 5 gives the simulated output voltage waveforms of proposed DC-DC converter. The voltage across capacitors C_{o1}, C_{o4} and C_{o2}, C_{o3} are equal. The difference between V_{co1}, V_{co4} and V_{co2}, V_{co3} depends on the transformer turns ratio selected. The voltage across individual capacitors is less than half of output voltage which will reduce the size and cost of capacitors.

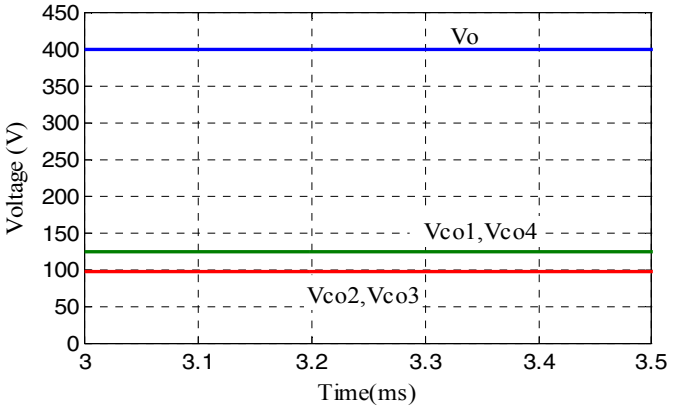

Fig. 5. Output voltage and voltages across each capacitor at full load.

Fig. 6 and 7 give the gate voltages and drain voltages of active switches S_m and S_a. Before switches S_m and S_a are gated, the drain to source voltages are brought down to zero. Thus all semiconductor switches are turned on with ZVS. Also voltage stress of switches is smaller as compared to output voltage, which ensures that high performance switch with low $R_{DS\text{-}ON}$ can be used. Hence both switching and conduction losses are reduced which improves the efficiency of converter. The voltage spike across the switch is clamped effectively by output capacitors and the energy associated with leakage inductor is recovered.

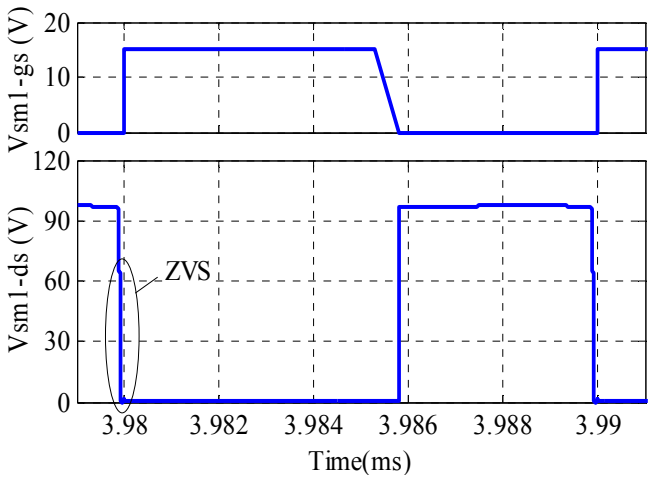

Fig. 6. Simulated results of gate voltage and drain voltage of switch S_{m1} at full load condition.

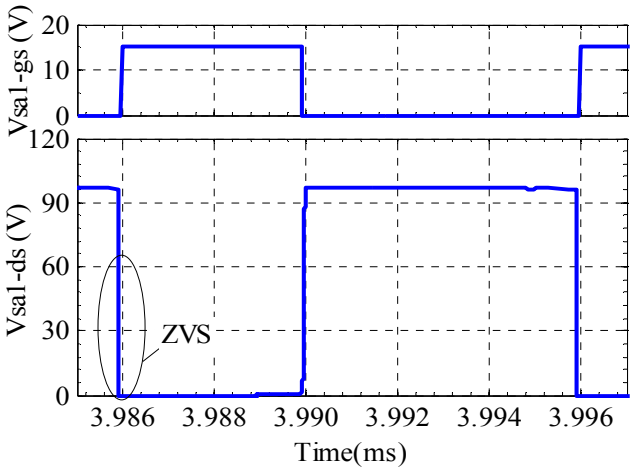

Fig. 7. Simulated results of gate voltage and drain voltage of switch S_{a1} at full load condition.

Fig. 8 shows simulated waveforms of gate voltage $V_{sa2,gs}$ and diode currents i_{D1} and i_{D4}. Diode currents are decreased to zero with lower di_D/dt and the diodes are turned off at ZCS. Hence diode reverse recovery problem is alleviated.

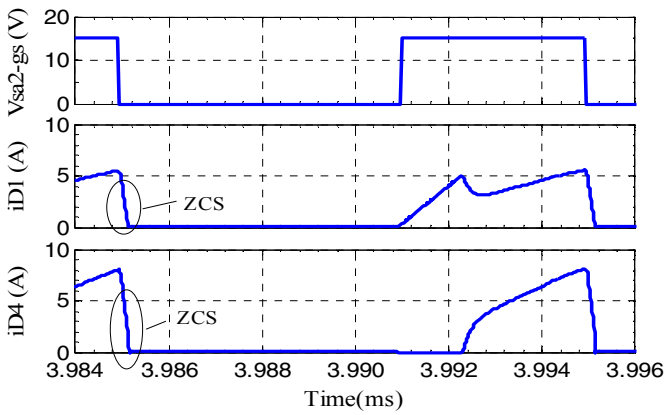

Fig. 8. Simulated waveforms of $V_{sa2,gs}$ and diode currents i_{D1} and i_{D4} at full load condition.

Fig. 9 shows the gate voltage $V_{sm,gs}$ and current flowing through main switch S_m and auxiliary switch S_a.

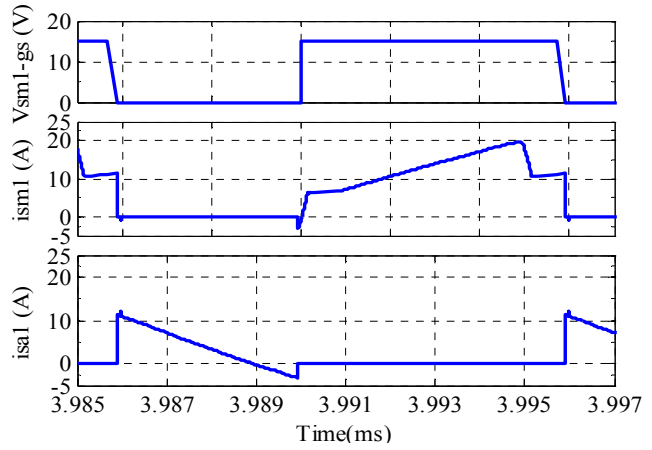

Fig. 9. Simulated waveforms of $V_{sm1,gs}$, switch current i_{sm1} and current i_{sa1} at full load condition.

Fig. 10 shows the current flowing in the leakage inductance L_{lk1} and L_{lk2}. From simulated waveforms, it is observed that these currents are approximately mirror replica of each other which results in input current ripple cancellation. Thus interleaved structure helps in reducing input current ripple as well as increasing converter power level.

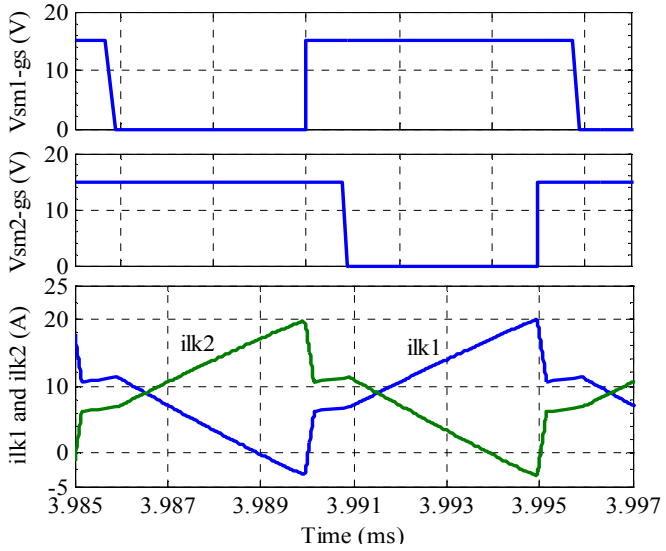

Fig. 10. Simulated waveforms of $V_{sm1,gs}$, $V_{sm2,gs}$, current i_{lk1} and i_{lk2} at full load condition.

VII. CONCLUSION

This paper introduces a novel interleaved input floating output boost converter with winding coupled inductor which offers large voltage gain with the help of proper turn ratio selection. Consequently the power switch has lower voltage stress. Power switch turn off voltage spike is suppressed and leakage energy of coupled inductor is released in output through clamp capacitors. In addition, all semiconductor devices are switched on/off using soft switching scheme i.e. power switches are turned on by using ZVS while all diodes are turned off using ZCS improving the efficiency. Interleaved structure with winding coupled inductor adds lower input and output current ripples, smaller size of reactive component and turns ratio which in turn reduces the overall size and cost of converter.

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