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A Fully On Chip Slewrate Enhanced Low Drop-out Voltage Regulator

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Abstract

A novel full on-chip low dropout linear regulator is presented in this paper. This LDO is designed with single ended OTA for better gain which in order improves load regulation. A self-biased comparator is used to detect the change in regulated voltage and increase slew rate at output of error amplifier. A frequency compensation scheme is used which maintains LDO stable over entire load current range i.e. 0-100mA. The load regulation of the LDO is 0.68 μv/mA .The overshoot/ undershoots in the output voltage under the extreme load transients are 120mV/165mV respectively. The settling time is only 750nS. The LDO presented requires a bias current of 50μA and 200mV dropout voltage and is designed with UMC 130mmrf technology. The LDO presented is useful analog application such as baseband of receiver where high load regulation is necessary for robust application.

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*Keywords:*Operational Transconductance Amplifier (OTA), High slew rate, low-dropout regulator (LDO), low-quiescent current.

1. Introduction

Now for system on chip (SOC) application fully integrated on-chip power management has become a topic of intense interest. Low-dropout (LDO) regulators are widely used in battery-powered mobile systems intense interest. Low-dropout (LDO) regulators are widely used in battery-powered mobile systems. The rapid evolution of battery operated mobile devices has driven the requirement for development of low-voltage integrated

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systems. Although supply voltages are lowered, the power consumption of modern systems are not necessarily low. Battery usage time is determined by power consumption of a mobile device. LDO is generally a voltage reference converter for mobile devices. So the quiescent current of LDO should be kept low in order to reduce battery usage on non-working part of a mobile device so that device can be operated for more time period. But a low quiescent current will result in low bandwidth of error amplifier used in LDO which unavoidably slows the transient responses of regulated voltage. The power efficiency of LDO depends on dropout voltage of LDO. When LDO is driving full load current, if the voltage drop across pass transistor of LDO is less then more voltage is available for the device which increases power efficiency. So for LDO regulator design, the main issue is to minimize the quiescent current and dropout voltage to increase power efficiency. This should be done while maintaining good regulation and a fast response time. For handheld applications such as smart phones and tablets, the number and size of external components such as output capacitors should be minimized to reduce the printed-circuit-board (PCB) space and to speed up the manufacturing process. So, an output capacitorless LDO regulator is preferred. However, because of the limited on-chip size, the internal on-chip output capacitor is smaller and the equivalent serial resistance (ESR) is increased. This leads to severe output voltage changes during a fast-load current transient [1]. To prevent this sudden change in output voltage many researchers have proposed various techniques. It includes procedures for modifying error amplifier to improve slew rate [2]-[7]. However, they fall short of meeting the required performance improvement (power efficiency) due to additional circuitry which consumes more current. Surkanti's and Kwok's studies[8], [9]revealed that by cancelling the effect of existent out pole by determining its location and dynamically adding a zero over it using Resistor–Capacitor (RC) series connected to the gate of the pass device. This technique improves bandwidth which will improve in settling period. But it will not improve the slewrate of the circuit, so the regulated voltage variation during transient will not be affected that much. The technique reported by Leung [10], [11] relies on pole splitting compensation technique that assures that the zero of the system is well below the UGF and high frequency poles are at least three times larger than UGF. The concept utilized is to use the transconductance of pass device and low output node capacitance for achieving stability but the achieving of large transconductance of pass transistor in drop out condition is extremely difficult to be achieved and involved extra stages which increases the complexity.

According to the analysis of literature, it is concluded that the fast transient technique plays a great role for providing a reliable supply voltage at full loads, small overshoot and undershoot of output voltage, and good load regulation and small silicon area. To attain efficient performance, for low power consumption and limited silicon area, this paper presents a low quiescent current, slew rate enhanced LDO with a improved transient response at full load variation. The purposed LDO uses Resistor–Capacitor (RC) compensation scheme to improve bandwidth and phase margin and a dynamic slew rate enhancement circuit to reduce undershoot and overshoot during transient response.

The organization of this paper is given as follows: Section 1 presents introduction,Section 2 presents the proposed LDO description defining the overall performance. Section 3 explains transistor level implementation. Section 4 presents the simulation results, followed by conclusion in Section 5.

2. Proposed LDO Topology

The components of proposed LDO are error amplifier, a power/pass transistor (Q1), a compensation circuit, a slewrate enhancement circuit and feedback resistors RF1, RF2.The block diagram of proposed LDO shown in Fig.1.

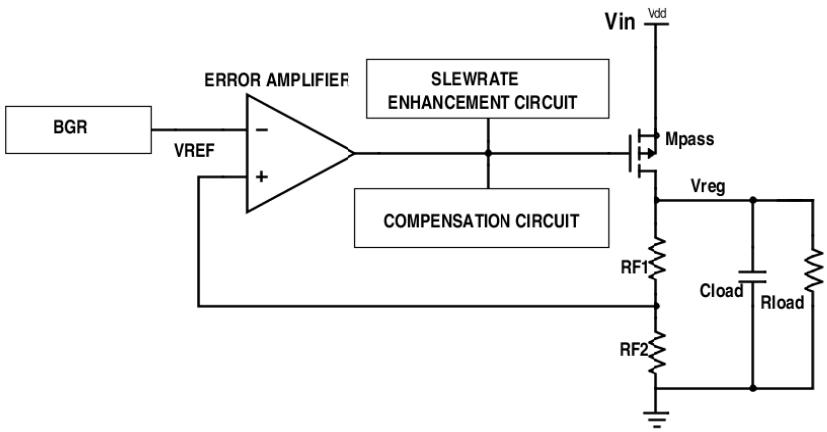

Fig. 1. Proposed Low drop out Regulator

Cload and Rload are the capacitance and resistance of the load circuit which is driven by regulated output of LDO. Generally the load capacitance remains constant but load resistance is a variable, it depends on how much current is consumed by device.

In compensation circuit a Resistor–Capacitor (RC) compensation scheme is implemented across the gate and drain terminal of pass transistor. The parallel capacitor acts as miller compensation and moves the pole at output of error amplifier towards origin and pushes away the pole at out output of pass transistor. By adding a parallel signal path with R-C across pass transistor we are introducing a zero in the left half plane (LHP). By controlling the zero position we can improve the phase margin and bandwidth of the system.

The slewrate enhancement circuit consists of a self-biased comparator, two inverter and sinking transistor. At the time of full load switching the pass transistor cannot respond quickly due to bandwidth limitation, so in order to satisfy the current requirement the node capacitor at regulated voltage starts discharging so node voltage goes on decreasing until the error amplifier is able to change the gate voltage of pass transistor. The voltage droop at output of LDO, derived from capacitor current equation is given as,

$$\Delta V_t = \frac{I_{load}}{C_0} \Delta t_1 \tag{1}$$

Where ΔV_t is the transient voltage droop, I_{load} is the load current step, C_0 is the output load capacitance, Δt_1 is the time taken by the pass transistor to respond. So, if we can decrease the response time of the pass transistor then we can decrease the voltage drop. We can decrease the response time by increasing bandwidth of error amplifier. But increasing the bandwidth of error amplifier will require more quotient current which is against our design goal of making a low power LDO. The other option is to introduce an extra circuitry which will be active only during load transient and will increase slewrate at gate of pass transistor. The proposed slew rate enhancement circuit has two stages. First stage is a self-biased comparator and the second stage is a sinking transistor. The self-biased comparator detects the change in regulated value and changes gate potential of sinking transistor which drains the gate potential of pass transistor, so that the pass transistor able to respond to load change quickly and voltage drop across output is less. But the regulation of gate voltage solely depends on error amplifier which in order decides the settling time.

3. Transistor Level Implementation

The transistor level implementation of the proposedLDO is sown in Fig. 2.The error amplifier constitutes of transistors M1-M11, capacitors C1 and resistor R1. The self-biased comparator constitutes of transistors M12-M17. The pass transistor is represented by Mpasswhile feedback resistances by RF1 and RF2. The R2 and C2 form the compensation circuit across pass transistor.

An operational transconductance amplifier (OTA) is chosen as the error amplifier. A single ended architecture is chosen as it gives higher the gain in one output of first stage than the double ended architecture and it has a higher power supply rejection value [noise]. The more gain from error amplifier contributes to lower the load regulation of the LDO. The size differential pair of the error amplifier, M1 and M2 are kept at a higher value in order to minimize the offset effect. The error amplifier is biased through a β-multipler bias circuit. It reduces the effect of external voltage change on error amplifier operation. The negative input terminal of error amplifier is supplied with a reference voltage of 1V from BGR circuit and the positive terminal is supplied with the feedback from LDO output through resistor pair RF1 and RF2. The error amplifier plays the important role to stabilize the output value during transient. The slewrate enhancement circuit is faster than the error amplifier but regulation of output solely done by error amplifier only.

In order to avoid circuit complexity and more biasing circuit a self-biased comparator circuit is chosen which require only two input signal. One input terminal of comparator is supplied with reference voltage from BGR and other terminal is supplied with LDO output through a resistor divider network Rx and Ry. The value of Rx and Ry are choosen such that the voltage to the other end of comparator is just above the reference voltage and default output set as zero. So when load current switch from 0.5mA to 100mA the output voltage decreases, also the one input to comparator. Now the comparator output changes from zero to one. The self-bias comparator output is not rail to rail, so in order to convert it to rail to rail a digital buffer is used. The buffer output is given to the gate of transistor M23. The transistor M23 is a current sinking transistor. In ideal condition comparator output is zero so this transistor remains off. But during transient as the comparator output becomes one this transistor becomes on and drains charge from gate node of pass transistor and improves the slew rate. The sizing of this transistor is critical as if size is kept too high then gate potential of pass transistor keeps oscillating for more time and settling time of LDO will increase.

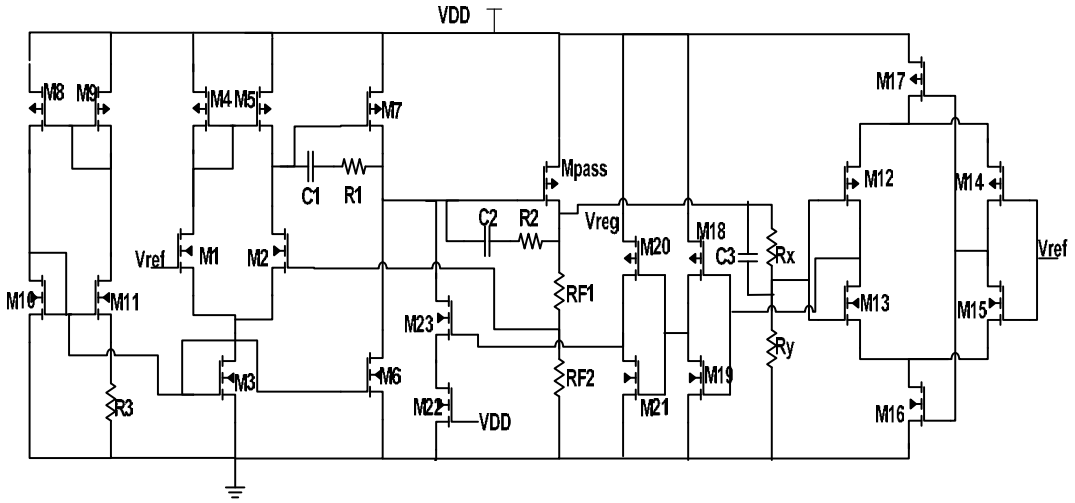

Fig.2. Schematic Proposed Low drop out Regulator

4. Simulation Results

The proposed LDO voltage regulator has been simulated with UMC 130mmrf CMOS process using cadence tool.

A. Transient Response

Fig.3 demonstrates the circuit transient response under load current changes from 0.5mA to 100mA. The overshoot value is165mV and undershoot value is 120mV. The load transient response confirms that the proposed regulator is stable for whole range of load currents.The post layout undershoot value is 138mV.

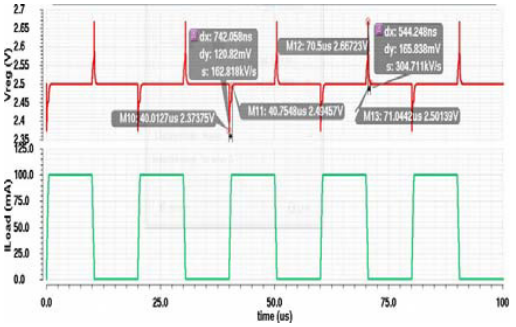

Fig.3. Transient response

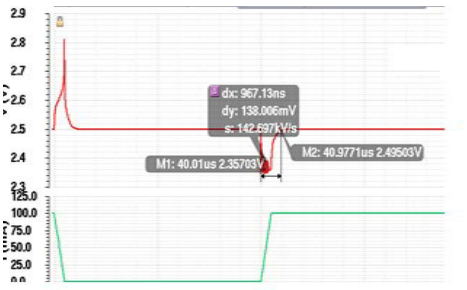

Fig.4. Post layout Transient response

B. Load Regulation

The load regulation is described by the following equation

$$\text{Load regulation} = \frac{\Delta V_0}{\Delta I_0} = \frac{R_0 - Pass}{1 + A\beta}$$

The load regulation is 0.68µV/mA at load current of 100mA as shown in Fig. 5. The post layout load regulation is 1.4µV/mA.

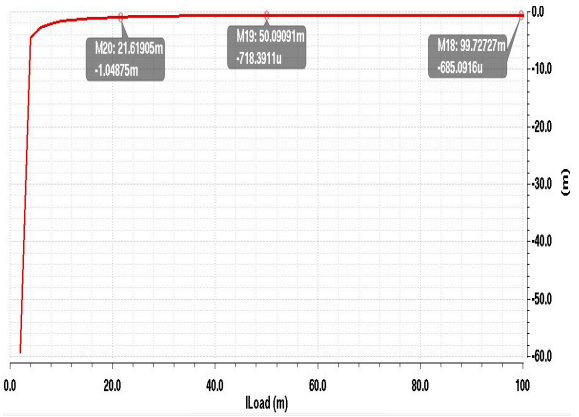

Fig.5. Load Regulation

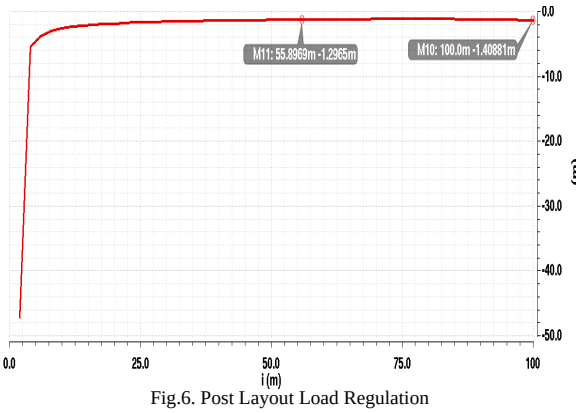

Fig.6. Post Layout Load Regulation

C. *Line Regulation*

The line regulation is the measure of the capability of the LDO to maintain constant output voltage for the input voltage change and is described by Line regulation=Δvo/Δvi. The LDO gives a stable regulated output of 1.4V for a input range of 2.55-5V with a Line Regulation of 1 mV/V. Simulated value of line regulation is represented in Fig.7. The post layout line regulation is also 1 mV/V.

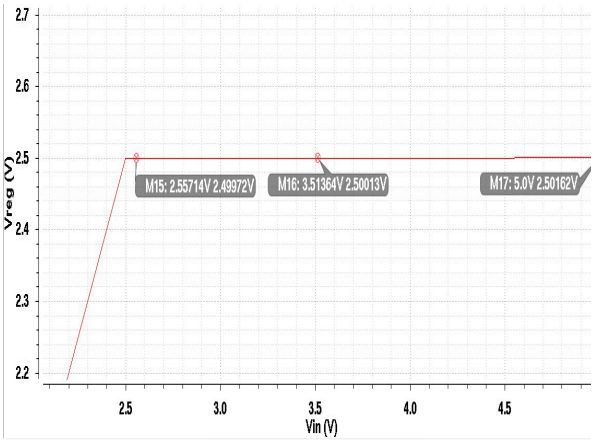

Fig.7.Line Regulation

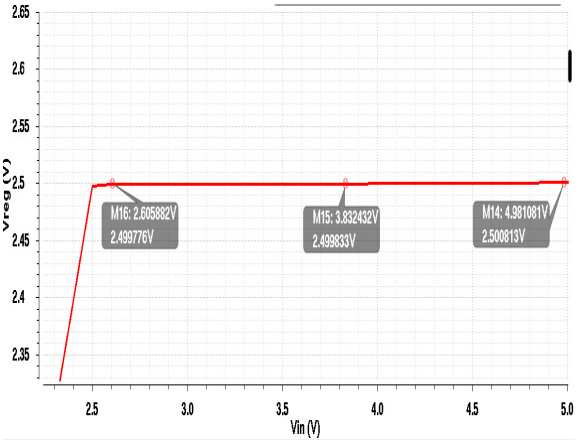

Fig.8. Post Layout Line Regulation

D. PSSR (Power supply rejection ratio)

By the virtue of proposed Double recycling folded cascode the PSRR is -88dB at 1Hz, -59 at 100 kHz and -21 dB at 1 MHz and is shown in Fig. 9.

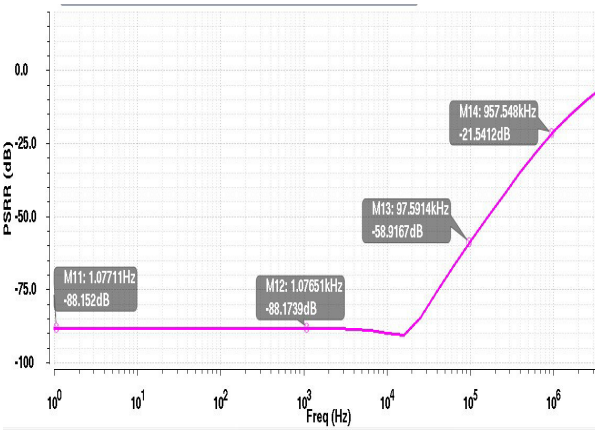

Fig.9. PSR Response

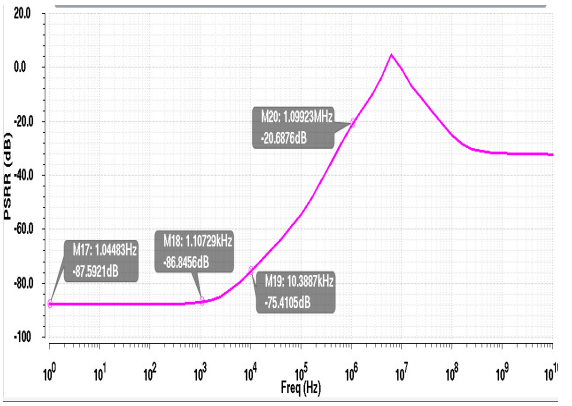

Fig.10. Post Layout PSR Response

E. Loop gain and phase response

The overall stability of the system is defined by the loop gain and its phase response and is as shown in Fig.11. The result shows that the system is stable for varied load current changes.

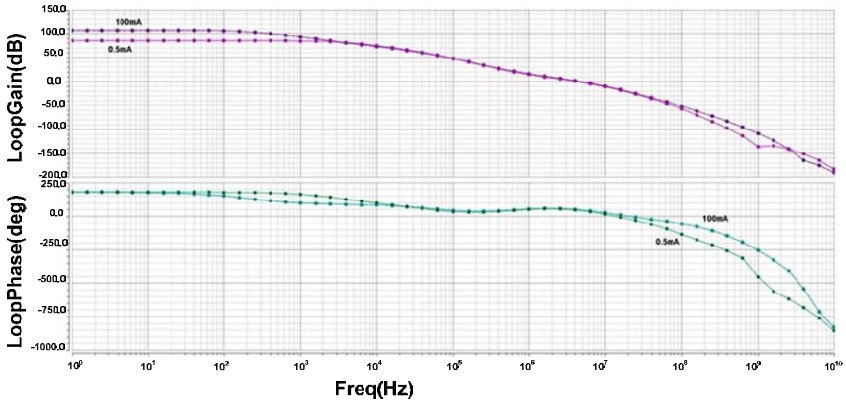

Fig.11.Simulated Loop Gain and Phase Response

5. Conclusion

This paper presented a stable LDO voltage regulator with a dynamic slewrate enhancement circuit. The overshoot of the LDO with the proposed circuit is 165mV for the current change from 100mA to 0.5mA and undershoot of 120mV, when the output current changes from 0.5mA to 100mA. The line regulation is 1mV/V while load regulation is 0.68µV/mA at 100mA. The post layout results also match the schematic results. Therefore, the proposed LDO is a suitable choice for SoC power management applications.

Experimental results show that the proposed LDO voltage regulator exceeds current work in the area of external capacitorless LDO regulators in both transient response and ac stability while consuming only 50µA of quiescent current. The proposed LDO is tested in every corner. The worst case variation of 2mv occurs on slow nMOS and fast pMOS (snfp) corner.

	[12]	[13]	[14]	[15]	[16]	This work
Year	2007	2012	2012	2013	2014	2015
Tech.[µm]	0.18	0.18	0.35	0.11	0.18	0.13
V_{Drop}[mV]	200	N-A	150	200	200	200
C_{OUT}	100pf	100pf	100pf	40pf	100pf	0-100pf
I_{Max}[mA]	50	5	100	0.5-200	100	100
I_Q[mA]	0.0012	0.12	0.007	0.0415	0.0037	0.05
ΔV_{OUT}[mV]	490	170	236	385	277	120
Settling Time Ts[µs]	4.4	1.4	0.15	0.61	6	0.75

TABLE I. COMPARISON OF THE PROPOSED CAPACITOR-LESS LDO TOPOLOGY AGAINST THE STATE OF THE ART

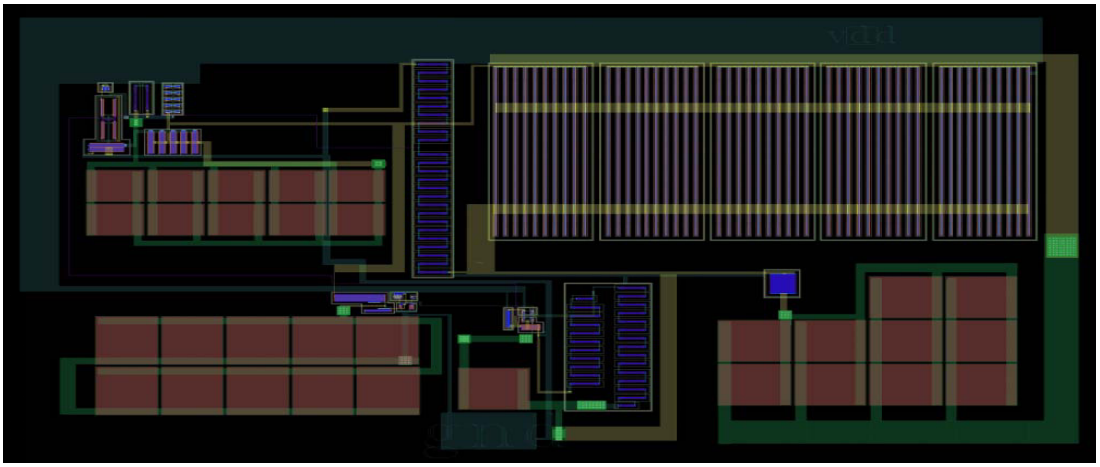

Fig.12.The layout of LDO

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