Low-Dropout Regulator with modest ripple and rugged performance in 180nm

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ABSTRACT

Low-dropout (LDO) regulator with modest ripple and improved transient response is implemented in 0.18μm CMOS technology. The proposed regulator for SOC application can achieve high stability for load current from zero to 100mA. This LDO uses process, temperature independent biasing for error amplifier which makes LDO temperature and process independent. The experimental results show the load regulation of 162 μV/mA and line regulation of 0.9 mV/V. The whole LDO chip consumes a quiescent current of 50 μA with an ultra low dropout voltage of 200mV at the maximum output current of 100mA

Keywords: line regulation, load regulation, transient response, bandgap reference

1. INTRODUCTION

The regulation function is especially important in high-performance applications where systems are increasingly more integrated and complex.A system-on-chip (SoC) incorporates numerous functions, many of which switch simultaneously with the clock, demanding both high-power and fast-response time[1].The bandwidth performance of the regulator, that is, its ability to respond quickly, determines the magnitude and extent of these transient variations. The implication of fewer components in a linear regulator ensures simplicity and less delay through the feedback loop results in higher bandwidth and faster response as compared to its counterpart switching regulators having high efficiency.

The need for integrated systems(soc) invoked lot of research interest in embedding regulators on chip.An ultra fast load transient LDO utilizing decoupling capacitor of 600pf was used which consumed large silicon area [2].The flipped voltage follower requires large power transistor and have low loop gain for output current of given specification[3,4]. This paper presents a low-dropout regulator with fast paths for SoC application. The block diagram of the LDO regulator is shown in Fig. 1. This LDO uses compensation techniques to achieve high stability. This paper is organized as follows: Section 2 presents LDO regulator and its stability analysis. Section 3 presents simulation results

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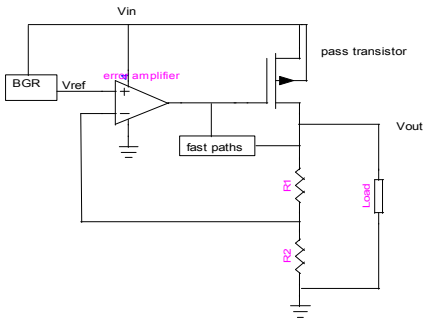

Fig. 1. Low-dropout regulator with fast path

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2.FAST SELF REACTING LDO REGULATOR

2.1 Principle of operation

The fast reacting paths of LDO regulator are illustrated in Figure 1.These are explained as follows.
First reacting path: When load current increases, the output voltage falls .As Mf1 is biased with constant current source V_{SG} of Mf1 remain constant .The decrease in v_{OUT} leads to decrease in gate drive for Mf2 leading to more drive current to be drawn through it. As a result, gate voltage drive for transistor Mp decreases resulting in restoring v_{OUT} to its original value thus completing the feedback operation.

Second reacting path: When load current increases, the output voltage falls. The decrease in v_{out} leads to increase in the V_{GS} of Mf4 which is further coupled through cm2 to input of transistor Mf5 resulting in increase of its operation current. The drive for Mp1 gets reduced and restoring output voltage to its original value instantaneously.

Third reacting path: Transistors M_{F6}-M_{F10} along with Mp constitute a feedback loop as load current increases instantaneously output voltage decreases. The decrease in output voltage sampled through resistors R1 and R2 is coupled to transistor M11 results in drive through M13 increases. The sampled voltage of M13 is then coupled to M16, increasing its drive current ,which further leads to fall in gate drive for transistor Mp,resulting in output voltage to rise.

These three reactive paths lead to quickly recover the output voltage to its regulated value.

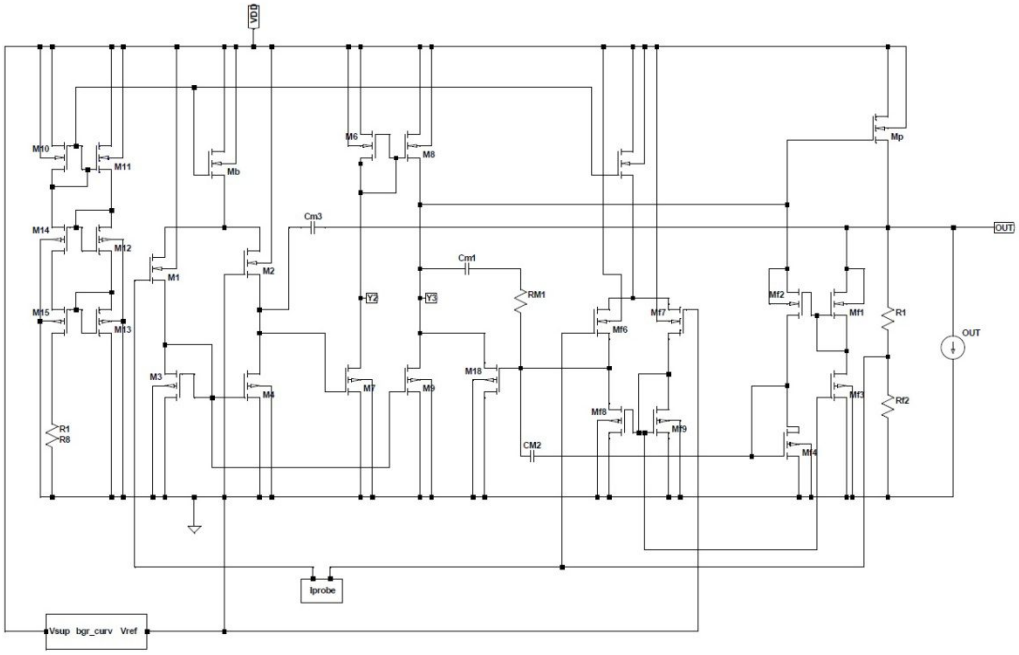

Fig. 2 Schematic of LDO with modest ripple

2.2 Process and temperature independent biasing

The transconductance of MOSFETs plays a critical role in analog circuits, determining performance parameters as small signal gain, speed and noise. Therefore it is desirable to bias the transistors such that their transconductance is independent of process, supply voltage and temperature. By applying KVL to M_{13}, M_{15} and $R_B$loop we get

$$Gm_{13} = \frac{2\left[1-\sqrt{\frac{\frac{w}{L_{13}}}{\frac{w}{L_{15}}}}\right]}{R_B} \qquad (1)$$

By making $W/L_{15} = 4\ W/L_{13}$ we get $gm_{13} = 1/R_B$ and hence gm_{13} is independent of temperature and process variation.

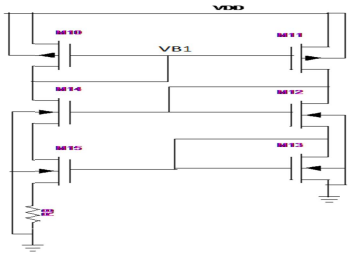

Fig 3 Process and Temperature independent biasing

2.3 System stability

Designed LDO stability is verified for full load and no load currents.

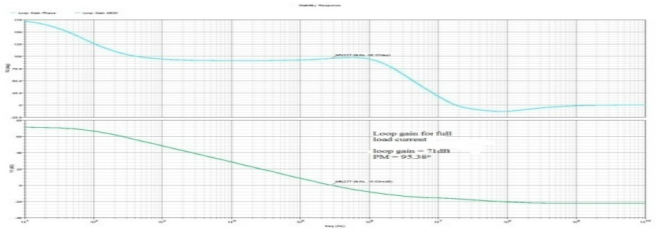

Fig 4. Loop gain for full load currents

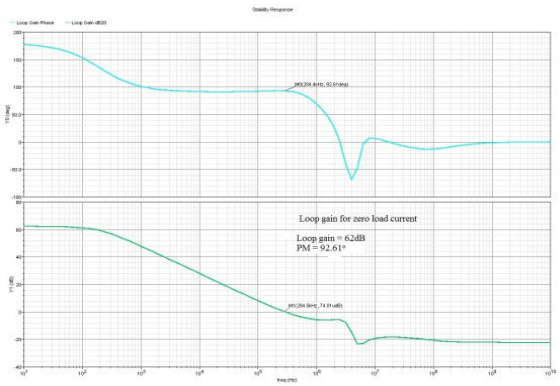

Fig 5 Loop gain for zero load currents

3. EXPERIMENTAL RESULTS

Figure 6 shows the load regulation of LDO for load current swept from 0 – 100mA. This LDO achieved a load regulation of 0.162mV/mA. Figure 7 shows load transient response for a load current step of 100mA with 4us rise and fall time. This LDO has an overshoot of 63mV and undershoot of 63mV.The recovery time for the LDO output voltage is about 1us when load current swept from 0 – 100mA. Figure 8 shows ripple present in the transient response. It has a ripple of 0.9mV in the output. The proposed LDO achieved PSRR of 42dB @1KHz. Over Shoot (OS) and Under Shoot (US) (in mV) for different load currents with 1us rise and fall times are displayed in Table 1.Table 2 compares the present work with the previous works.

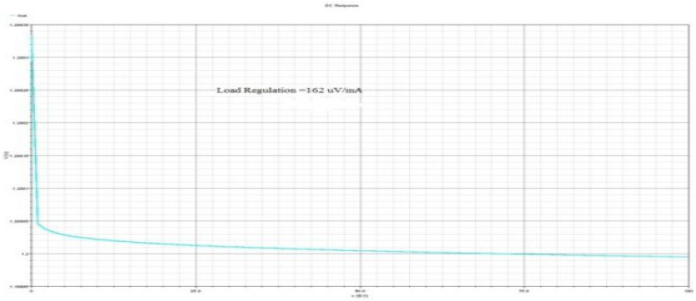

Fig 6 Load regulation

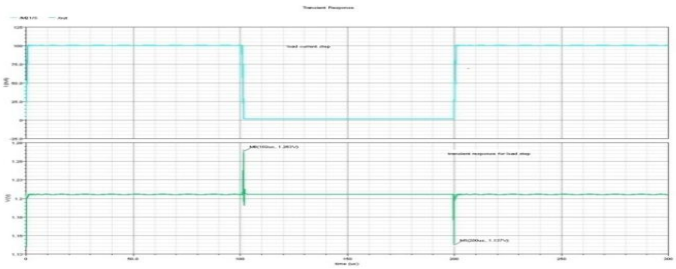

Fig 7 LDO transient response

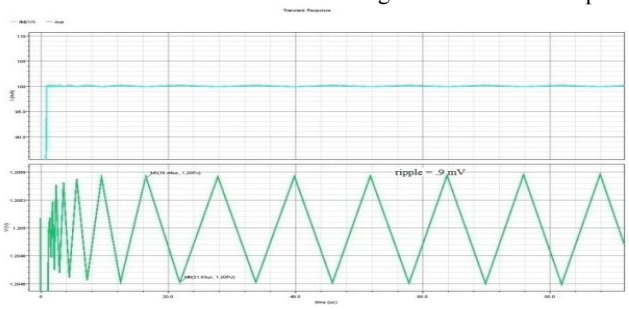

Fig 8 Ripple present in LDO output

Table 1 Transient response for all corners

	0-100mA		10uA-100mA		100uA-100mA		1mA-100mA	
	OS	US	OS	US	OS	US	OS	US
TT	334	360	178	310	97	150	18	20
FF	376	362	191	330	106	148	22	20
SS	368	355	166	260	87	148	14	22
SF	326	340	186	280	101	146	19	11
FS	206	320	167	170	93	145	17	22

Table 2 Comparison of present work with the previous works

parameter	[5]	[6]	[7]	[8]	[9]	This work
technology	0.35um	0.35um	0.35um	0.35um	0.35um	0.18um
$I_{LOAD(max)}$	50mA	100mA	100mA	100mA	50mA	100mA
Δv_{out}(undershoot)	90mV	40mV	70 mV	25mv	150 mV	63mV
Δv_{out}(overshoot)	-	-	-	-	-	63mV
Load regulation (mV/mA)	0.56	0.338	0.4	0.0752	0.28	0.162
Line regulation (mV/V)	23	0.344	-	1.046	18	.989*
PSRRR@1KHz	-57dB	-	-60.6dB			-42dB

*at worst case process corners

4. CONCLUSIONS

A CMOS LDO with fast reacting paths is designed using UMC 0.18µm CMOS process. This LDO yields a regulated output voltage of 1.2V. A line regulation of 0.9mV/V and a load regulation of 162µV/mA are obtained which are better

relative to Chia-Min et.al., while exhibiting a fairly modest transient response. Curvature compensated CMOS band gap reference which produces an output voltage of 0.8V is designed and used as reference for this LDO. The band gap reference circuit is observed to exhibit a temperature coefficient of 12ppm/ ^{0}C.

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