A factorization method for FPGA implementation of Sample Rate Converter for a multi-standard radio communications

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Abstract- **In modern radio communications systems Digital Down Converters (DDC) play a significant role to receive a transmitted signal. The transmitted signal, which is usually a bandpass signal riding over a high intermediate frequency gets sampled at a very higher rate than the ideal Nyquist rate due to the phenomenon of bandpass sampling. Hence a Digital Down converter is used to lower the sampling rate, which eliminates the need of a high speed digital signal processing and reduces power consumption. In this paper we present an architectural implementation of DDC suitable for multi-standard radio communication systems. We have implemented a DDC on FPGA suiting various wireless standards viz, WiMAX 802.16, WCDMA, CDMA2000 and GSM system by the method of factorization [1]. The implemented architecture uses CORDIC algorithm as a mixer in the IF stage and a Cascaded Integrated Comb filter as a decimation filter. We have compared the hardware resources utilized for this multi-standard DDC with a radio communication system with a single standard. The hardware resources for a multi-standard radio have increased by less than fifteen percent.**

keywords:Digital Down Converter, CORDIC, FPGAs, CIC filter, GSM, CDMA2000, WCDMA, WiMAX802.16.

I. INTRODUCTION

The state of art Communication systems forces analog to digital converters(ADCs) to move as close as possible towards the antenna so that a practical software radio becomes existent. The signal to be digitized is an RF signal which poses a high sampling rate requirement on ADCs and therefore high power dissipation. Due to this the present software radio has three functional blocks namely an analog RF processor, digital IF stage and a baseband processor. In an analog RF processor an analog mixer translates the radio frequency signal to a single intermediate frequency signal irrespective of the radio standard. In the subsequent digital IF stage, the intermediate frequency signal is digitized with a sampling frequency equal to twice the IF signal. Due to the phenomenon of bandpass sampling the baseband signal is digitized at a very higher rate than the required Nyquist rate. Sample rate conversion a highly computation intensive task and also channelization task is carried out in this stage. A bandlimited digitized IF signal, sampled at a very high rate is mixed with digital samples of a local oscillator in quadrature to obtain the low frequency inphase and quadrature components of the signal. Then the sampling rate of the signal is decimated to the required sampling rate and filtered. As illustrated by Paul Burns the process of down conversion requires two high end DSP processors per channel which is a cost ineffective solution. Hence FPGAs which are reconfigurable offers high design flexibility, high precision computing and performance improvement can replace the Digital signal processors [2].

A prototype DDC architecture suitable for down conversion of an IF signal at 80MHz to baseband signal of multimode, multi-standard radio is proposed. The pipelined architecture is simulated with XC6VCX75t-1ff484 VIRTEX-6 device, operating at a maximum operating frequency of 240MHz. We make an attempt to estimate the hardware resource utilization on FPGA as suggested by Faheem etal [1].

This paper is organized as follows. Section II describes the theory of DDC, CORDIC algorithm, digital filters, specifications of different wireless standards. Section III presents the calculations for realization of multi-mode, multi-standard software radio and the implemented architecture for DDC. Section IV presents the results with a simulation setup on Virtex-6 XC6VCX75t-1FF484 FPGA and conclusions are presented in section V.

II. THEORY

A. Digital Down Converter

Figure 1 shows the basic architecture of a digital down converter. Numerically Controlled Oscillators(NCO), mixers, decimator and filters are the building blocks. NCOs in quadrature can be employed to generate waveforms and mixers to multiply the incoming IF signal with NCO outputs to produce the sum and difference components i.e., a high frequency component and a low baseband frequency component respectively. Frequency translation

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TABLE I
Specifications for multi-standard software radio

Radio Standard	**WiMAX 802.16**	**WCDMA (UMTS)**	**CDMA 2000**	**GSM 900**
Intermediate Frequency(MHz)	80	80	80	80
Sampling Rate(MSps)	160	160	160	160
Single Channel Bandwidth(MHz)	20	5	1.25	0.2
Required Sampling Rate(MSps)	40	10	2.5	0.4
Over sampling Ratio	4	16	64	400
Target Data Rate(Mbps)	10	3.84	1.2288	0.270
Sample Rate Conversion Ratio	1/8	6/125	48/3125	677/200000

in frequency domain is given by equation(1) and (2). The difference component is filtered out and then decimated.

$$cos\omega_c t\ x(t) \leftrightarrow 0.5[X(\omega-\omega_c)+X(\omega+\omega_c)] \quad (1)$$

$$sin\omega_c t\ x(t) \leftrightarrow j0.5[X(\omega-\omega_c)+X(\omega+\omega_c)] \quad (2)$$

Where x(t) is the input signal, $X(\omega)$ is its Fourier transform and ω_c is the carrier frequency of the signal.

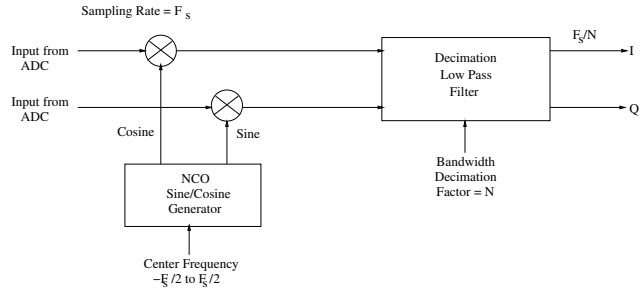

Fig. 1. Block diagram of Digital Down Converter

B. CORDIC algorithm

An iterative algorithm employing simple shift and add operations to compute the value of trigonometric functions using Coordinate rotation of a vector was first developed by Volder in 1959, CORDIC algorithm [3]. Apart from the trigonometric computations CORDIC can also be used for computation of multiplication, division, logarithmic functions, exponential functions as generalized by J.S.Walther in 1971 [4]. Different architectures have been proposed in the literature for realization of CORDIC algorithm. Speed, power, throughput and area constraints governs the choice of the architecture to be used[5] [6]. Due to its structural regularity it is well suited for VLSI implementation. The iteration equations of radix-2 CORDIC algorithm for vector rotation of coordinates in cartesian coordinate system are given as

$$x_{i+1} = x_i - \sigma_i y_i 2^{-i} \quad (3)$$

$$y_{i+1} = y_i + \sigma_i x_i 2^{-i} \quad (4)$$

$$z_{i+1} = z_i - tan^{-1}(\sigma_i 2^{-i}) \quad (5)$$

where σ_i represents the direction of rotation in each iteration and $tan^{-1}2^{-i}$ is an elementary rotation angle. As the CORDIC rotation results in a constant gain(K), the magnitude of the vector increases. The norm of the vector is preserved by scaling the final coordinates by K^{-1}, the CORDIC scale factor.

$$K^{-1} = \prod_{i=1}^{n} \sqrt{1+\sigma_i{}^2 2^{-2i}} \quad (6)$$

For a CORDIC architecture implemented in radix-2 number system, scale factor compensation can be achieved through constant canonic signed digit multipliers. In the design of a receiver for communication systems this parameter can be taken care in the automatic gain control unit of the receiver.

C. Digital Filters

Sampling rate decimation requires digital filters to suppress the aliasing components. A decimator always follows a low pass filter. Implementation of digital filters employs multiplication and accumulation as its fundamental operations. Hence a high speed multiplier operating at twice the frequency of the IF signal must be employed before decimation. To avoid multiplications a special class of multiplier less digital FIR filters called Cascaded Integrated Comb Filters are proposed by Hogenaeur [8]. The process of sample rate conversion is highly aided by CIC filters due to their multiplier less architectures. An N^{th} order CIC filter designed for decimation has N integrators operating at a high sampling rate and N differentiators operating at decimated sampling rate. The transfer function of CIC filter is given by equation 7. In principle CIC filters are simple in design, but integrators become highly instable due to bit growth. A large passband droop is observed in the frequency response of these filters. To restore the signal strength in the passband a droop compensation filter has to be designed.

$$H(z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} \quad (7)$$

Where R = Decimation Factor, M = Differential delay (1 or 2), N = No of Integrators/Combs

D. Specifications

The intermediate frequency of signal for Mobile communications is taken as 80MHz. This signal is digitized with high speed analog to digital converters and has to be passed through a DDC. DDC performs the required frequency translation to produce a baseband signal. Table I shows the specifications for multi-mode multi-standard radio communication systems.

III. ARCHITECTURE

In order to address the problems related to the phase distortions due to phase synchronization and errors due to mixing operations, CORDIC algorithm is used to generate quadrature waveforms and multiplier less mixing operation. CORDIC based DDCs have good SFDR when compared with the conventional Look up table approach [7]. The pipelined CORDIC architecture is implemented with 16-bit precision using carry look ahead adders and CIC filters are implemented on Virtex-6 XC6VCX75t-FF484 device. Though number of architectures have been reported in the literature we choose to opt a non-redundant radix-2 CORDIC architecture. The required throughput for CORDIC architecture depends on the intermediate frequency signal of the radio which is 80MHz requiring a throughput of 160MSPs. A non-redundant radix-2 pipelined CORDIC architecture employing carry look ahead adders is implemented. The maximum throughput of the architecture is 240MSps which is well within the required throughput. A non-redundant architecture reduces the hardware by almost 50 percent in the CORDIC cell as well as in the subsequent stages of system design.

A. Numerically Controlled Oscillator

The structure of a numerically controlled oscillator consists of two blocks viz, phase accumulator and phase to amplitude (sine/cosine) generator. The digital output of the phase to amplitude generator is fed to Digital to Analog Converter and then passed through a low pass filter to remove the unwanted frequency components. The frequency of the NCO is controlled by the frequency control word f_{cw}, which is nothing but the phase increment given to the phase accumulator. In each clock cycle the phase accumulator increments itself by that value until it overflows and wraps around. Thus the frequency of NCO is given by

$$f_c = F_{clk} * \frac{f_{cw}}{2^{n-1}} \tag{8}$$

where F_{clk} = Frequency of the clock,f_c = Required local oscillator frequency and f_{cw}=Frequency control word
We have configured the frequency control word such that the numerically controlled oscillator frequency is tuned to 80MHz.

B. Digital Down Converter block

As stated earlier, equations (3) and (4) describe the rotation of the vectors by an angle θ. The CORDIC module is configured in the circular rotation mode with inputs being $x_0 = x_{if}cos(\omega_{if}n), y_0 = 0, z_0 = \omega_c n$ as shown in figure. The output of the CORDIC module is given by the equations(9) and (10), generating the in phase and quadrature phase mixer outputs.

$$x_{out} = K^{-1}x_{if}cos(\omega_{if}n)cos(\omega_c n) \tag{9}$$

$$y_{out} = K^{-1}x_{if}cos(\omega_{if}n)sin(\omega_c n) \tag{10}$$

$$z_{out} = 0 \tag{11}$$

According to the trigonometric identities, the output of the CORDIC module has two frequency components viz, $\omega_{if} + \omega_c$ and $\omega_{if} - \omega_c$. we have chosen $\omega_{if} = \omega_m + \omega_c$, $\omega_c = 80MHz$ to generate a difference component of ω_m with 160MS/s, which has to be decimated by a decimation factor as shown in table I for Nyquist sampling rate.

C. Filtering and Decimation

In order to remove the aliasing components in the process of decimation a low pass filter has to be employed along with a decimator. CIC filters are the best choice to decimate a signal when high decimation rate is required and a narrow band signal has to be extracted from a wide band signal. We have implemented a pipelined architecture for CIC filters in four stages using three integrators and three differentiators. Decimation factors per stage are calculated using factorization method as stated by Sheikh et al [1] and tabulated in table II. As the CIC filter is implemented in four stages the bit growth requirements are relaxed as suggested by Hogenaeur [8]. Apart from the first stage CIC filter, all subsequent CIC filters in the filter chain are clocked at a frequency of $f_{clk}/4$ or less, hence power dissipation is also reduced to a great extent.

TABLE II
Decimation Factor of CIC Filters for multi-standard Radio calculated by the factorization method [1]

Standard	OSR	**CIC 1**	**CIC 2**	**CIC 3**	**CIC 4**
WiMAX	4	4	1	1	1
WCDMA	16	4	4	1	1
CDMA2000	64	4	4	4	1
GSM	400	4	4	4	6

IV. RESULTS

The simulation setup for testing prototype DDC shown in figure 3 uses three CORDIC based digital synthesizers/mixers generate message signal of 39KHz, Amplitude modulated wave with a carrier frequency of 80MHz and demodulates with CORDIC mixer respectively. CIC filters as stated in section 3C are implemented to extract the inphase and quadrature component of the baseband signal at a lower sampling rate. The design is implemented on VIRTEX-6 XC6VCX75t-1ff484 FPGA and the simulation results are shown in figures[4-7]. Table III shows comparison of device utilization summary for Digital Down Conversion of the inphase and the quadrature channel for a multi-channel radio is made with the single channel GSM900 radio, which requires the highest decimation factor and

TABLE III
Hardware resource utilization on XC6VCX75t-1FF484 FPGA

Hardware Resources	**Multi-Standard Radio**	**GSM900**
No. of Slice Registers	3278	2432
No. of Slice LUTs	4594	4496
No. of Slice LUT-FF Pairs	2359	1747
Frequency(MHz)	240	240

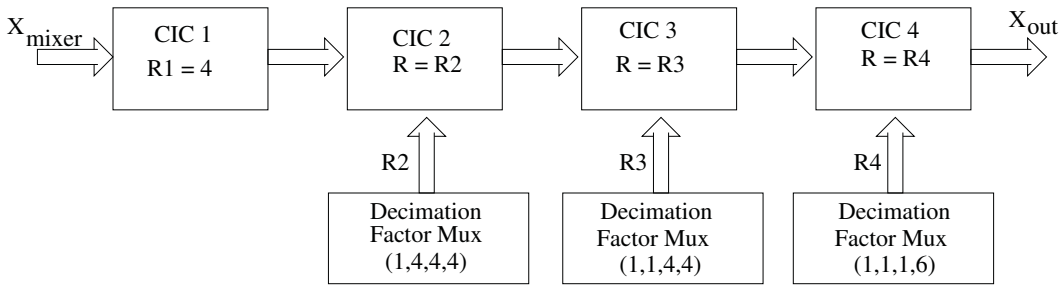

Fig. 2. Architecture of multistage CIC filter

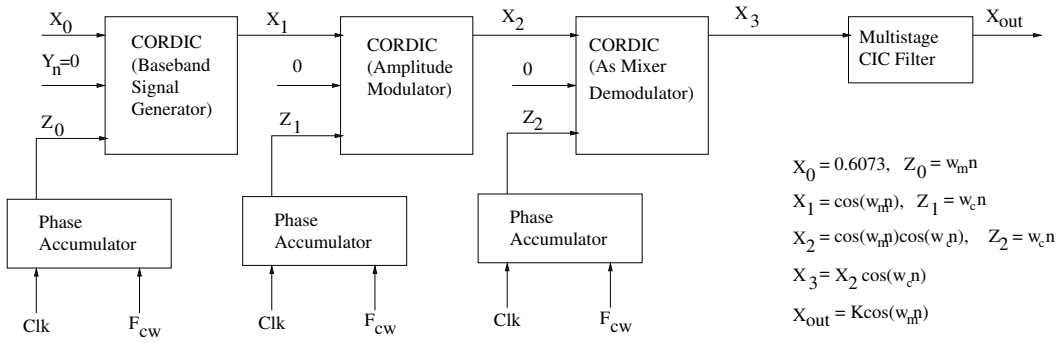

Fig. 3. Simulation setup used for CORDIC based DDC

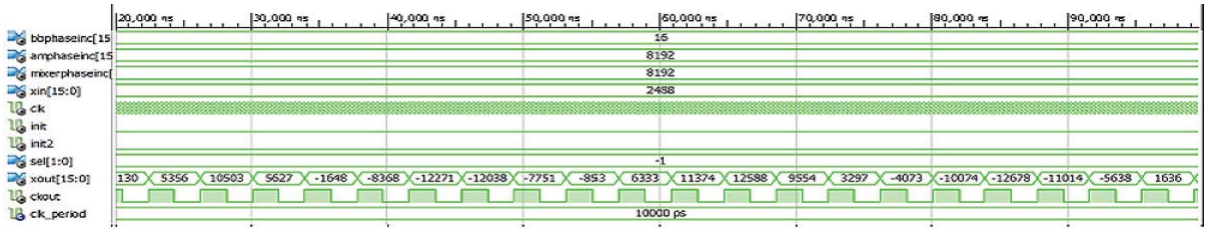

Fig. 4. Simulation result of GSM down converted output Decimation Factor=384

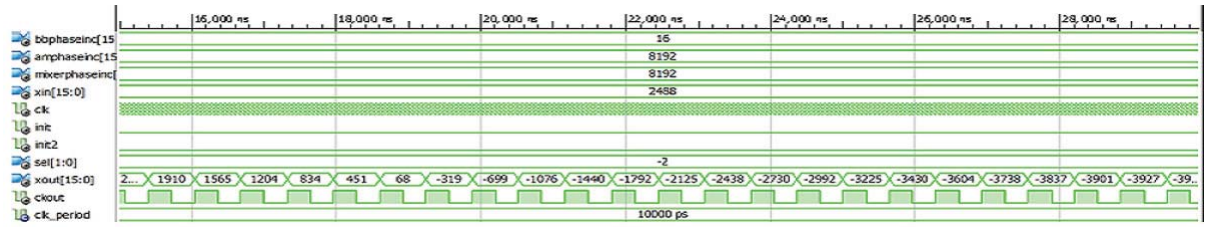

Fig. 5. Simulation result of CDMA2000 down converted output Decimation Factor=64

higher order CIC filter.

For simulation a sinusoidal signal with a frequency of 39KHz is generated by configuring the frequency control word of the phase accumulator of the first CORDIC cell which generates 4096 samples. These samples are amplitude modulated and demodulated with a carrier frequency of 80MHz in the second and third CORDIC cells respectively. For GSM900 specification the decimation factor is 384 and figure 4 shows that mixer output is decimated by the required factor and the number of samples in message signal is found to be 10. Similarly, for CDMA2000, WCDMA and WiMAX the decimation factors are 64, 16 and 4 respectively and the number of samples of the message signal are 64, 256 and 1024 respectively figures 5-7. The results are validated by verifying the repetition of the samples with a sample interval of 10, 64, 256 and 1024 for GSM900, CDMA2000, WCDMA and WiMAX respectively.

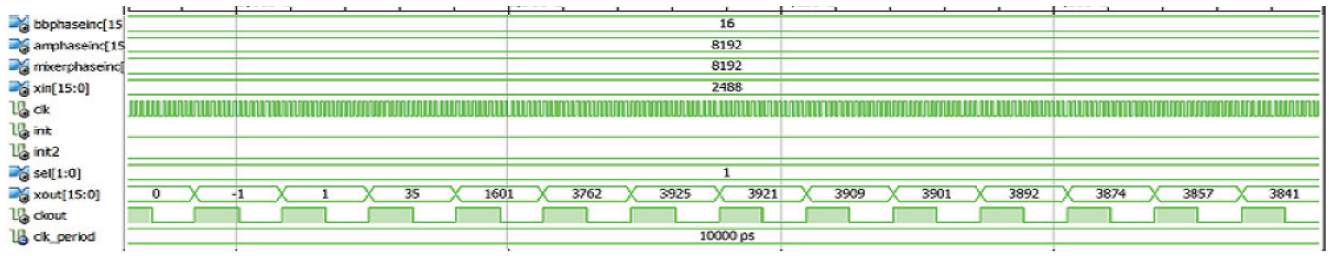

Fig. 6. Simulation result of WCDMA down converted output Decimation Factor=16

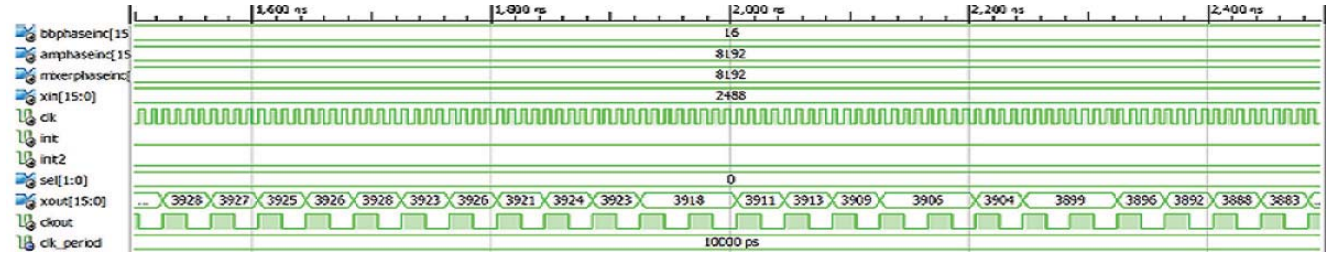

Fig. 7. Simulation result of WiMAX 802.16 down converted output Decimation Factor=4

V. CONCLUSIONS

We have simulated an architecture for sample rate conversion of a multi-standard radio on Virtex-6 XC6VCX75t-1FF484 FPGA based on the factorization method. The use of CORDIC architecture facilitates the implementation of numerically controlled oscillator and quadrature mixer producing the in-phase and quadrature component without employing explicit phase shifter and multipliers. We have made a comparison of the hardware resource utilization of multi-standard radio with a GSM900 standard radio. The comparison shows that increase in the hardware resources for a multi-standard radio is less than 15 percent. Further a programmable interpolation and sample rate conversion filter has to be implemented on FPGA.

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