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Space-vector pulse width modulation scheme for open-end winding induction motor drive configuration

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Abstract: This study proposes a novel space-vector pulse width modulation scheme for an induction motor with open-end windings. The proposed PWM scheme requires two two-level inverters with isolated power supplies. This PWM scheme uses instantaneous phase reference voltages for the generation of gating signals. Open-end winding induction motor (OEWIM) offers significant switching redundancy. Thus, with the proposed scheme the required gating pulses can be generated to reduce the voltage stress on the switching devices. In addition, the switching scheme is capable of equalising the junction temperature rise during the switching and conduction state of the devices. In the present switching scheme when one inverter is switching while the other inverter is clamped and vice versa. The proposed scheme is simulated using MATLAB/Simulink. The PWM scheme is experimentally validated on dSPACE for a three-level OEWIM.

1 Introduction

Multi-level inverter (MLI) is introduced as a solution to increase the converter operating voltage above the voltage limits of the classical semi-conductors [1]. Since three decades, immense research and developments have been found in multilevel inverters for high-voltage and high-power industrial drive applications. MLIs provide various advantages such as, quality voltage waveforms with low harmonic content relating to switching pattern, low dV/dt stress, reduction of common-mode voltages and lesser rating of switching devices. Besides these, it also reduces the problems associated with dielectric breakdown between motor windings influenced by dV/dt stress [1]. Although MLIs offer several advantages, the modulation and control is more complex because of the transitions between the voltage levels. Few important MLI topologies are neutral-point-clamped (NPC) [1], flying capacitor-type [2], cascaded configuration [3], hybrid configuration [4, 5], modular MLI [6], cross-switched MLI [7] and open-end winding induction motor (OEWIM) drive configuration [8].

This paper presents a novel space-vector pulse width modulation (SVPWM) scheme for OEWIM drive topology which offers several advantages such as 50% reduction in DC-link voltage and device ratings, respectively, absence of neutral-point fluctuations compared with other three-level inverter topologies. Several PWM schemes for OEWIM drive have been reported in the literature which addressed various issues relating to zero sequence voltages [8], common mode voltages [4, 5] and DC-link voltage balancing [9]. In [10] alternate-sub-hexagonal-centre (alternate-SHC) PWM switching strategy and alternate-inverter PWM switching strategy for an OEWIM were compared. Alternate-SHC scheme performs better than the alternate-inverter PWM scheme; however, there is a considerable disparity in the junction temperature between the top and bottom switches of the inverter leg, because of the unequal switching and clamping duty of the switching devices. The proposed scheme addresses the disparity and significant reduction in junction temperature of the switches. An existing thermal model [10, 11] has been adopted in this work to quantify the switching- and conduction-losses for the proposed scheme.

2 Two isolated inverters feeding OEWIM

An OEWIM has six input terminals as in Fig. 1*a*, formed by removing the star point of a conventional induction motor. Thus, an OEWIM has two sets of three phase input terminals accounting a total of six input terminals. This OEWIM is now capable of functioning such as a conventional three phase induction motor, if it is fed by two two-level inverters from either side. It is important to ascertain the phase sequence in this motor as any inapt connection would stall the motor or it may result in reversal of the direction of rotation. Each side of the OWEIM can be connected to a conventional three-phase two-level inverter independently, which results in the three-level inversion with its space vector locations similar to NPC three-level-inverter. A reduced DC-link voltage with 50% is sufficient to obtain the voltage levels as that of a NPC three-level inverter, which results in 50% reduction of the rating of the DC-link capacitors and the switches. The OEWIM can be connected in two different configurations pertaining to three-level inversion mode. One such connection uses a common DC-link for the two inverters. In the other configuration the inverters are connected with isolated DC-link power supply. In case of common DC-link the zero sequence currents are allowed to flow through the top rail or bottom rail. Conversely, the zero sequence currents are blocked by using isolated DC-link power supplies; consequently, the zero sequence voltage appears across the points '*O*' and '*O*''. It can also be seen that in dual-inverter scheme, the DC-link voltage of individual inverters is equal to $V_{dc}/2$, whereas the DC-link voltage of an equivalent single inverter drive is equal to V_{dc}. Fig. 1*b* illustrates the voltage vectors for Inv-1 and Inv-2. Eight switching states can be reaped out from Inv-1 and another eight switching states can be reaped out from Inv-2. The sharing of both the inverters resulted in 64 switching combinations, which are heaped up in few locations and sparsely located in other locations within the available 19-space vector locations of a three-level hexagonal structure. An example is worked out for clarity in which Inv-1 switching state is assumed to be 2 (++−) and Inv-2 state is assumed to be 3′ (−+−). These individual states of the two inverters will collectively form the space vector '2–3'' for the OEWIM drive, which is located in 'A' as shown in Fig. 1*c*.

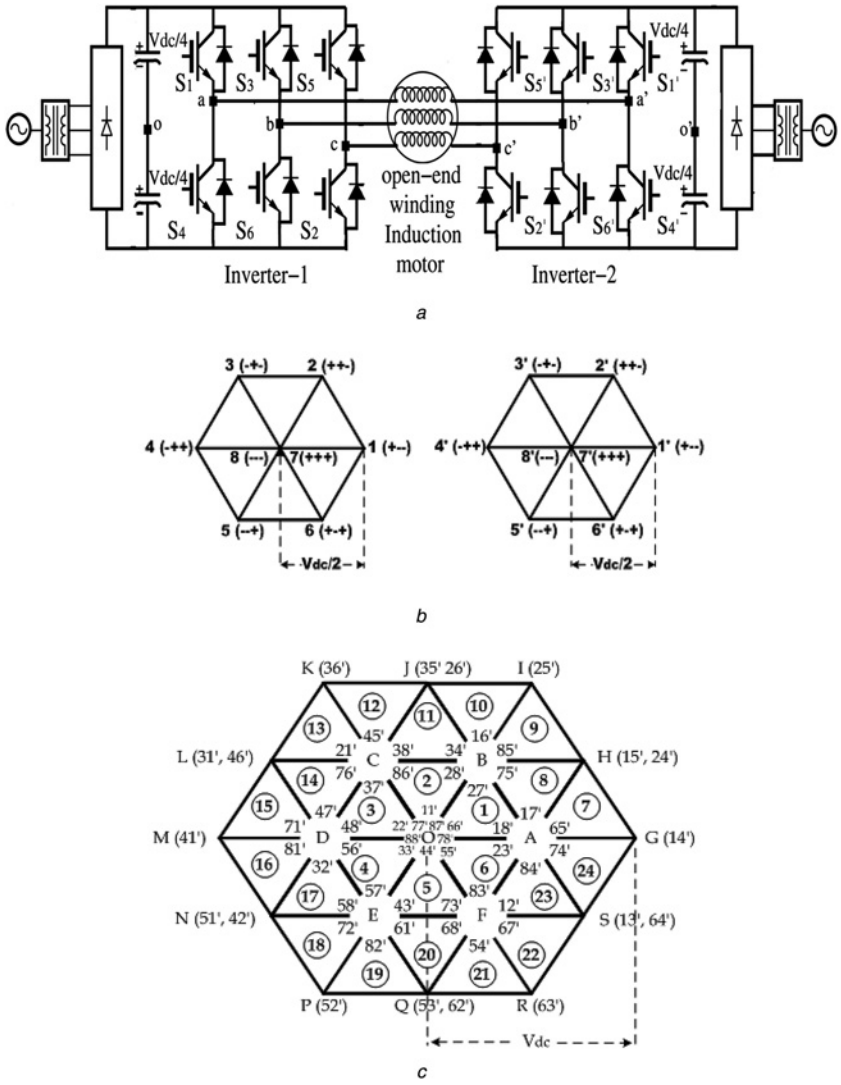

Fig. 1 *OEWIM has six input terminals*

a Two isolated inverters fed OEWIM drive
b Voltage vectors for Inv-1 and Inv-2
c Space vector locations for a 3-level dual inverter scheme

Fig. 1*c* shows the switching vector locations for an OEWIM drive. It is observed from Fig. 1*c* that a reference space vector can be realised by using different switching combinations because of the presence of high switching redundancy. Moreover, it can be observed that there exist a base hexagon with its centre 'O' and its boundaries are marked by the alphabets '*A*, *B*, *C*, *D*, *E*, *F*', which again forms the centres of six concurrent hexagons. As a whole there are seven hexagons with 19-space vector locations and each vertex corresponds to the DC-link voltage of individual inverter which is $V_{dc}/2$. A switching power pole of the inverter can rack up either '$V_{dc}/4$' or '$-V_{dc}/4$' depending on the position of the switch being operated in the power pole or phase leg. If the top switch is closed then the pole voltage is '$V_{dc}/4$' and if the bottom switch is closed, then the pole voltage attained is '$-V_{dc}/4$' by Inv-1 phase leg. Similarly it can be noted for the two other phase legs of Inv-1 and for three phase legs of Inv-2. The motor phase voltage across a particular phase winding is given by the expression

$$V_{xx'} = V_{x0} - V_{x'0'} \tag{1}$$

where, x – Inv-1 phases denoted by '*a*' or '*b*' or '*c*', x' – Inv-2 phases denoted by '*a*'' or '*b*'' or '*c*'', 0 – Fictitious neutral of Inv-1, 0′ – fictitious neutral of Inv-2.

The motor phase voltage of the individual phase winding of a dual inverter fed OEWIM drive is given by

$$V_{aa'} = V_{a0} - V_{a'0'} \tag{2}$$

$$V_{bb'} = V_{b0} - V_{b'0'} \tag{3}$$

$$V_{cc'} = V_{c0} - V_{c'0'} \tag{4}$$

The phase windings in this drive configuration is capable of reaching any of the following voltage levels, '0', '$-V_{dc}/2$' and '$+V_{dc}/2$'. Voltage space vector denoted by 'V_{sr}' is the outcome of the collective effect of the voltages in the three-phase windings of the motor, which is given by

$$V_{sr} = V_{aa'} + V_{bb'}e^{(j2pi/3)} + V_{cc'}e^{(-j2pi/3)} \tag{5}$$

From (5) the voltage space vector locations for different switching combinations are shown in Fig. 1*c*. This voltage space vector can be equivalently represented as the sum of the voltage space vectors generated by the two two-level inverters. If V_{s_1} and V_{s_2} are the voltage space vectors generated by Inv-1 and Inv-2,

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Table 1 States of individual inverters

State of Inv-1	Switches turned ON	State of Inv-2	Switches turned ON
1 (+ − −)	S_6, S_1, S_2	1′ (+ − −)	$S_{6'}$, $S_{1'}$, $S_{2'}$
2 (+ + −)	S_1, S_2, S_3	2′ (+ + −)	$S_{1'}$, $S_{2'}$, $S_{3'}$
3 (− + −)	S_2, S_3, S_4	3′ (− + −)	$S_{2'}$, $S_{3'}$, $S_{4'}$
4 (− + +)	S_3, S_4, S_5	4′ (− + +)	$S_{3'}$, $S_{4'}$, $S_{5'}$
5 (− − +)	S_4, S_5, S_6	5′ (− − +)	$S_{4'}$, $S_{5'}$, $S_{6'}$
6 (+ − +)	S_5, S_6, S_1	6′ (+ − +)	$S_{5'}$, $S_{6'}$, $S_{1'}$
7 (+ + +)	S_1, S_3, S_5	7′ (+ + +)	$S_{1'}$, $S_{3'}$, $S_{5'}$
8 (− − −)	S_2, S_4, S_6	8′ (− − −)	$S_{2'}$, $S_{4'}$, $S_{6'}$

respectively, the resultant voltage space vector is

$$V_{sr} = V_{s_1} + V_{s_2} \tag{6}$$

Inv-1 and Inv-2 are operated with a DC-link voltage of $V_{dc}/2$. Thus, the sum of the DC-link voltages is equal to V_{dc}, which is the DC-link voltage of an equivalent conventional three-level inverter drive Table 1.

As all three phase winding are balanced, any one phase winding is considered to define the phase voltages for various operating states of the individual inverter as described in Table 2. Fig. 2 depicts the operating modes of OEWIM drive for different phase voltages given in Table 2. From Fig. 2*a* it can be noted that the top switches in both the inverters are turned-ON, which represents the switching combination '7–7′'. This implies that all the top switches of Inv-1 and Inv-2 are turned-ON, results in zero output voltage across the motor phase windings as given in (1). Fig. 2*b* depicts the switching combination '7–8′' with '7 (+ + +) and 8′ (− − −)' in which all the top switches of Inv-1 are turned-ON and all the bottom switches of Inv-2 are turned-ON, which would again result in zero output voltage across the motor phase windings. Similarly, Fig. 2*c* depicts the switching combination '8–8′' with '8 (− − −) and 8′ (− − −)', in which all the bottom switches of both the inverters are turned-ON, which would again result in zero output voltage across the motor phase windings.

Table 2 Pole voltages and motor phase voltage

Pole voltage of Inv-1	Pole voltage of Inv-2	Motor phase voltage
$V_{dc}/2$	$V_{dc}/2$	0
$V_{dc}/2$	$-V_{dc}/2$	V_{dc}
$-V_{dc}/2$	$-V_{dc}/2$	0
$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}$

The next case corresponds to the switching combination '8–7' with '8 (− − −) and 7′ (+ + +)' as shown in Fig. 2*d* in which the three bottom switches of Inv-1 are turned-ON and three top switches of Inv-2 are turned-ON resulting in zero output across the motor phase windings.

The switching combinations depicted in Fig. 2 corresponds to the null states, which is in the core hexagon located at 'O' of the three-level hexagonal structure as shown in Fig. 1*c*. However, considering the switching combination '2–3′', state '2 (+ + −)' corresponds to Inv-1 switching state and '3′ (− + −)' corresponds to the Inv-2 switching state. A '+' indicates a particular phase being connected to the positive rail of the DC-link. A '−' indicates a particular phase being connected to the negative rail of the DC-link. For '2–3′', the 'phase-a' legs of Inv-1 and Inv-2 are connected to a DC-link with '$V_{dc}/2$' and '$-V_{dc}/2$', respectively. Thus the motor 'phase-a' voltage for the switching combination '2–3′' is 'V_{dc}'. Similarly, the motor 'phase-b' and 'phase-c' voltages are '0'.

3 SVPWM schemes for OEWIM

3.1 Alternate-SHC PWM switching scheme

In alternate-sub-hexagonal-centre PWM switching scheme [9], Inv-1 is clamped during a particular interval of time while Inv-2 is switched and vice-versa. Fig. 3*a* shows the principle of alternate-SHC PWM scheme. Again from the same figure the shaded and unshaded regions significantly show the clamping and switching inverters. Inv-1 is clamped and Inv-2 is switched in the shaded region while in the un-shaded region Inv-2 is clamped and Inv-1 is switched. The principle of alternate-SHC PWM is illustrated for clarity. When the reference voltage space vector 'OV' is located in the shaded region OSGH, it is resolved into two components namely OA and AV, respectively. The first component OA is generated by clamping Inv-1 to state '1 (+ − −)' and the component AV is generated by switching Inv-2 as long as the reference space vector lies in the shaded region within the nearest sub-hexagonal centre-A (NSHC-A). Now, as the reference space vector moves although an angle of 30° from the phase-a reference axis, it falls under the vicinity of NSHC-B, which in the un-shaded region. Here Inv-2 is clamped to state 5 (− − +), while Inv-1 is switching. Thus the both the inverters alternate their clamping and switching duty every 60°. As the reference space

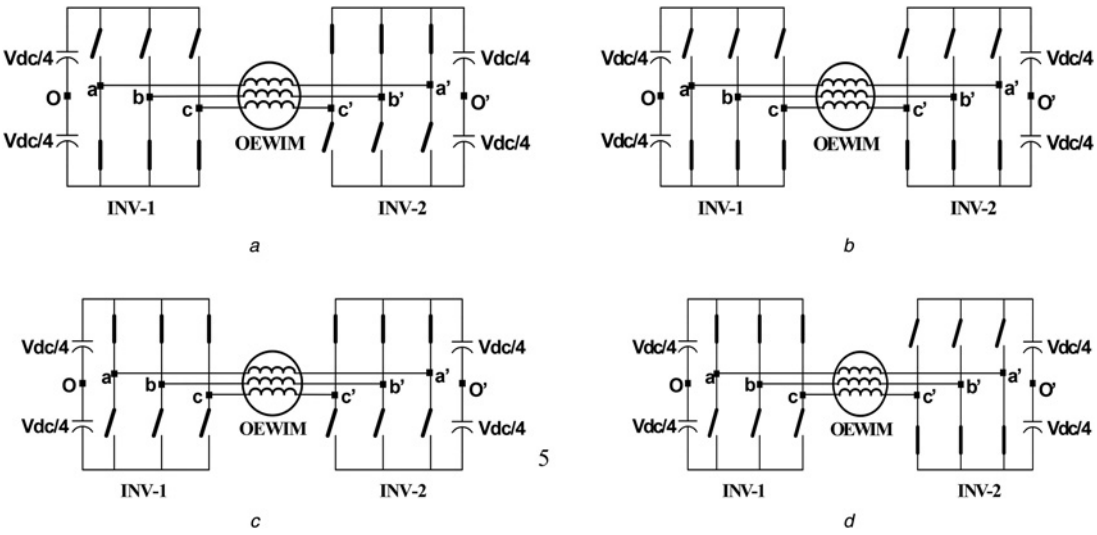

Fig. 2 *Different states for both the inverters*

a Switching combination 7-7′
b Switching combination 7-8′
c Switching combination 8-8′
d Switching combination 8-7′

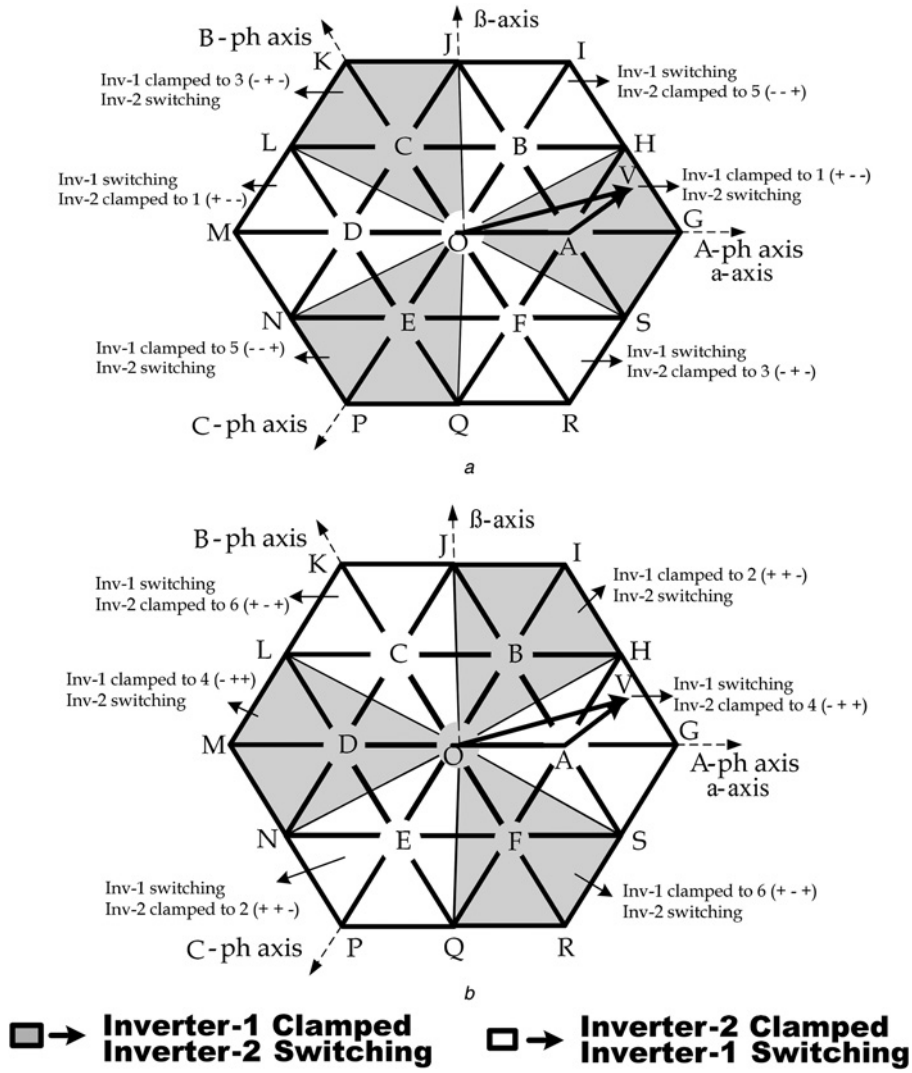

Fig. 3 *Principle of alternate-SHC PWM strategy and scheme*

a Principle of alternate-SHC PWM strategy [9]
b Principle of proposed alternate-SHC PWM scheme

vector lies in the shaded regions such as NSHC-A or NSHC-C or NSHC-E, Inv-1 is clamped to state '1 (+ – –)' or '3 (– + –)' or '5 (– – +)', respectively, while Inv-2 is switched. If the NSHC is B or D or F, Inv-2will be clamped to states '5′ (– – +)' or '1′ (+ – –)' or '3′ (– + –)', respectively, while Inv-1 is switched Table 3.

3.2 Proposed SHC PWM scheme for loss minimisation

A new space vector based PWM switching scheme is proposed in this paper as illustrated in Fig. 3*b*. The method proposed in [12] is extended in generating the gating pulses for the proposed PWM scheme. Considering the reference space vector OV with its tip 'V' located in the sector '7' is resolved into two components namely OA and AV. The component OA is generated by clamping one inverter while switching the other inverter as long as the reference space vector lies in the vicinity of the nearest (NSHC). Since the NSHC is 'A' in this case, Inv-1 is allowed to perform the clamping duty by clamping to state '1 (+ – –)' while Inv-2 is allowed to perform the switching duty. This switching is liable till the reference space vector lies in the quadrangle 'OSGH' which is marked by the 60° span as shown by the shaded region in Fig. 3*b*. When the reference space vector crosses the line marked by OH, then it comes under the influence of the next NSHC, which happens to be 'B'. As long as the reference space vector is under the influence of NSHC-B, Inv-2 will be performing the clamping duty by clamping to state '5' (– – +)'and Inv-1 will be performing the switching duty. Depending upon the NSCH, Inv-1 and Inv-2 will exchange their clamping and switching duties. If the NSHC is A, C or E, Inv-1 is clamped to states '1 (+ – –)', '3 (– + –)' or '5 (– – +)', respectively. At the same instants, Inv-2 will be involved in the switching operation as dictated by the PWM scheme. If the NSHC is B, D or F, Inv-2 is clamped to states '5' (– – +)', '1' (+ + –)' or '3' (– + –)', respectively and Inv-1 will be performing the switching operation as dictated by the PWM scheme. Thus during the first cycle of rotation of the reference space vector, the clamping and switching operation of both the inverters are similar to alternate-SHC PWM scheme.

Table 3 Inverter roles for realising the reference vector [9]

NSHC	A	B	C	D	E	F
Inv-1	clamped to 1 (+ – –)	switched	clamped to 3 (– + –)	switched	clamped to 5 (– – +)	switched
Inv-2	switched	clamped to 5 (– – +)	switched	clamped to 1 (+ – –)	switched	clamped to 3 (– + –)

Table 4 Inverter roles for realising the reference vector for the proposed scheme

	NSHC	A	B	C	D	E	F
during the first cycle of rotation of space vector	Inv-1	clamped to 1 (+ − −)	switching duty	clamped to 3 (− + −)	switching duty	clamped to 5 (− − +)	switching duty
	Inv-2	switching duty	clamped to 5 (− − +)	switching duty	clamped to 1 (+ − −)	switching duty	clamped to 3 (− + −)
during the second cycle of rotation of space vector	Inv-1	switching duty	clamped to 2 (+ + −)	switching duty	clamped to 4 (− + +)	switching duty	clamped to 6 (+ − +)
	Inv-2	clamped to 4 (− + +)	switching duty	clamped to 6 (+ − +)	switching duty	clamped to 2 (+ + −)	switching duty

During the second cycle of operation, when the tip of the reference vector lies within the territory marked by 'OSGH', Inv-2 is clamped to state '4 (− + +)' and Inv-1 is switched around it. As the reference space vector moves over and fall within the un-shaded region marked by 'OHIJ', Inv-1 is clamped to state '2 (+ + −)' and Inv-2 is switched around Inv-1. If the NSHC is A, C or E, Inv-2 is clamped to states '4' (+ − −)', '6 (+ − +)' or '2 (+ + −)', respectively and Inv-1 will be performing in the switching operation as imposed by the PWM scheme. If the NSHC is B, D or F, Inv-1 will be clamped to states '2 (+ − −)', '4 (− + +)' or '6 (+ − +)', respectively, while Inv-2 is involved in the switching operation as dictated by the PWM scheme. Thus during the first cycle of rotation of the space vector, Inv-1 is clamping and Inv-2 is switching and vice versa during the second cycle depending upon the NSHC for every 60° of the cycle. During the third cycle, the duties of inverters in the first cycle are replicated and so on. The instantaneous three-phase reference voltages govern the switching times for the switching inverter and clamping times for the clamping inverters, thus eliminating the need for either sector identification or lookup tables. Inverter clamping and switching role are synopsized in Table 4.

Two PWM schemes namely alternate-SHC and modified-alternate-SHC for loss minimisation PWM scheme are presented in this paper for comparison of device temperature and switching power loss. Among the two inverters, one inverter is allowed to perform clamping duty whereas the other inverter is dictated to perform the switching duty within the same sampling instant. In the first method, the clamping states such as '1 (+ − −)', '3 (− + −)' and '5 (− − +)' are only used to clamp both the inverters when they fall under the appropriate NSHC. In the proposed method despite using the clamping sates '1 (+ − −)', '3 (− + −)' and '5 (− − +)' during the first cycle of rotation of the reference space vector, the inverters are additionally subjected to deploy '4 (− + +)', '6 (+ − +)' and '2 (+ − −)' as their clamping states during the second cycle of rotation of the reference space vector. It is evident that both the PWMs look similar, but the sample disposition makes the proposed SVPWM different and unique. The switching losses and the conduction losses in a power semi-conductor device are mainly based on the switching speed. Hence, the switching and clamping duties of the switches that are used in the inverters would certainly have an impact on the losses and the temperature build-up in their junctions. A critical

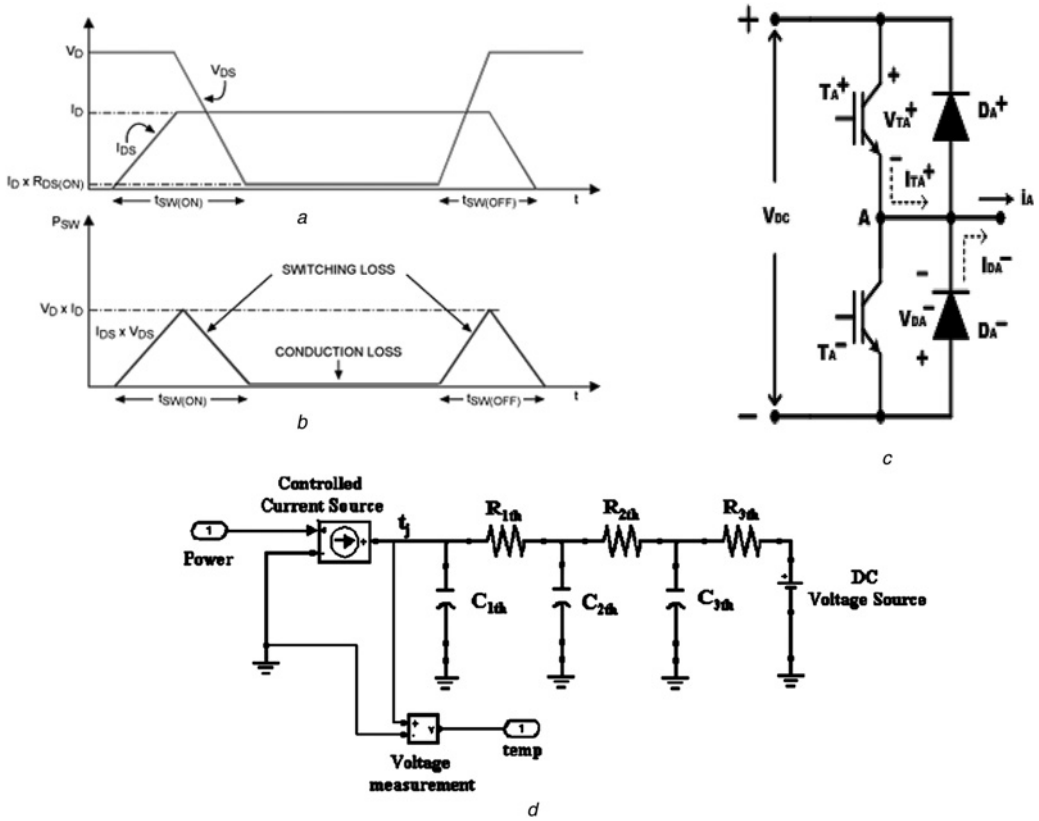

Fig. 4 *Phase-a leg of the one of the two two-level inverters of the dual inverter fed open end winding induction motor drive system*

a Device switching strategy
b Switching loss and conduction loss
c Phase-a leg of Inv-1 showing the controllable switches and their anti-parallel diodes
d R-C Thermal Network for estimation of junction temperature

comparison is carried out in this work to evaluate the losses arising due the above described PWM schemes using simulation studies.

4 Switching loss and conduction loss calculation

In power electronic switches, power loss in the form of heat dissipation is usually observed. In this work, two two-level inverters are used to realise the three-level inversion using the OEWIM drive. Each phase leg of the inverter consists of two switches which is capable of conducting the flow of current in either direction. A phase-a leg of the one of the two two-level inverters of the dual inverter fed open end winding induction motor drive system is shown in Fig. 4*c*. In Fig. 4*c* T_A^+ and T_A^- represents the controllable top- and bottom- switches of phase-a leg of one of the inverters of dual inverter fed OEWIM drive. Again from Fig. 4*c*, D_A^+ and D_A^- represents the anti-parallel diodes for the controllable switches of the same phase leg. This combination of controllable switch and its anti-parallel diode will allow the flow of load current in both the positive and negative directions. Either T_A^+ should be switched-ON or the naturally forward biased anti-parallel diode D_A^- should be in conducting mode if the load current is positive. Conversely, T_A^- or D_A^+ will conduct for negative values of load current. The anti-parallel diodes are assumed to be ideal since their losses are lesser compared with the losses that occur in the power semi-conductor switches [10, 11]. The current flowing through the switch and the voltage across it, when operated with a switching frequency of $f_s = 1/T_s$, where T_s is the switching time period is illustrated in Figs. 4*a* and *b* [10]. The proposed work addresses an alternate-SHC PWM scheme for loss minimisation by evaluating the switching losses, conduction losses and the rise in junction temperature of the power semi-conductor devices. A comparative result analysis has been carried in contrast with the alternate-SHC PWM switching strategy [9, 10].

For positive and negative values of load current the turn-ON and turn-OFF transitions of the controllable switches are shown in Figs. 4*a* and *b*. Switching losses occurs during the turn-ON and turn-OFF transitions of the switch and the conduction losses are influenced by the ON-state resistance of the switching device. Since there are two controlled switches in each phase leg of the inverter, the combined effect of the switching and conduction losses of both the switches will account for inverter leg-losses. The variables considered for evaluating the losses in inverter leg are the switching pulses, motor phase current, the rise time (t_r) and fall time (t_f) of the voltage and current, the ON-state voltage-drop and OFF-state voltage of the switch [10]. To estimate the rise in junction temperature of the switch with respect to the ambience, the calculated leg-losses are fed to a conventional R–C thermal network shown in Fig. 4*d* [10]. The three-prototype thermal impedances such as junction to case impedance, case to heat-sink impedance and heat-sink to ambient impedance are normally assumed in the thermal design of a conventional converters are considered. Steady-state temperature and the rise in temperature dynamics are determined by the thermal resistance and capacitor, respectively.

5 Results and discussions

The proposed alternate-SHC switching scheme for loss minimisation has been simulated using MATLAB/Simulink. Fig. 5*a* illustrate the

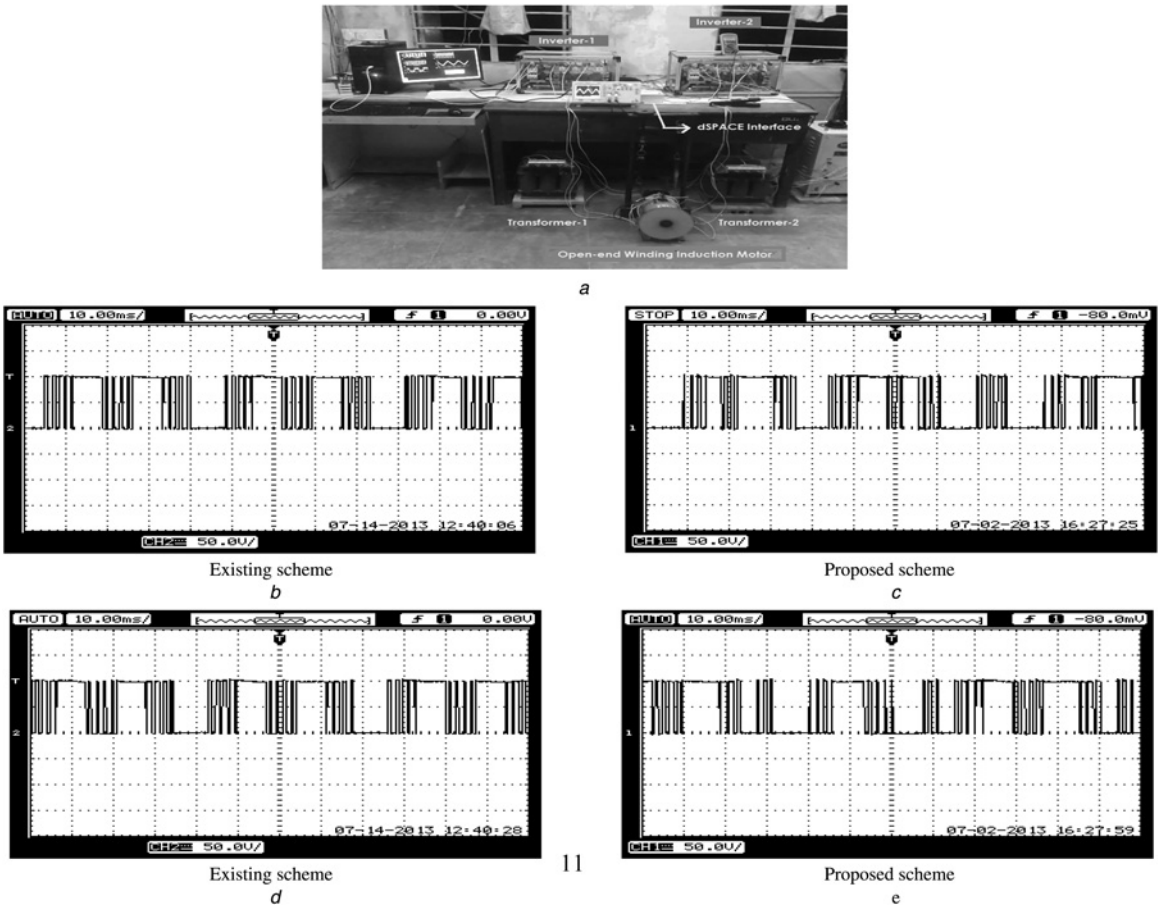

Fig. 5 *Prototype of dual-inverter fed 5-hp, three-phase OEWIM with V/f control which is built and validated experimentally using dSPACE platform*

a Prototype of Dual-Inverter fed 5-hp three-phase OEWIM
b and *c* Pole Voltages of Inv-1
d and *e* Pole voltages of Inv-2

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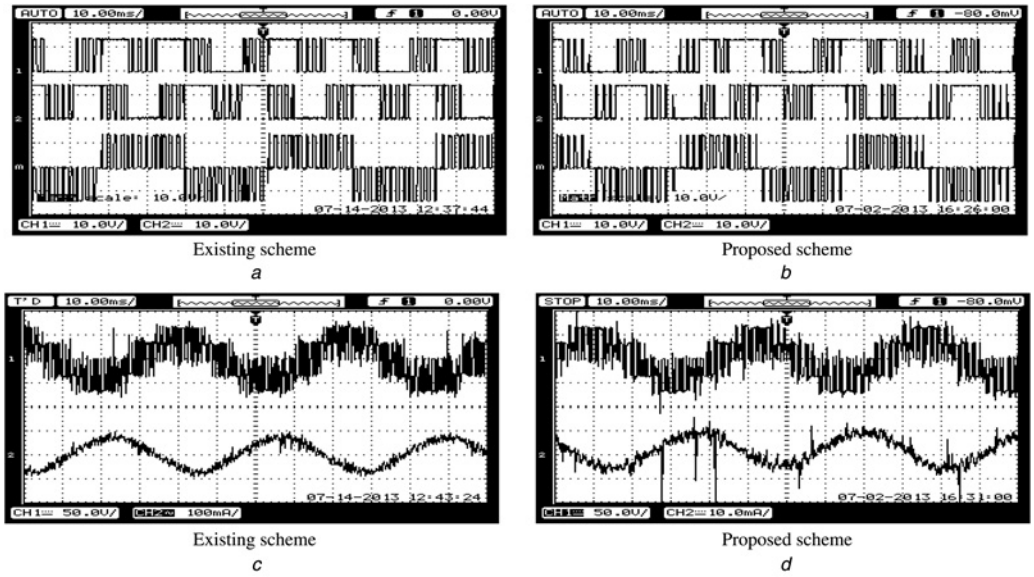

Fig. 6 *Gating pulses for the existing and proposed PWM schemes, top trace and middle traces shows the gating signals for Inv-1 and Inv-2 and the bottom trace depicts the difference of the pole voltage derived as a function of the difference of the gating signals*

a and *b* Gating pulses and difference of gate pulses
c and *d* Phase voltage and current with $m_a = 0.4$

prototype of Dual-Inverter fed 5-hp, three-phase OEWIM with *V*/*f* control which is built and validated experimentally using dSPACE platform. The switching device used in the inverter module is SEMIKRON make SPT IGBT module SKM 75GB128D. Figs. 5*b* and *c* shows the experimentally obtained pole voltages of Inv-1 and Inv-2 for alternate-SHC PWM scheme. Figs. 5*d* and *e* depicts the pole voltage of Inv-1 and Inv-2 for the proposed alternate-SHC scheme for loss minimisation.

It is observed from the Figs. 5*b* and *d* that the clamping and switching duties of Inv-1 and Inv-2 are same and also it depicts that the conduction and switching losses are predominant because of clamping the inverters to the DC-link in the existing PWM scheme [9]. In contrast to the existing scheme, from the Fig. 5*c* and *e* it can be noted that the clamping time interval is significantly higher for Inv-1 and Inv-2, which results in cooling of the power semi-conductor devices. Hence the proposed PWM scheme results in reduction in switching and conduction losses.

Figs. 6*a* and *b* depicts the gating pulses for the existing and proposed PWM schemes, respectively. In Figs. 6*a* and *b*, the top trace and middle traces shows the gating signals for Inv-1 and Inv-2 and the bottom trace depicts the difference of the pole voltage derived as a function of the difference of the gating signals. Figs. 6*c* and *d* illustrates the motor phase voltage and currents, respectively. In Figs. 6*c* and *d*, the top and the bottom traces indicates the motor phase voltage and the motor phase currents with modulation index (m_a) of 0.4, respectively. Figs. 7*a* and *b* shows the motor phase voltages with $m_a = 0.7$ for existing and proposed schemes, respectively. Similarly, Fig. 7*c* and *d* shows the motor phase currents with m_a of 0.7 for existing and proposed schemes, respectively.

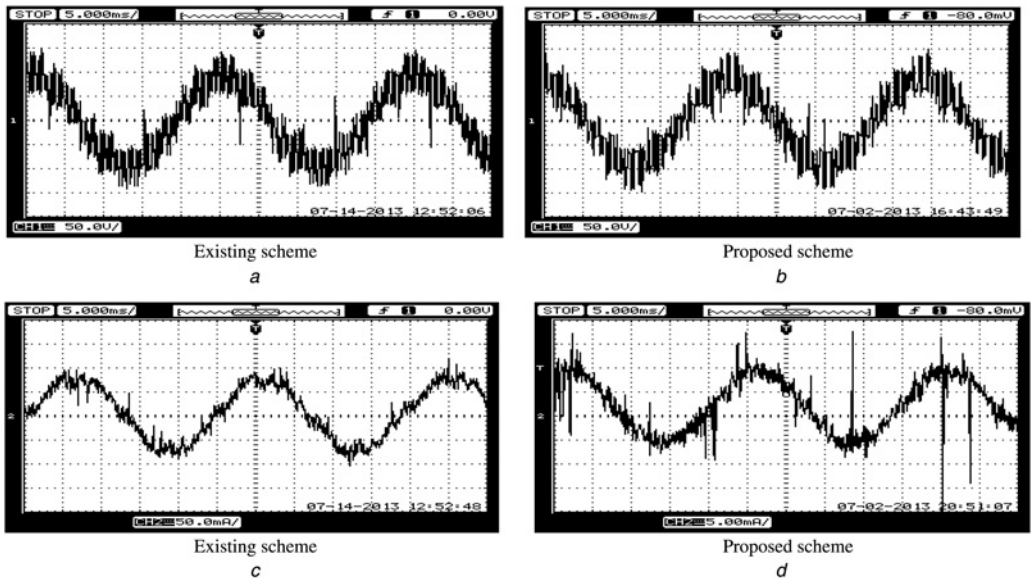

Fig. 7 *Motor phase voltages with $m_a = 0.7$ for existing and proposed schemes*

a and *b* Motor phase voltages and
c and *d* Phase current waveforms with $m_a = 0.7$

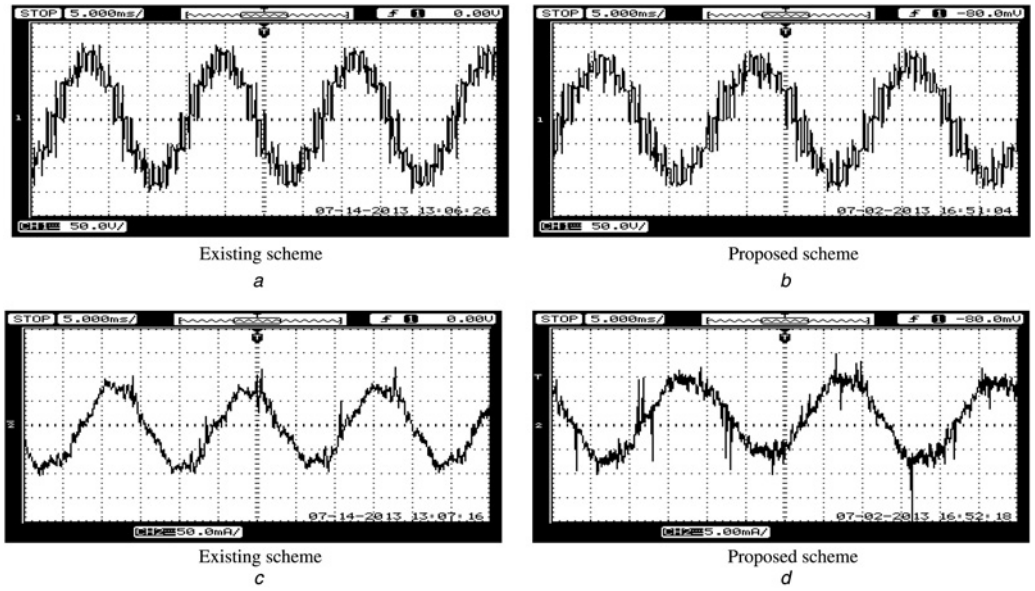

Fig. 8 *Experimental motor phase voltage waveforms for the existing and proposed scheme*

a and *b* Motor phase voltages and
c and *d* Phase current waveforms for over-modulation

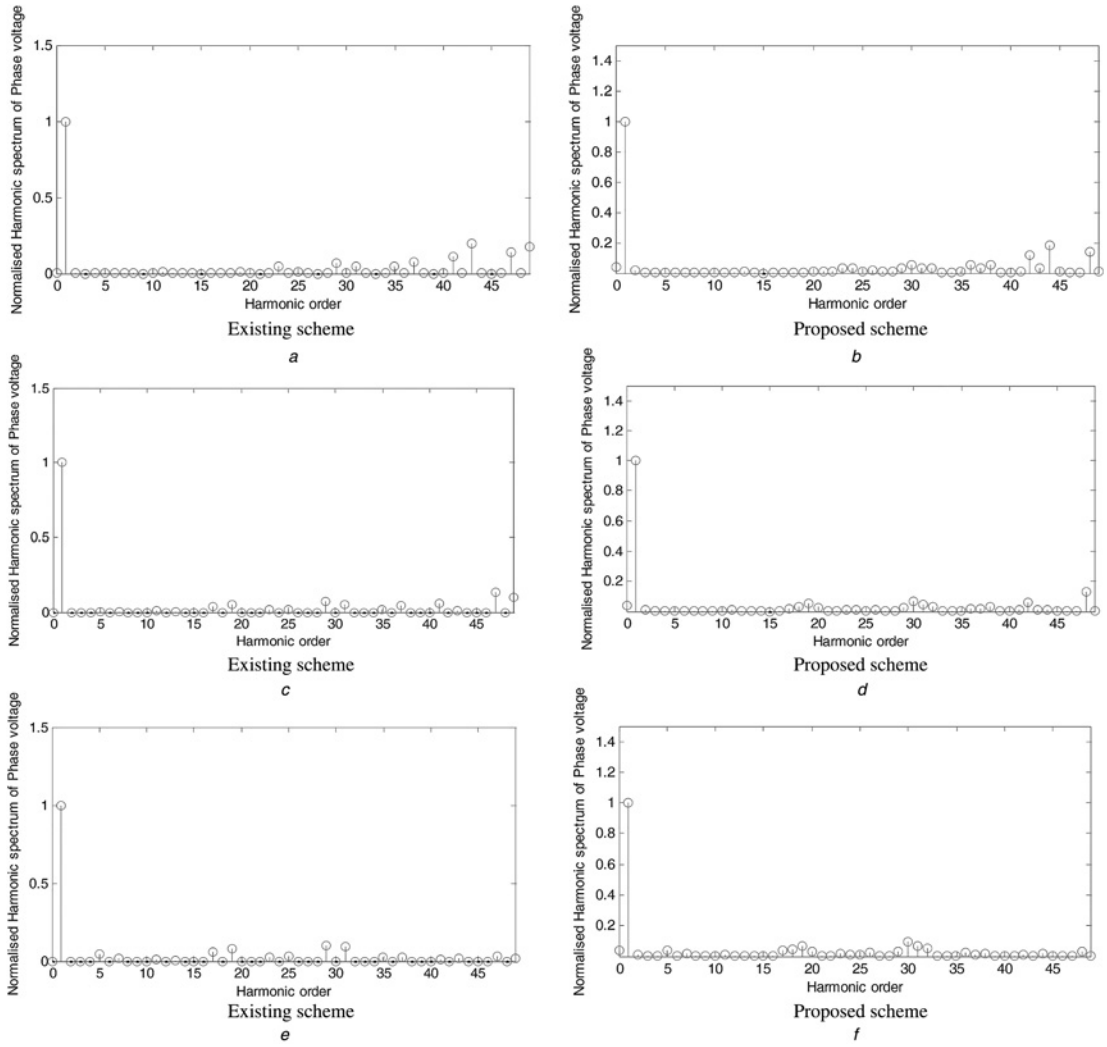

Fig. 9 *Normalised harmonic spectrum for motor phase voltage*

a and *b* with ma = 0.4
c and *d* with ma = 0.8
e and *f* with over-modulation

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Figs. 8*a* and *b* illustrates the experimental motor phase voltage waveforms for the existing and proposed scheme, respectively. Figs. 8*c* and *d* depicts the current through the motor phase-a winding for the existing and proposed scheme with over-modulation. The switching frequencies for a low power rating switching device are small as their switching speeds are comparably higher. Conversely, the switching transition time is high for high power rating switching devices on account of low switching frequencies to enable them for better thermal management characteristics. Two cases are compared in this work such as a high power rating switching device and low power rating switching device for a modulation index of ma = 0.4 with 48 samples. It is shown in [9] that either doubling the switching frequency with half the reduced modulation index or by reducing the switching frequency by half with doubled modulation index would result in same net losses. So, in this paper the rise in junction temperature under steady state conditions is carried out for a modulation index of 0.4 with 48 samples only. This is because of the clamping and the switching duties of the inverters.

Fig. 9 shows the normalised harmonic spectrum for various modulation indices of the motor phase voltage. Figs. 9*a*, *d* and *e* shows the spectral performance of the motor phase voltage for the existing scheme with modulation indices of $m_a = 0.4$, $m_a = 0.8$ and over-modulation region, respectively. Similarly, Figs. 9*b*, *d* and *f* shows the spectral performance of the motor phase voltage for the proposed scheme with modulation indices of $m_a = 0.4$, $m_a = 0.8$ and over-modulation region, respectively.

From experimental studies, it is observed that when Inv-1 is clamped; Inv-2 is switched for one complete cycle of operation. It is also observed that when Inv-2 is clamped, Inv-1 is being switched alternatively. Thus in one complete cycle, Inv-1 is clamped and Inv-2 is switched and in the subsequent cycle, Inv-2 is clamped whereas Inv-1 is switched. Thus both the inverters alternate their switching duty every cycle. Thus this PWM scheme ensures that all the active switching states are utilised, which also envisages that the complete switching resources are employed effectively in this PWM scheme rather than partial utilisation of the switching resources as mentioned earlier in the literature [9, 10].

Figs. 10–13 depicts the junction temperature rise and the power loss that occur in the considered high power slow switching device and low power fast switching device. Simulation studies are attempted in this paper to estimate the rise in junction temperature and power loss that occur in the considered power semi-conductor switches. The timing parameters for the considered for high power slow switching device and low power fast switching device are shown in Tables 5 and 6, respectively. During the experimentation, the measured ambient temperature is 30°C. Two two-level inverters along with an OEWIM are used in the experimental set up. The parameters of the motor are given in Appendix. The proposed SVPWM scheme is experimentally verified however the power loss and junction temperature rise for the considered two types of power devices are investigated using simulation studies using the existing RC-thermal network.

Figs. 10*a* and *b* shows the simulated waveforms of power loss and junction temperature of the top switch of the phase-a leg of Inv-1 for the considered high power slow switching device with an ON-state conduction drop of 2 V. Similarly Figs. 10*c* and *d* depicts the simulated graphs obtained for the power loss and junction temperature of the same leg of Inv-1 for the considered power device with 2 V ON-state drop, respectively. Figs. 11*a* and *b* depicts the waveforms for the power loss and junction temperature of the top switching device and Figs. 11*c* and *d* presents the waveforms for the power loss and junction temperature for the bottom switching device, respectively, of phase-a leg of Inv-1 for a conduction drop of 1 V for the considered high power slow switching device.

Figs. 12*a* and *b* depicts the simulated waveforms of power loss and junction temperature of the top switch of the phase-a leg of Inv-1 for the considered low power fast switching device with a ON-state conduction drop of 2 V. Similarly Figs. 12*c* and *d* shows the simulated graphs obtained for the power loss and junction temperature of the same leg of Inv-1 for the considered power semi-conductor device with 1 V ON-state drop, respectively. Figs. 13*a* and *b* depicts the waveforms for the power loss and junction temperature of the top switching device and Figs. 13*c* and *d* presents the waveforms for the power loss and junction

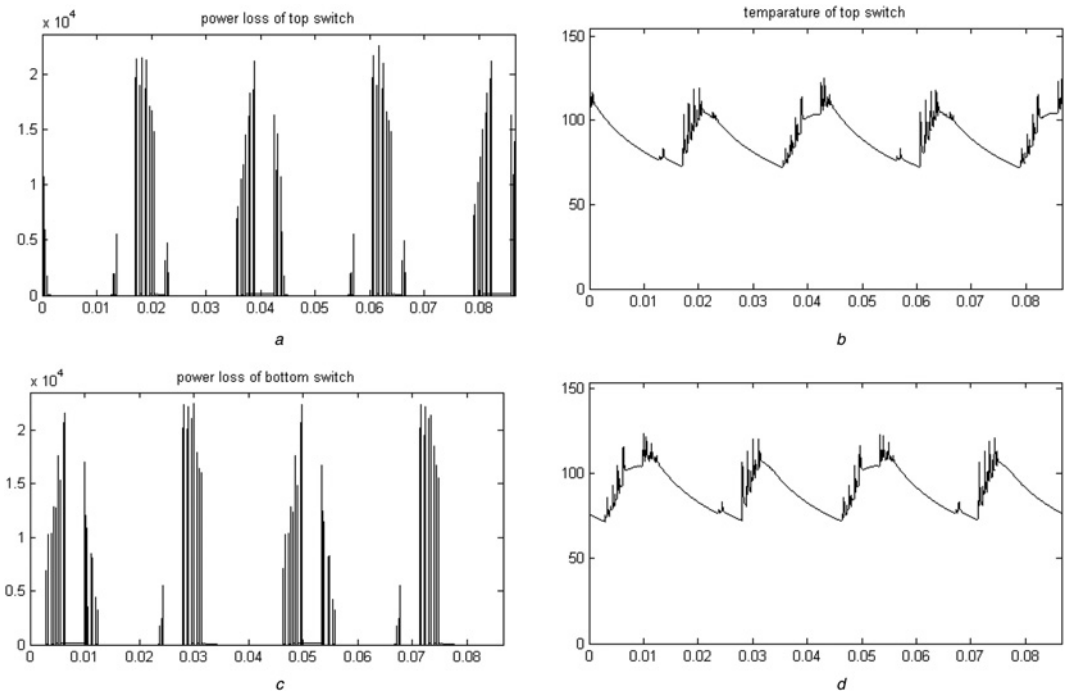

Fig. 10 *Temperature and power loss for Inv-1with $V_{cond} = 2$ V for high power slow switching device*

a Power loss of the top switch
b Temperature of the top switch
c Power loss of the bottom switch
d Temperature of the bottom switch

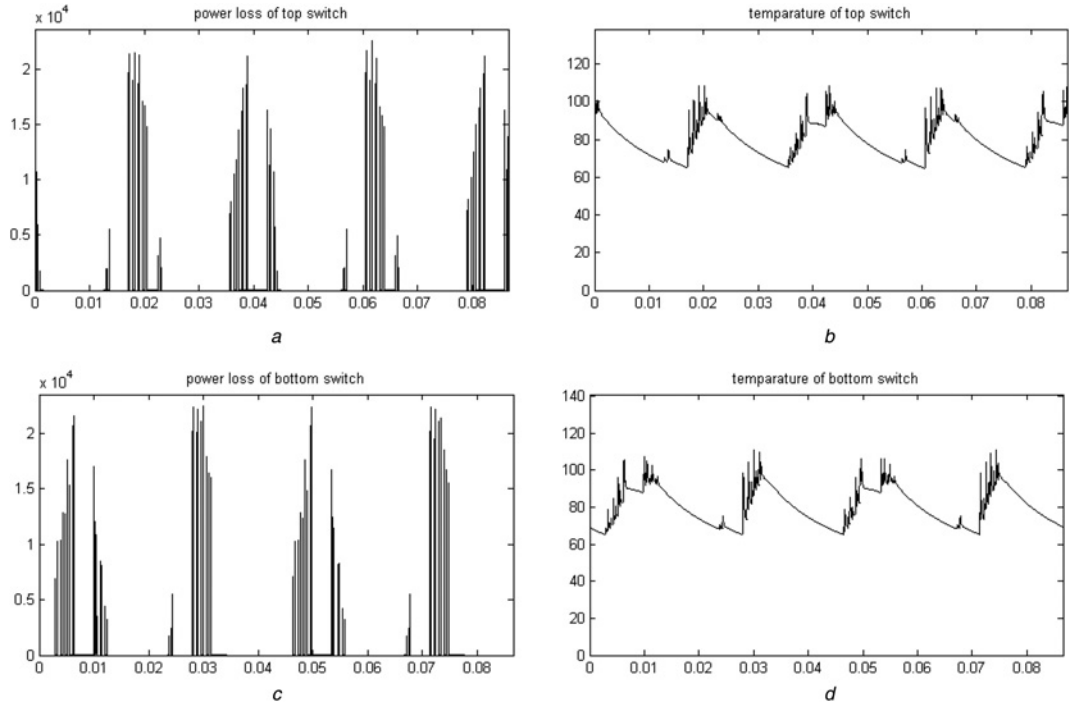

Fig. 11 *Temperature and power loss for Inv-1with V_{cond} = 1 V for high power slow switching device*

a Power loss of the top switch
b Temperature of the top switch
c Power loss of the bottom switch
d Temperature of the bottom switch

temperature for the bottom switching device, respectively, of phase-a leg of Inv-1 for a conduction drop of 1 V for the considered low power fast switching device.

From the subfigures (a) and (c) of Figs. 10–13 it is observed that for any device that during the switching transition there is a predominant loss that is occurring in the device and from the

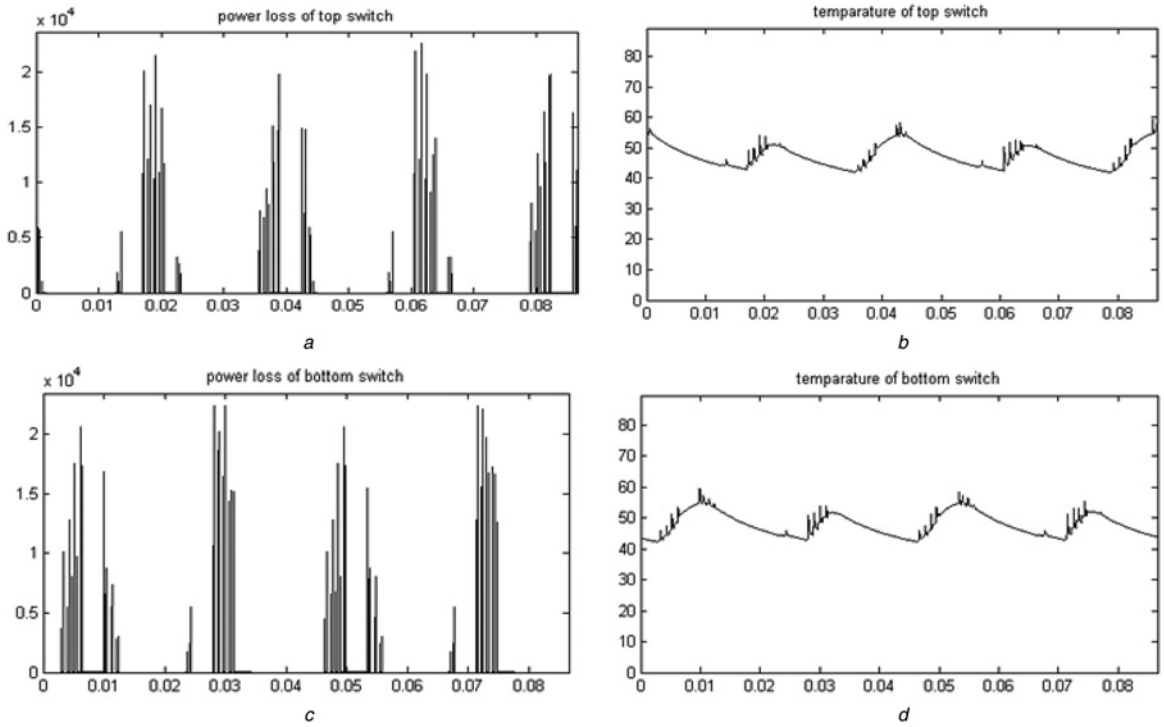

Fig. 12 *Temperature and power loss for Inv-1with V_{cond} = 2 V for low power fast switching device*

a Power loss of the top switch
b Temperature of the top switch
c Power loss of the bottom switch
d Temperature of the bottom switch

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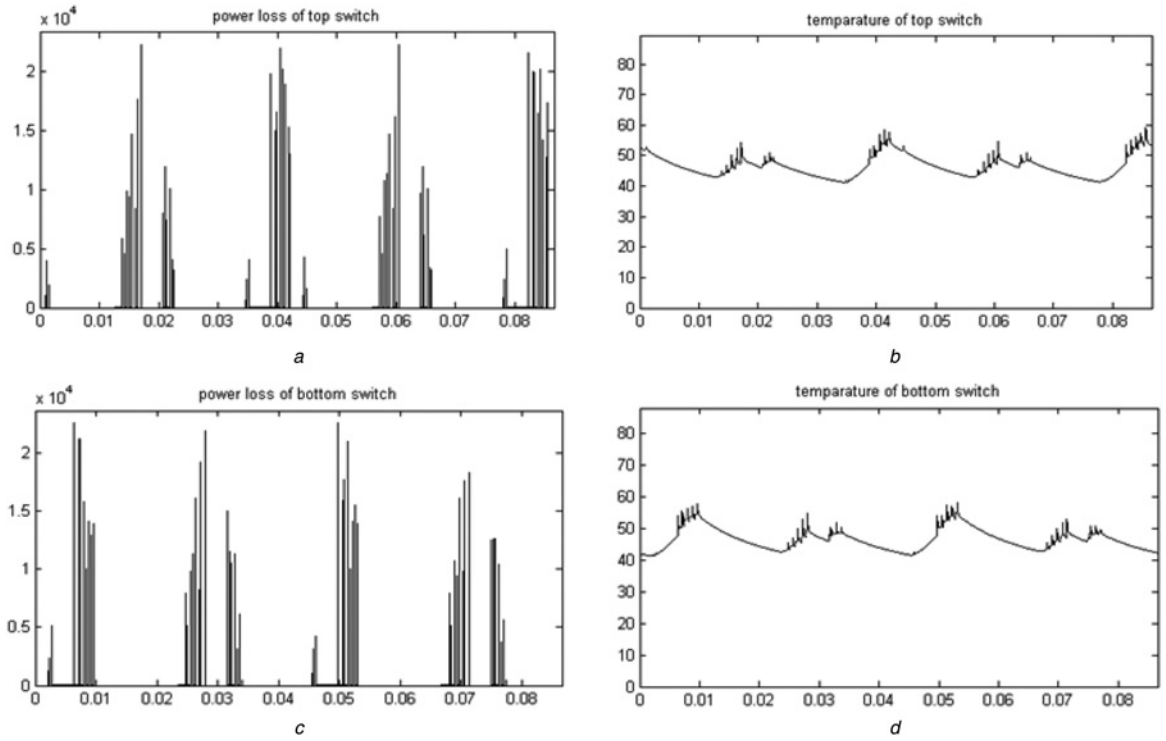

Fig. 13 *Temperature and power loss for Inv-1with V_{cond} = 1 V for low power fast switching device*

a Power loss of the top switch
b Temperature of the top switch
c Power loss of the bottom switch
d Temperature of the bottom switch

subfigures (b) and (d) of the same Figs. 10–13, it is observed that there is a rise in junction temperature which is because of the PWM pattern. Moreover, from the same figure, it is evident that the device temperature is on the falling side due the turn-OFF of the switch which is a better proposition of the proposed SVPWM scheme over the existing scheme [9, 10] where the device is clamped to the positive rail of the DC-link which does not necessarily allow the device to cool. It is because of this fact that the mean junction temperature of the considered high power slow switching device and low power fast switching device is lesser compared with the existing scheme presented in [10].

The simulated results of the maximum temperature rise, mean temperature rise and the power loss that occur in the top and bottom switch of both the inverters for the considered high power slow switching device and low power fast switching device for a modulation index of 0.4 with 48 samples assuming 2 and 1 V as the conduction drop are tabulated in Tables 5 and 6, respectively. The timing parameters are also shown at appropriate location just below the tables for the corresponding switching devices assumed. From Table 5 it is observed that for a conduction drop of 2 V, the average junction temperature of the top and bottom switching devices of Inv-1 are 89° and 90°C and for Inv-2 the junction temperature estimated is 88° and 88°C for the top and bottom switching devices. This is in contrast with the mean junction temperature obtained in [10], which is unequal because of the PWM pattern. Again from Table 5, for the assumed voltage drop of 1 V, the junction temperatures of the top and bottom switching devices of Inv-1 are 47° and 47°C and for Inv-2 are 48° and 48°C, respectively.

This same phenomenon can be noted in Table 6; that is, assuming a conduction drop of 2 and 1 V for the considered low power fast switching device, the mean junction temperatures of the top and bottom switches of Inv-1 are 57° and 57°C whereas for Inv-2 it is

Table 5 High power slow switching device

Modulation index, m_a = 0.4, Number of samples = 48		INV-1		INV-2	
		Top switch (A +)	Bottom switch (A –)	Top switch (A +)	Bottom switch (A –)
max temperature (degrees)	V_{cond} = 2 V	124.8616	123.7389	132.1550	128.1924
	V_{cond} = 1 V	108.4655	110.8796	117.4365	113.6621
average temperature (degrees)	V_{cond} = 2 V	89.7112	90.2460	88.5856	88.1204
	V_{cond} = 1 V	79.5372	80.2014	79.7422	79.3649
power loss (watts)	V_{cond} = 2 V	75.2019	76.0529	73.9457	73.2717
	V_{cond} = 1 V	62.3661	63.4032	62.7911	62.2472

Timing parameters assumed are: t_{ri} = 10 µs, t_{rv} = 10 µs, t_{fi} = 20 µs, t_{fv} = 5 µs; for high-power slow switching device.

Table 6 Low power fast switching device

Modulation index, m_a = 0.4, Number of samples = 48		INV-1		INV-2	
		Top switch (A +)	Bottom switch (A –)	Top switch (A +)	Bottom switch (A –)
max temperature (degrees)	V_{cond} = 2 V	76.0777	76.1518	73.9766	72.8109
	V_{cond} = 1 V	59.1973	59.4506	59.0712	58.0994
average temperature (degrees)	V_{cond} = 2 V	57.6410	57.9416	55.4666	55.4087
	V_{cond} = 1 V	47.3848	47.8180	46.5485	46.5805
power loss (watts)	V_{cond} = 2 V	34.8277	35.4205	32.3029	32.2037
	V_{cond} = 1 V	21.8877	22.6706	21.0540	21.0877

Timing parameters assumed are: t_{ri} = 2 µs, t_{rv} = 2 µs, t_{fi} = 4 µs, t_{fv} = 1 µs; for low-power fast switching device.

55° and 55°C, respectively. Again from Table 6, the mean junction temperature of the top and bottom switches for Inv-1 are 47° and 47° C and that for Inv-2 it is 46° and 46°C. These tabulated values suggest that in the proposed PWM scheme the device temperature is reduced compared with the existing scheme [10]. The disparity in junction temperature between the top and bottom switching devices within any phase leg of inverter [10] is also being addressed by the proposed SVPWM scheme.

From Tables 5 and 6 the power loss that incur in a switching device is tabulated. From Table 5 it is noted that the power loss in the top switch (75 W) and bottom switch (76 W) for Inv-1 and for Inv-2 top switch (73 W) and bottom switch (73 W) for the considered both high power slow switching device with a conduction drop of 2 V. Again from Table 5, assuming a conduction drop of 1 V, the power loss in top switch (63 W) and bottom switch (63 W) of Inv-1 and for Inv-2 the power loss in the top switch (62 W) and bottom switch (62 W) are noted. From Table 6 it is noted that the power loss in the top switch (34 W) and bottom switch (35 W) for Inv-1 and for Inv-2 top switch (32 W) and bottom switch (32 W) for the considered both low power fast switching device with a conduction drop of 2 V. Again from Table 6, assuming a conduction drop of 1 V, the power loss in top switch (21 W) and bottom switch (22 W) of Inv-1 and for Inv-2 the power loss in the top switch (21 W) and bottom switch (21 W) are noted. Thus from the simulation studies performed for the estimation of junction temperature and power loss in the power semi-conductor switches, it is evident that the proposed SVPWM scheme is better than the existing SVPWM scheme [10].

6 Conclusion

In this paper, a space vector-based PWM scheme is proposed. In this scheme, all the active vectors are used for clamping the inverters within two consecutive cycles resulting in improved utilisation of the switching resources. The proposed PWM scheme allows cooling of the switch intermittently during the conduction time intervals, which results in reduced junction temperature rise of the power semi-conductor devices. Thus the equalisation of the rise in junction temperature of the individual switches is reduced with an average value of 79°C for high power slow switching device with a power loss of 62 watt. Similarly for low power fast switching device the average junction temperature of 47°C with a power loss of 21 watt is obtained using the proposed PWM scheme which is significantly lesser than the existing scheme.

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8 Appendix

Motor Parameters

Rs = 6.564 V
Rs = 4.683 V
$x_{ls} = x_{lr} = 9.733\ \Omega$
Xm = 196.646 Ω
$J = 0.0131$ Jg m^2
$P = 4$

Parameters of the thermal model

$R_{1th} = 0.0265\ \Omega$
$R_{2th} = 0.3844\ \Omega$
$R_{3th} = 0.3844\ \Omega$
$C_{1th} = 13$ mF
$C_{2th} = 42$ mF
$C_{3th} = 163$ mF

Ratings of the device used in experimentation

Make: SEMIKRON
Device: IGBT
Model No: SKM 75GB128D
Voltage rating: 1200 V
Current rating: 70 A