POWER OPTIMIZED PLL IMPLEMENTATION IN 180nm CMOS TECHNOLOGY

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ABSTRACT

This paper describes the design of power optimized phase locked loop for frequency synthesis, Clock and Data recovery, carrier synchronization and many more communication and VLSI applications. PLL consist of Phase Frequency Detector, charge pump along with passive low pass filter and wide tuning VCO. A modified ring oscillator with tuning range of 280 MHz to 2.47GHz and phase noise of -112.4dBc/Hz at 1MHz offset is designed. Frequency Detector consist of DFF along with CMOS gates with low power architectures. Traditional charge pump, passive low pass filter, modified ring oscillator and divider for frequency synthesis offers less power and system noise. PLL proposed here has lock in range from 500MHz to 1GHz with output frequency ranging from 1GHz to 2GHz, maximum pull in time of 244ns and maximum power consumed is 252µW at 2GHz.

Keywords Phase Locked Loop (PLL), Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter, Voltage Controlled Oscillator (VCO), Pull-in Time

1 INTRODUCTION

The Phase frequency detector (PFD) forms the first component of PLL which is designed for high speed application by reducing the dead zone. The architecture of PFD has two D flip flops working in tandem to produce an output signal depending upon phase difference of inputs. Further, charge pump along with passive low pass filter transforms oscillating output of PFD to dc voltage requirement of VCO.VCO decides acquisition range of PLL. The VCO curve has to be monotonic to be employed in PLL.

This paper gives PLL system design with operating range of 1GHz to 2GHz which is decided by tuning range of VCO. Generally speaking PLL with high tuning linearity, wide Here we have opted for passive low pass filter which not only reduces system noise but power consumption as well Bandwidth and low noise is preferred and in accordance to application different design architectures are used.VCO and active low pass filter are main noise sources in our PLL.

2 BASIC PLL SYSTEM

The basic architecture for PLL.PLL contains PFD, Charge pump, VCO, Loop filter and optional Divider block is shown in Fig.1.

2.1 Phase Frequency Detector

The basic function of PFD is to detect the phase or frequency difference between two input frequencies and generate error signal proportional to difference in phase or frequency. . Here we have used the conventional DFF architecture for designing PDF as shown in Fig.2. When reference frequency leads the frequency

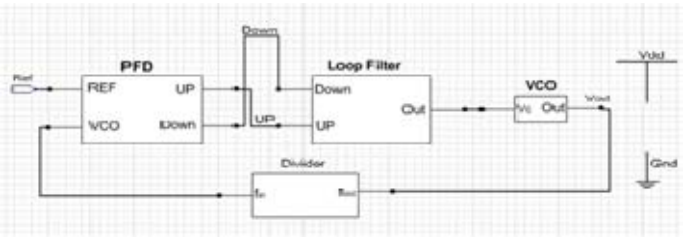

Fig. 1.Basic PLL Architecture

From divider UP signal is generated and vice-versa case generates the DOWN signal of various lengths totally relying on amount of phase variation of input frequencies. CMOS NAND and NOT gate is used in reset circuitry so that if both the input frequencies phases match (UP=1 and DOWN=1) then both FFs are reset to zero.

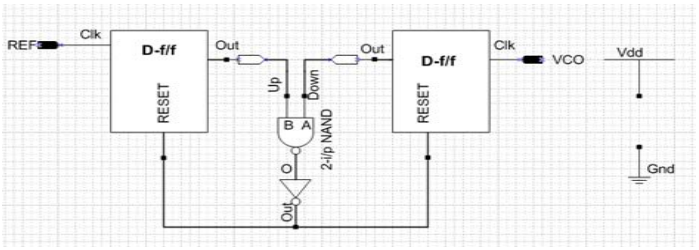

Fig 2. Phase Frequency Detector

2.2 Charge Pump

Charge pump converts the UP and DOWN signals generated by PFD into corresponding current values. Charge pump is followed by the loop filter. Charge pump either pumps current into loop filter or pump out the current from loop filter. The circuit of charge pump design along with loop filter is shown in Fig. When UP is high M2 is on and charge pump will pump current in loop filter thus increasing the control voltage, similarly when DOWN is high M3 will be on and current will be drawn out from loop filter and leading to drop of control voltage.

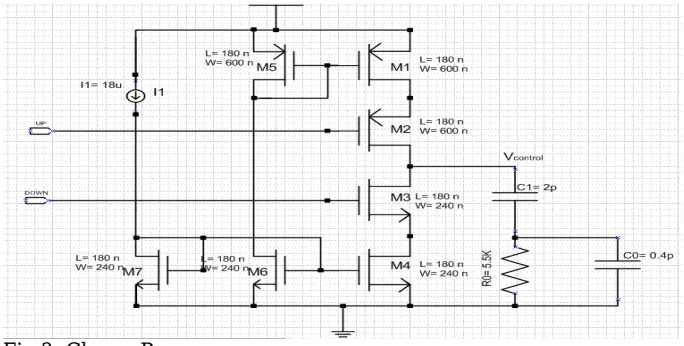

Fig 3. Charge Pump

2.3 Loop Filter

The main function of loop filter is to convert signal from PFD to a ripple free DC control voltage. Loop filter is low pass filter which plays important part in stabilizing of our entire system as shown in Fig. Values of C1, C2and R are given by [6]

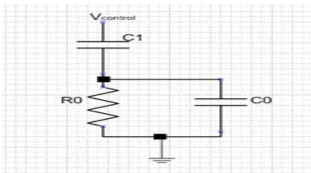

Fig 4. Loop Filter

Values of C1, C2and R are given by [6]

$$C1 = \frac{1}{W_{c}^{2}}\left(\frac{I_{cp}}{2\pi}K_{vco}\right) \quad \text{.................. (2)}$$

$$R = \frac{1}{Q}\sqrt{\frac{2\pi}{C1 I_{cp} K_{vco}}} \quad \text{............... (3)}$$

C1=5C0 . ... (4)

2.4 Voltage Controlled Oscillator

VCO generates variable frequency signals according to input voltage applied to it. VCO alters its output frequency on the basis of variation in control voltage which explicitly depends on input phase variation. Fig.7 shows modified structure of a ring oscillator. This VCO generates high frequency signals with low power consumption with operating frequency range from 280MHz to 2.47GHz.It consumes 39 µW at 1GHz and 56 µW at 2GHz.

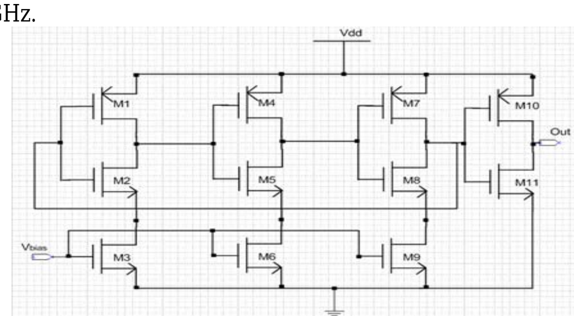

Fig 5. Voltage Controlled Oscillator

2.5 Divide by 2 circuit

It is nothing but the DFF where inverted output of DFF is connected back into DFF input and frequency which is to be divided is applied at clock in of DFF. It consumes 18µW at 1GHz and 28 µW at 2GHz input frequencies.

3 RESULT DISCUSSION

The designed VCO has tuning range from 280MHz to 2.1GHz. Fig 6.shows the characteristic curve for VCO.

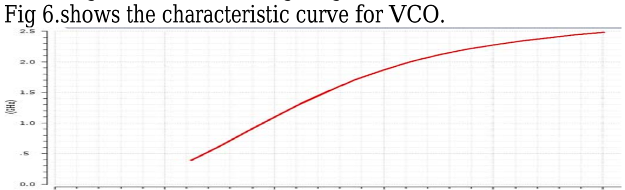

Fig 6. Control voltage curve V/S Frequency

The Fig.7 depicts control voltage response with time. It shows pull in time required for PLL to establish locked state with corresponding VCO input before it stabilizes. From here we can say that it requires about 244ns For PLL to acquire lock state and control voltage eventually stabilizes at 1.108V

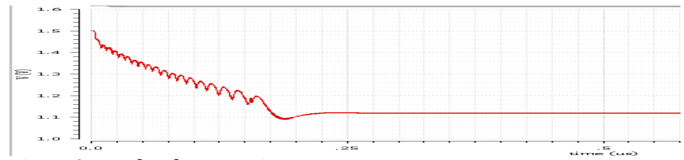

Fig 7. Control voltage vs time curve

Fig.8 shows the average power dissipation at 2GHz VCO output across whole PLL system and estimated power consumption is noted to be 252µW.

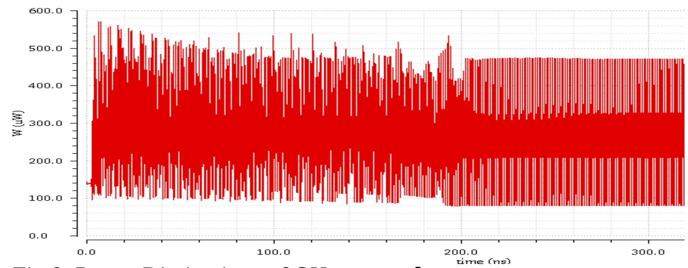

Fig 8. Power Dissipation at 2GHz output frequency

4 CONCLUSION

This paper demonstrates design of Phased locked Loop system optimized for low power applications. The use of basic and simplistic architecture is used with low transistor count to achieve average power dissipation as low as 252 µW at 2 GHz operation. The reduction in power is also due to voltage scaling, we can reduce power more by using supply voltage below 1.5 V .The pull in time required for PLL to settle is reduced to 244ns. Phase noise of -112.4dBc/Hz is achieved by using VCO configuration of modified ring oscillator. Thus with low power , low pull-in time and good phase margin this type of PLL can be used for EEPROM,EEROM,FPGA and wireless LAN applications.

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