A 10-bit 25MSPS Low Power Pipeline ADC for Mobile HDTV Receiver System

Krushna Dongre
Department of Electronics and Tele-Communication Engineering
Yeshwantrao Chavan College of Engg Nagpur, Maharashtra, India
kru.don@gmail.com

Rahul kamdi
Department of Electronics and Tele-Communication Engineering
Yeshwantrao Chavan College of Engg Nagpur, Maharashtra, India
rahulkamdi19@gmail.com

Pratik Akre
Department of Electronics and Tele-Communication Engineering
Yeshwantrao Chavan College of Engg Nagpur, Maharashtra, India
pratikakre2009@gmail.com

K. Sarangam
Department of Electronics and Communication Engineering
National Institute of Technology,Warangal
sarangam.nitw@gmail.com

Abstract- **This paper describes a 10-bit 25MSPS analog-to-digital converter (ADC) for Mobile HDTV Receiver System. The ADC is based on a 4-3-3 bits- per-stage pipeline architecture and The proposed pipelined ADC adopts a optimized stage resolution based on power consumption of sample and hold circuit and comparator. At the target sampling rate of 25MS/s, measured results show that the converter consumes 12.36mW from a 1.8V power supply and 56dB SNR and 60dB SFDR.**

Keywords:- **HDTV Receiver, ADC, Low power**

1. INTRODUCTION

The digital back-end circuit in Mobile HDTV receiver system uses DVB-H (Digital Video Broadcasting-Terrestrial) system [1, 2]. This has led to a demand for cheaper, higher performance analogue tuners, analogue-to-digital converters (ADCs), coded orthogonal frequency division multiplexing (COFDM) digital demodulators and other chipsets targeted at consumer digital television [3].

Mobile DVB, presently called DVB-H, is still in the process of standardization and will allow mobile phones and personal digital assistants (PDAs) to receive DVB programs on the move. As these handheld devices are battery operated, the minimization of power consumption will be a key requirement.

This paper presents the design of a 10-bit, 25MS/s ADC suitable for the digitization of the RF tuner output prior to COFDM demodulation for DVB-H. The converter employs a 4-3-3-stage differential pipeline architecture and dissipates 12.36mW from a single 1.8V power supply. The rest of the paper is organized as follows. Section 2 gives an overview of DVB-H and derivation of system level specification Section 3 describes the ADC architecture and the 4-bit flash ADC core on which the pipeline is based. Section 4 focuses on circuit design issues for the 10-bit ADC sample-and-hold amplifiers (SHAs), comparators, digital-to-analogue converter (DAC) and gain/buffer amplifiers. Simulated results are presented in Section 5, and conclusions are drawn in Section 6.

The TSMC 180nm mixed mode process is used in this paper and all of the simulations are done in LTspice. As such, for the fastest slew-rate, the smallest channel length of L = 1 (180 nm) will be used, and at this length, the device is in the short channel regime and will require short channel topologies.

The 180 nm process characterization is given in Table 1.

PARAMETER	NMOS	PMOS
Bias current I_D	30uA	30 uA
W/L	20/2	40/2
Actual W/L	3.6u/0.36u	7.2u/0.36u
$V_{DS,SD,sat}$	110mV	115 mV
$V_{ovn,p}$	90mV	90 mV
$V_{GS,SG}$	600mV	650mV
$V_{THN,P}$	510mV	560mV
$Dv_{THN,P}/DT$	-0.4V/C^o	-0.4V/C^o
$V_{satn,p}$	135e3 m/s	113e3 m/s
t_{OX}	4.1 nm	4.1 nm
C'_{OX}	8.57 fF/um^2	8.57 fF/um^2
$C_{oxn,p}$	11.1 fF	22.2 fF
$C_{qs,sq}$	7.4 fF	14.8 fF
$C_{qd,dq}$	2.96 fF	4.57 fF
$g_{mn,p}$	343 uA/V	231 uA/V
$r_{on,p}$	275 k	437 k
$g_m r_o$	94.3	101
λ	0.12 V^{-1}	0.093 V^{-1}
f_T	4.7 GHz	2.0 GHz

Table. 1. TSMC 180 nm device characterization.

2. DVB-OVERVIEW AND SYSTEM LEVEL SPECIFICATION

DVB is classified into 3 transmission specifications namely DVB-S (S for satellite), DVB-C (C for cable) and DVB-T. The new DVB-H specification allows DVB-T services to be available to mobile and hand held devices. The new DVB-H is extension of DVB-T with advanced forward error correction (FEC) algorithms to facilitate signal reception at very high achieved for the design, making it the most energy efficient speeds, with less silicon implementation overhead and lower power consumption (DVB-H reception has recently been verified to be consistent in quality at up to Mach 1 speeds with a 5-9 dB carrier-to-noise advantage over DVB-T [3]).

DVB-H is specified for 1.7, 5, 6, 7, 8, and 10 MHz channel bandwidth. Hence the minimum sampling frequency must be greater than twice the maximum bandwidth. Commercially available demodulator use a 20.45 MHz clock, hence 25 MHz is suitable for sampling.

The input SNR requirement for COFDM is 60dB [2].

$$ENOB = (SNR-1.76 -10\log (fs/2B))/6.02$$
$$= 9.5$$

Hence the ENOF (effective no. of bits) is 9.5, which makes 10bits resolution an absolute choice.

3. ADC ARCHITECTURE

The application requires medium resolution, high speed and low power consumption. The pipelined ADC is a popular topology for resolution on the order of 8 to 14 bits and sampling rates between a few MSps to hundreds of MSps [4,5].

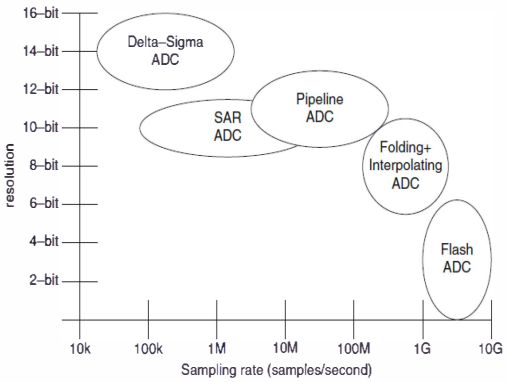

Fig.1 ADC ARCHITECTURE COMPARISON

Choice of no. of bits per stage depends on power consumption of Sample and Hold circuit and comparator. Making bit resolution/stage less and no. of stages more will make power consumption by sample and hold dominates the overall power consumption while high bits resolution will make power consumption of comparators dominate [6, 7]. Sample and Hold circuit and comparator in this work consume 1.3mW and 120uW respectively. From this available data power consumption for different combination of bits/stage is estimated. The combination 4-3-3 bit per stage consumes less power than any other combination.

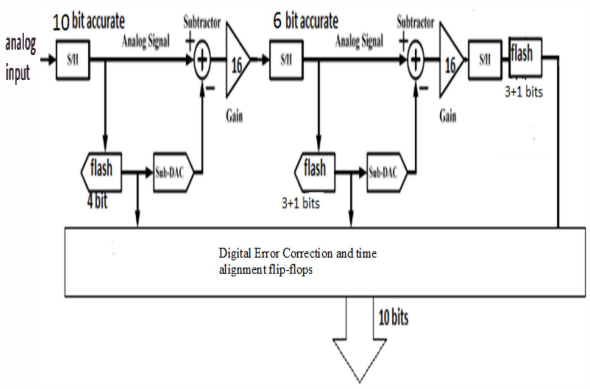

Fig. 2 pipelined ADC architecture (4-3-3) block diagram

The first stage is a full 4-bit, fully differential ADC. The second and third stages utilize a 3+1-bit ADC, the extra bit used for digital error correction thus allowing for the relaxation of the quantization DAC and comparator accuracy specification from +/-1/2LSB to +/-1LSB without any performance impact. A differential subtractor stage provides the quantization error, which is then amplified (×16) by the gain stages. The three SHAs allow the three stages to concurrently process different signal samples, thus enabling high throughput, albeit at an initial three-clock-cycle latency. This latency however is only an issue if the ADC is intended for use in a feedback control system, which is not the case with DVB applications. Further reduction in power consumption is achievable with the use of more pipeline stages but this will increase the latency, thus preventing the ADC from potentially being used as a 3-step ADC at lower sample rates.

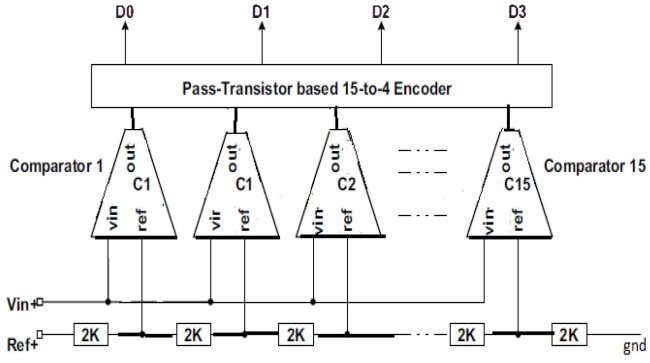

Fig.3 4 BIT FLASH ADC

Fig. 3 is an abridged diagram of the 4-bit flash ADC core. A fully differential path is utilized for both the signal and reference input with two resistor ladders establishing the differential thresholds for each comparator. Fifteen 4-input comparators are used, with digital logic used for bubble removal. A ROM-like pass transistor based on a 15-to-4 encoder is then used to convert the thermometer-code output of the comparator bank to binary nibbles. The pass-transistor approach was chosen to allow for high-speed operation, uniformity in the propagation delay for each output bit and a more compact physical layout. The 4-bit ADC was clocked at a maximum clock rate of 25MS/s whilst still achieving an

accuracy of up to 10-bits over process, temperature and supply variations

4. ADC CIRCUIT DETAILS

The design of different constituent blocks of the 10-bit pipelined ADC is described in this section. The different blocks are sample and hold circuit, comparator, residue amplifier, and DAC.

4.1. SAMPLE AND HOLD CIRCUIT

The op-amp is operating in a unity-follower configuration in which both inputs of the op-amp are held at V_{CM}. At this particular instance in time, prior to the amplifier is said to be operating in the sample mode of operation.

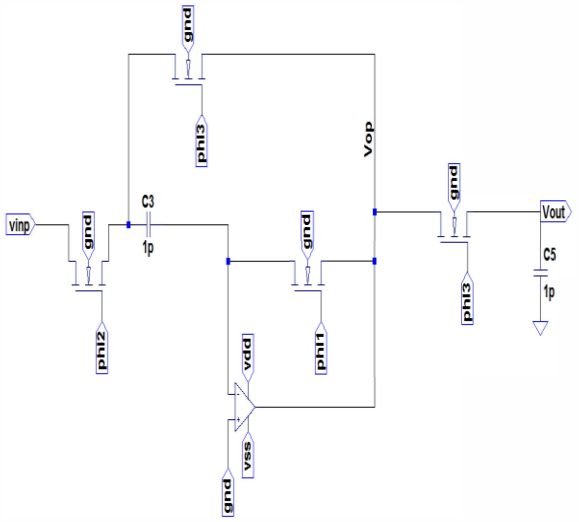

Fig. 4 Sample and Hold circuit

At t1the phi 1, switches turn off. The resulting charge injection and clock feedthrough appear as a common-mode signal on the inputs of the op-amp and are ideally rejected. Since the top plates of the hold capacitors (the inputs to the op-amp) are always at VCM, at this point in time the charge injection and clock feedthrough are independent of the input signals. This produces an increase in the dynamic range of the sample-and-hold (the minimum measurable input signal decreases). The voltage on the inputs of the op-amp (the top plate of the capacitor) between t1 and t2 is V0FFI + VCM, a constant voltage. Note that the op-amp is operating open loop at this time so the time between t2 and t3 should be short.

At t2 the phi2 switches turn off. At this point in time, the voltages on the bottom plates of the sampling (or hold) capacitors (polyl) are vin. The voltages on the top plates of the capacitors (connected to the op-amp) are V0FFl + V0FF2 + VCM (assuming that the storage capacitors are much larger than the input capacitance of the op-amp). The term V0FF2 is ideally a constant that results from the charge injection and capacitive feedthrough from the phi2 switches turning off. The time between t1 and t2 should be short compared to variations in the input signals.

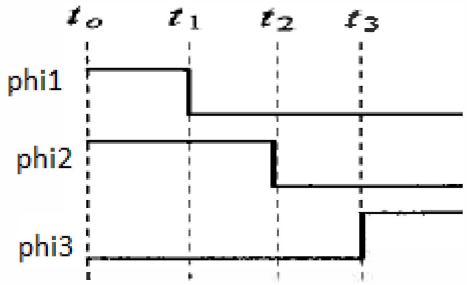

Fig. 5 Timing diagram for Sample and Hold

At time t3 the phi3 switches turn on and the op-amp behaves like a voltage follower; the circuit is said to be in the hold mode of operation. The charge injection and clock feedthrough resulting from the phi3 switches turning on causes the top plate of the capacitor to become *V0FFl + V0FF2 + V0FFi + VCM*, again assuming that the storage capacitors are much larger than the input capacitance of the op-amp. The outputs of the sample-and-hold are Vinp.

4.2. PREAMPLIFIER BASED COMPARATOR

It is required in 4 bit flash. The sampling time

Ts=1/25M=40ns

One fourth of sampling time is taken as delay of comparator

DELAY=40ns/4

=10ns

Now,

LSB =1.2V/(2^4)

=75mV

The comparator has to resolve at least fourth part of LSB

Resolving capability=19mV

For DNL to be less than one fourth of LSB

|DNL|=Vref/2^N*|Δ Ri/R|max +2|Vos |max

Vos maximum value is 14mV.

This much propagation delay with low power is obtained only with positive feedback preamplifier based comparator [8].

This circuit consists of three part.

1. Preamplification

For the preamplification (pre-amp) stage, we chose the circuit of Fig. 6. For this first section we'll use the long-channel CMOS process to illustrate the design procedures. This circuit is a differential amplifier with active loads. The sizes of Ml and M2 are set by considering the diff-amp transconductance, gm, and the input capacitance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the sizes of Ml and M2. Notice that there are no high-impedance nodes in this circuit, other than the input and output nodes. This is important to ensure high speed. Using the sizes given in the schematic, we can relate the input voltages to the output currents.

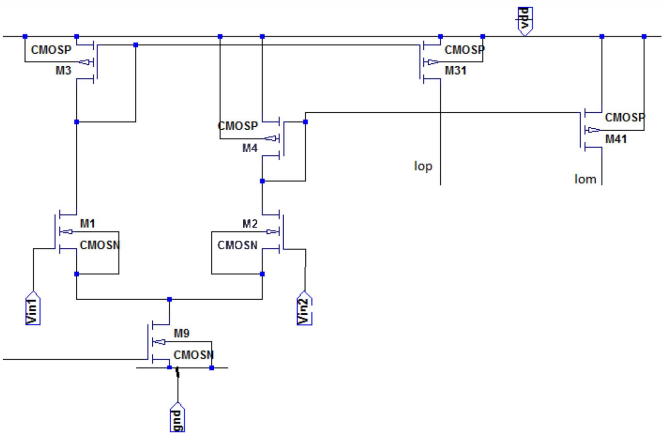

Fig.6. Preamifier

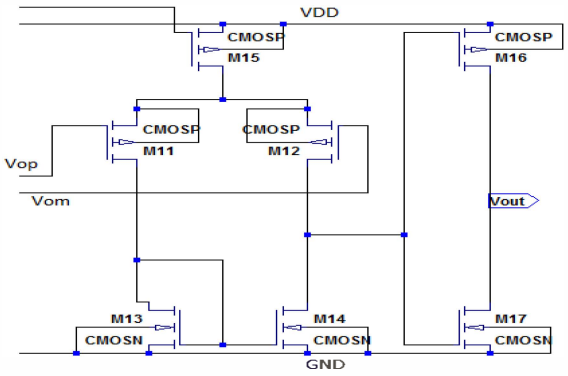

Fig.8 Output Buffer.

2. *Decision Circuit*

The decision circuit is the heart of the comparator and should be capable of discriminating mV-level signals. We should also be able to design the circuit with some hysteresis for use in rejecting noise on a signal. The circuit that we use in the comparator under development is shown in Fig. 7. The circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element.

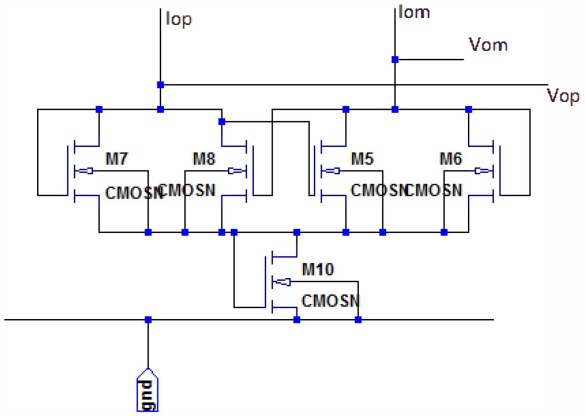

Fig.7. Decision Ckt.

3. *Output Buffer*

The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or VDD). The output buffer should accept a differential input signal and not have slew-rate limitations.

4.3 OPAMP for SAMPLE AND HOLD CIRCUIT

Opamps are required as gain buffer in sample and hold circuits. Accuracy of ADC depends on various parameter of Opamp such as DC gain, Slew Rate, UGB [9].

First Stage Sample and Hold

For accuracy of one forth of LSB for 10 bits the dc gain Opamp required is

DC gain=1/accuracy
=1/0.25 LSB
$=2^{N+2}$
$=2^{12}$
=4096 watt
Gain in dB=20 $\log_{10}(4096)$
Gain in dB=72.3dB
=73dB

Now bandwidth, to settle the output within time‘t’, the output of OTA must reach to settle state -1/2 LSB and ½ LSB

Precision of s/h = output of OTA

$1/2^{N+1}$ = 1-Vout/ (Vout-ideal)
=exp (-t/τ)
T =1/ ($2\Pi\beta f_u$)
Fu =(f_{clk} ln(2N+1))/ $2\Pi\beta$

For β =1 and
F_{clk} =25MHz
N=10 bits

Fu=30.4MHz
=31MHz

Slew rate is rate of change output. But output of OTA never changes to full range. Let the change be 1V in 20ns
Hence the slew rate required is

Slew rate= 1/20ns
=50V/us

Stage no.	DC gain	UGB	Slew rate
Stage 1	72dB	31MHz	50V/us
Stage 2	54dB	25MHz	50V/us
Stage 3	54dB	25MHz	50V/us

Table 2. Specification of Opamp in Different Stages

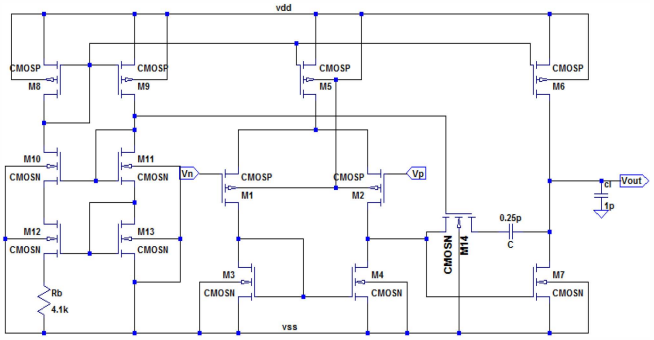

Fig. 9. Two stage Opamp as gain buffer

For low power consumption two stage Opamp is best option the gain buffer, miller compensation is used to get desired Phase margin to get settling time and stability.

5. SIMULATION RESULTS

The converter was designed in a 0.18um CMOS technology. BSIM3v3.1 models were used for the MOS devices.

Table 3 shows the power consumption of Opamp in each stage.

Stage no.	DC gain	Power dissipation	UGB	SLEW Rate
Stage 1	>73dB	1.56mW	31MHz	75V/us
Stage 2	>60dB	1.02mW	30MHz	60V/us
Stage 3	>60dB	1.02mW	30MHz	60V/us

Table 3 Opamp results

Delay	5ns
Resolving capabilities	9mV
offset	19mV
Power dissipation	112.2uW

Table 4. Comparator results

Table 4 shows the result of comparator.

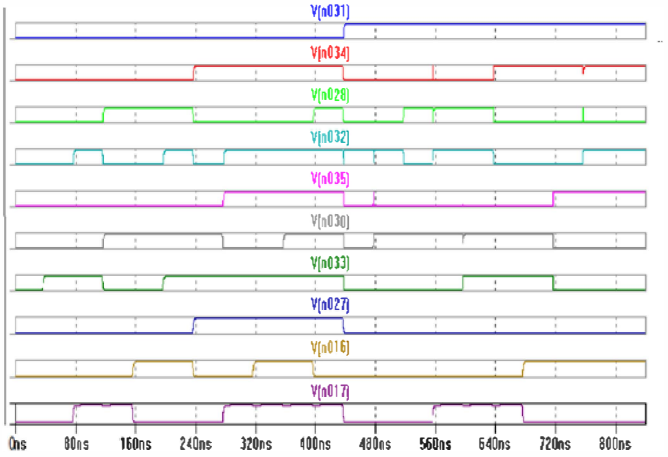

Fig. 10 Output of the ADC for ramp input

Fig. 11 shows the power dissipation of ADC. The overall power consumption of ADC is 12.36mW @ supply of 1.8V

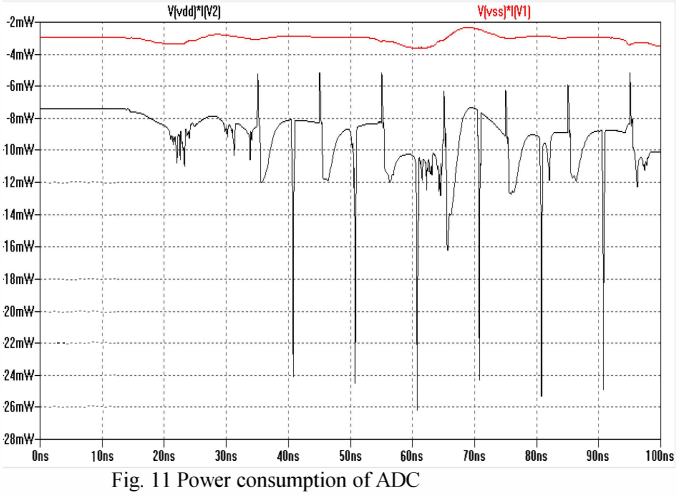

Fig. 11 Power consumption of ADC

Technology	TSMC 180nm
Resolution	10 bits
Conversion Rate	25Ms/s
Input Range	1Vpp
Power Consumption	12.36mW
ENOB	9.5

Table 12. Summary of Performance

Reference	Supply	Power Consumption
This work	1.8V	12.36mW
[4]	2.8V	19.5mW
[10]	1.4V	21mW
[11]	2.0 V	16mW
[12]	3.0 V	60mW

Table 13. Comparison between different ADC

6. CONCLUSION

The design of a 1.8 V 10-bit CMOS pipeline ADC for Mobile HDTV Receiver System (DVB-H) has been presented. Optimized bits per stage helps to reduce the power consumption. Power consumption for this architecture is less than 12.5mW.

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