IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Dual frequency inverter configuration for multiple-load induction cooking application

ISSN 1755-4535
Received on 13th February 2014
Accepted on 22nd October 2014
doi: 10.1049/iet-pel.2014.0114
www.ietdl.org

Sharath Kumar Papani ✉, *Vishwanathan Neti*, *Bhagwan K. Murthy*

Department of Electrical Engineering, National Institute of Technology, Warangal, AP, India
✉ *E-mail: sharathphd@gmail.com*

Abstract: Induction cooking application with multiple loads powered by suitable power converters and appropriate control technique needs attention. This study proposes dual frequency operated full-bridge inverter for multiple-load induction cooking. This inverter simultaneously powers two series resonant circuits. Each series resonant circuit is for one induction cooking load. This technique provides constant switching frequency operation for individual loads with asymmetrical duty cycle control. Output power of each load is independently controlled. The proposed inverter configuration and control technique is simulated and experimentally tested for two loads. Simulation and experimental results are in good agreement. This technique can be extended to more than two loads.

1 Introduction

Induction cooking is one of the several applications of induction heating. It is a better heating technique than conventional heating techniques. In induction heating, heat is developed inside the load by the generation of eddy currents at skin depth levels from the surface. Skin depth (δ) is expressed as

$$\delta = \sqrt{\frac{\rho}{\pi f_s \mu}} \tag{1}$$

where ρ is the electrical resistivity, μ is the magnetic permeability of the load material and f_s is the switching frequency of the inverter.

A high-frequency (HF) AC source is needed for induction cooking. Series resonant inverters are commonly used for generation of HF AC for this application. Quasi-resonant, half-bridge and full-bridge resonant inverter configurations are generally used [1–5]. Full-bridge resonant inverter is used for high-power applications. Control of output power of these resonant inverters can be achieved by certain methods such as pulse-amplitude modulation, pulse-frequency modulation, phase-shift control, asymmetric voltage cancellation (AVC), asymmetric duty cycle (ADC) control and hybrid control technique [6–13]. All these proposed methods have their advantages and disadvantages.

In the recent past, certain inverter configurations have been proposed for multiple-load induction cooking application. Main objectives of multiple-load induction cooking application are reduction in components count, simple and independent control of each load, and high conversion efficiency. An inverter with two loads is proposed and analysed in [14]. This method has one master and one slave load. It uses several resonant capacitors connected in parallel with electro-mechanical switches. Control of load power is achieved by activating these electro-mechanical switches. Large number of capacitors and use of electro-mechanical switches are the disadvantages of this method. In [15], an inverter configuration for two-loads is presented which has three legs (six switching devices). One leg of the inverter is common for both loads. It offers independent control of each load with high efficiency. It also offers reduced components count and better utilisation of the devices. AVC control technique is adopted for power control. In [16], two-output induction cooking with power factor correction is proposed. Power control of each load is done by AVC control technique. In [17], a load-adaptive control algorithm is used for variable load and large output power range. Aspects like, efficiency, acoustic noise and flicker control are considered in the design stage. For different ranges of output power, different control techniques are adopted. Although certain objectives are met, it makes the control structure more involved. To improve light-load performance, discontinuous conduction mode control is adopted in [18]. It uses variable frequency in the range 20–150 kHz. It improves the light load efficiency to 95% but the variable frequency operation is the limitation of this technique. Digital implementation of induction heating load is proposed in [19]. An AC–AC power conversion technique is presented in [20] for multiple induction heating system. It has higher efficiency, reduced components count and reduced complexity. It uses a variable frequency control, which is the limitation of this method.

In most of the above papers, power configurations are either with larger components count or variable frequency control is adopted for performance improvement. It appears that still there is enough scope for improvement in multiple-load induction heating cooking systems. In this paper, an attempt is made to propose an inverter configuration, which can provide power to multiple-loads with independent control, high efficiency, reduced components count and fixed frequency control of each load.

This paper is organised as follows. In Section 2, principle and modes of operation of the proposed configuration are presented. Section 3 describes simulation and experimental results. Section 4 presents characteristics showing independent control of loads. Section 5 presents an extension of the proposed configuration to more than two loads. Section 6 concludes the paper.

2 Proposed inverter configuration and control technique

2.1 Operating principle

Induction cooking system consists of a vessel and a heating coil. The coil and vessel are like primary and secondary of a transformer. Based on this, induction cooking load referred to the coil is modelled as a series R_{eq}–L_r circuit for constant switching frequency operation [14, 21–25]. R_{eq} is the referred equivalent resistance and L_r is the referred equivalent inductance to the coil, respectively. The concept of series resonance is used with each load. Resonant capacitor is connected in series with R_{eq}–L_r model to form the series load-resonant circuit.

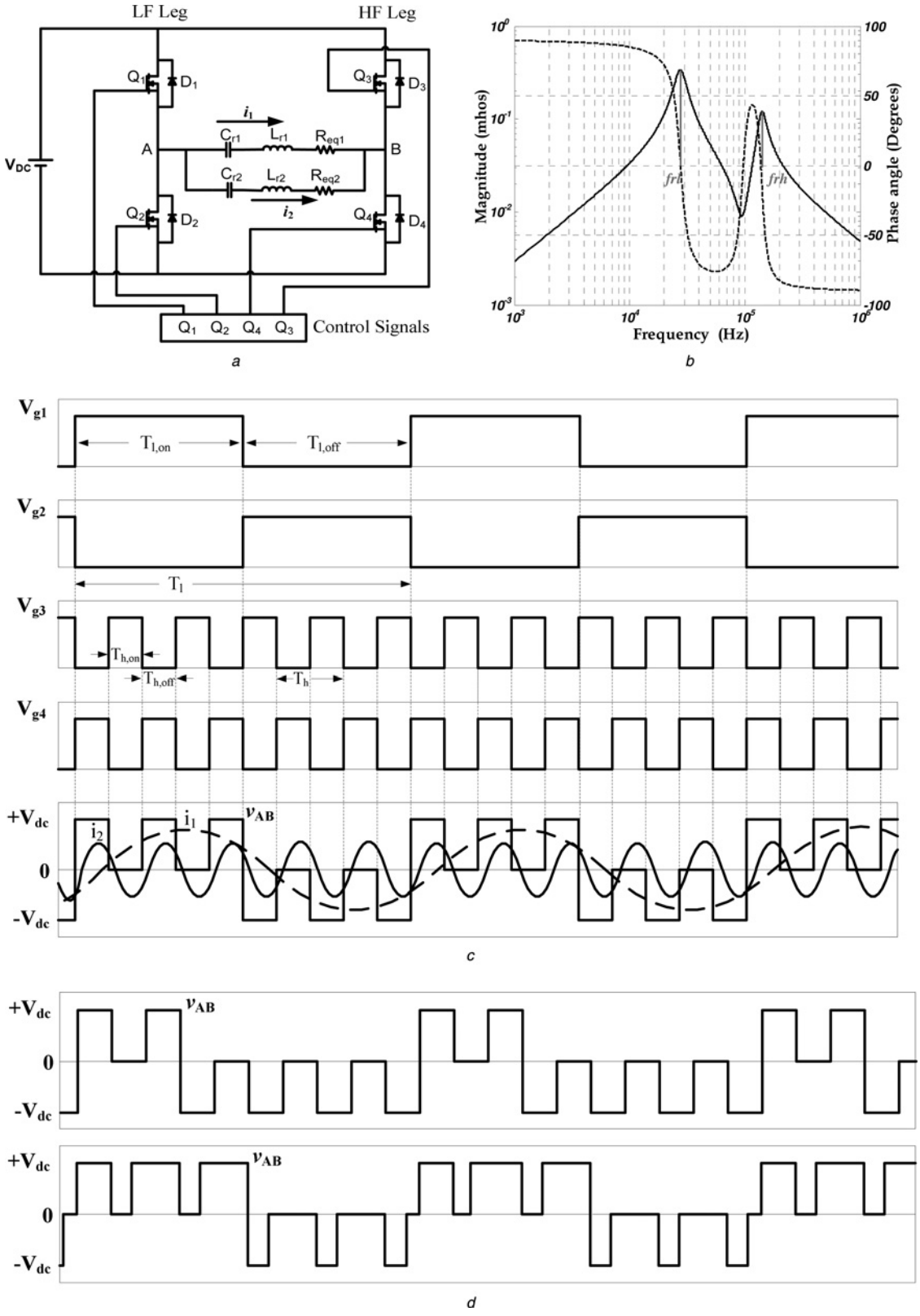


Fig. 1 *Proposed inverter configuration, admittance characteristic and waveforms*

a Proposed dual frequency inverter configuration
b Admittance characteristic
c Inverter output voltage and both load currents with gate pulses at $D_l = 1$ and $D_h = 1$
d Inverter output voltages at $D_l = 0.6$ and $D_h = 1$ and $D_l = 1$ and $D_h = 0.6$

The circuit diagram of proposed dual frequency full-bridge resonant inverter configuration is shown in Fig. 1*a*. This figure shows two load resonant circuits connected in parallel to output terminals of the inverter. One leg of the inverter is switched at low-frequency (LF) and the other leg is switched at HF. They are marked as LF leg and HF leg, respectively. ADC control technique is used with each leg. Load-1 consists of C_{r1}, L_{r1} and R_{eq1}, which are resonant capacitor, inductance of load-1 and

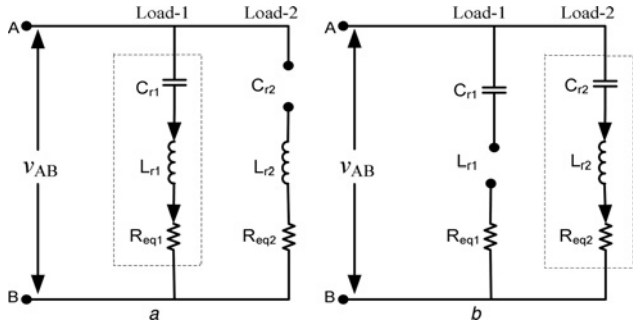


Fig. 2 *Equivalent circuits for load-1 and load-2*

a Load equivalent circuit for LF component of v_{AB}
b Load equivalent circuit for HF component of v_{AB}

equivalent load resistance, respectively. Similarly for load-2, C_{r2}, L_{r2} and R_{eq2} are resonant capacitor, inductance of load-2 and equivalent load resistance, respectively.

Admittance characteristic of the two-load circuit is shown in Fig. 1*b*. At resonant frequency of LF load $f_{rl} = \left(1/2\pi\sqrt{L_{r1}C_{r1}}\right)$ and resonant frequency of HF load $f_{rh} = \left(1/2\pi\sqrt{L_{r2}C_{r2}}\right)$, magnitudes of respective tank admittances reach peak and corresponding phase angles are zero. In this figure, magnitude plot indicates that the LF load circuit offers low admittance to the HF current component. The HF load circuit offers low admittance to the LF current component. Similarly, the phase angle plot indicates that respective series resonant tank phase angles are negative above their respective resonant frequencies.

Inverter output voltage (v_{AB}) and both load currents are shown in Fig. 1*c*. v_{AB} is a combination of two voltage waveforms v_{LF} and v_{HF} with LF and HF, respectively. These two voltages are independently controlled with ADC techniques for LF and HF legs. Duty-ratios for LF and HF legs are defined as $D_l = T_{l,on}/(T_l/2)$ and $D_h = T_{h,on}/(T_h/2)$, respectively. Variation of D_l and D_h independently controls LF and HF components of output voltage. Thus respective load current magnitudes are also controlled. This gives power control in each load. Although both loads are connected in parallel and supplied from the same output terminals, negligible amounts of LF current

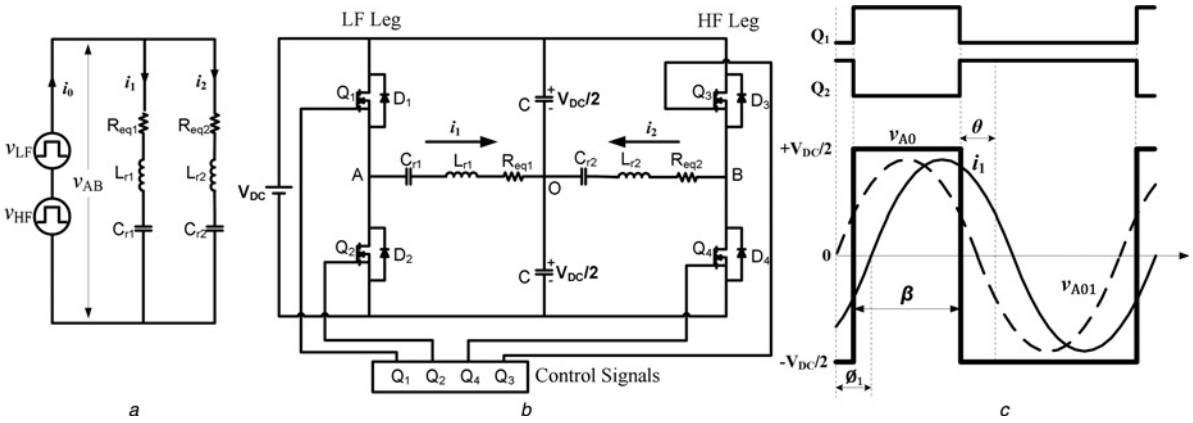


Fig. 3 *Equivalent circuit of the dual frequency inverter*

a Equivalent circuit of dual frequency inverter
b Dual frequency inverter as two half-bridge inverters
c Waveforms under ADC control

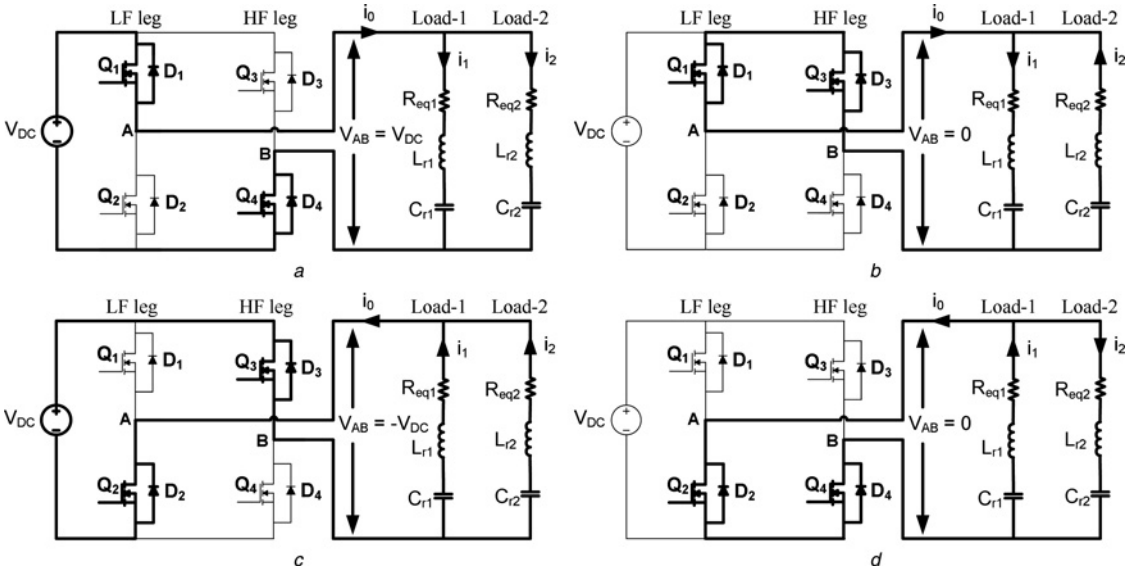


Fig. 4 *Equivalent circuits for modes of dual frequency resonant inverter*

a Mode 1: Q_1 and Q_4 are ON
b Mode 2: Q_1 and Q_3 are ON
c Mode 3: Q_2 and Q_3 are ON
d Mode 4: Q_2 and Q_4 are ON

flows in an HF load and vice-versa. Fig. 1*d* shows waveforms of v_{AB} under two different duty-ratio combinations of LF and HF legs.

2.2 Selection of switching frequencies

For zero voltage switching operation, f_l and f_h are taken 5–10% higher than f_{rl} and f_{rh}. Selection criteria for f_l and f_h should be to isolate the operations of load-1 and load-2 from one another. Although load-1 and load-2 are in parallel across v_{AB}, LF component of v_{AB} should power only load-1 and HF component of v_{AB} should power only load-2. f_l and f_h should be selected such that impedance offered by a LF load circuit should be as large as possible to an HF and vice-versa. This ensures individual load currents to be dependent only on the corresponding LF or HF components of v_{AB}. For this, f_h should be as high as possible in comparison to f_l. The range of switching frequencies normally used with induction cooking is 20–150 kHz. In the prototype of dual frequency inverter, f_h/f_l is taken as five. For f_l of 30 kHz, f_h is taken as 150 kHz. In the prototype, both the induction heating coils are identical with equal inductances ($L_{r1} = L_{r2}$). For the selected values of f_l and f_h, C_{r2} is much smaller than C_{r1}.

Figs. 2*a* and *b* represent equivalent load circuits for LF and HF components of v_{AB}. In Fig. 2*a*, C_{r2} behaves as an open circuit because of its large reactance at LF. Similarly, C_{r1} has negligible

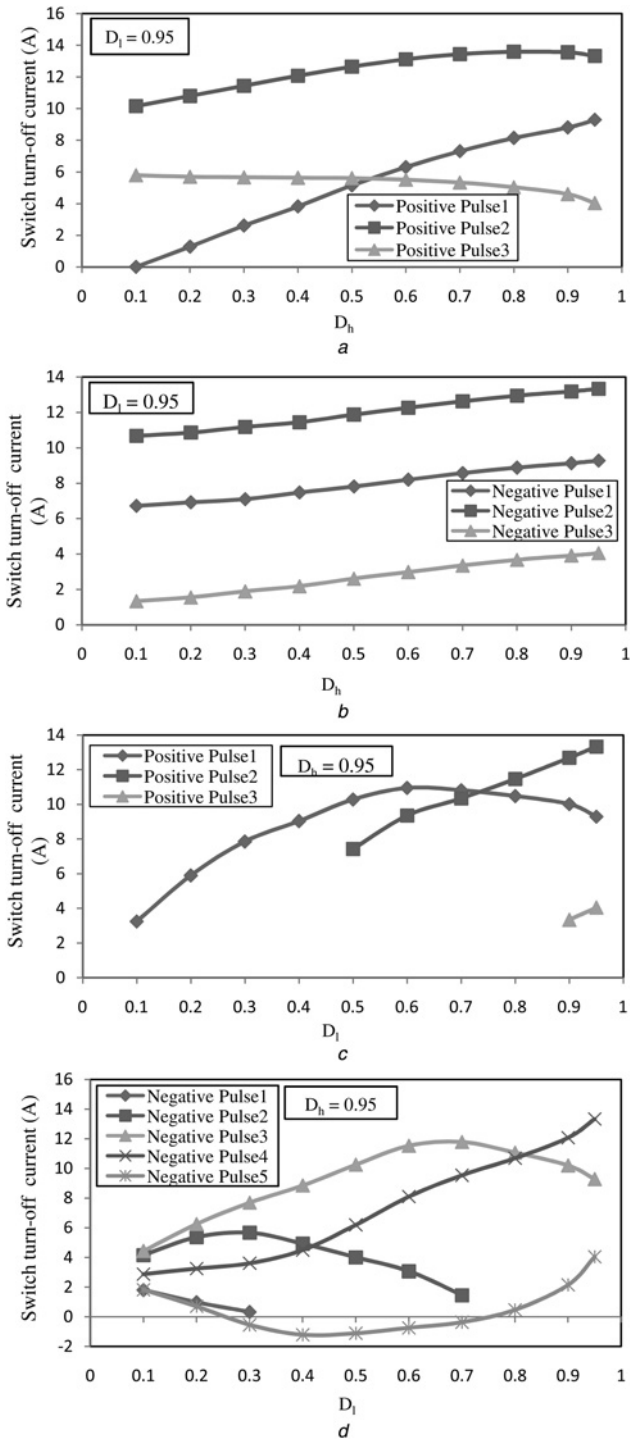


Fig. 5 *Switch turn-off currents against duty-ratio*

a Switch turn-off currents for HF leg against D_h (positive half-cycle)
b Switch turn-off currents for HF leg against D_h (negative half-cycle)
c Switch turn-off currents for HF leg against D_l (positive half-cycle)
d Switch turn-off currents for HF leg against D_l (negative half-cycle)

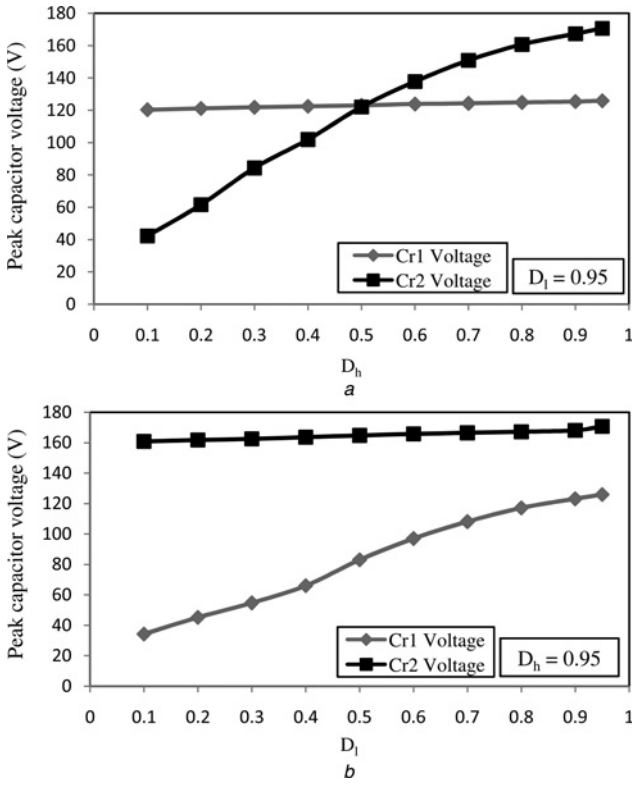


Fig. 6 *Resonant capacitor voltage against duty-ratio*

a Peak capacitor voltage against D_h
b Peak capacitor voltage against D_l

Table 1 Parameters of dual frequency full bridge resonant inverter

Item	Symbol	Value
source voltage	V_{DC}	35 V
equivalent resistance of load-1	R_{eq1}	1.95 Ω
equivalent inductance of load-1	L_{r1}	68 μH
parasitic series resistance of IH load-1 coil		0.14 Ω
resonant capacitor of load-1 (MKV type) (EPCOS B25834-F6104-M001) [(3 × 0.1 μF) + (0.15 μF) = 0.45 μF]	C_{r1}	0.45 μF
ESR for 0.15 μF capacitor		24 mΩ
ESR for 0.1 μF capacitor		33 mΩ
low resonant frequency	f_{rl}	28.77 kHz
low switching frequency	f_l	30 kHz
equivalent resistance of load-2	R_{eq2}	2.6 Ω
equivalent inductance of load-2	L_{r2}	68 μH
parasitic series resistance of IH load-2 coil		0.14 Ω
resonant capacitor of load-2 (MKV type) (EPCOS B25834-F6104-M001) [five 0.1 μF are in series]	C_{r2}	0.02 μF
ESR for 0.1 μF capacitor		33 mΩ
high resonant frequency	f_{rh}	136.47 kHz
high switching frequency	f_h	150 kHz
MOSFETs used	IRFP4110	100 V, 180 A
$R_{DS(on)}$		3.7 mΩ
control ICs	UC3875	
driver IC	IR2110	

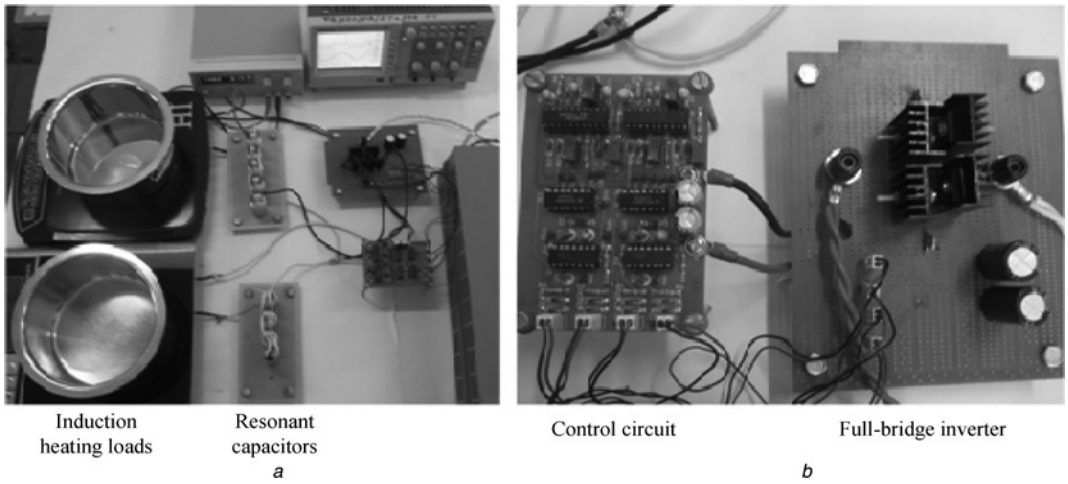


Fig. 7 *Experimental setup for dual frequency full-bridge resonant inverter configuration*

a Experimental setup
b Full-bridge inverter with control circuit

reactance at HF. Impedance of load-1 at HF is mainly dominated by reactance of L_{r1}, which behaves as an open circuit as shown in Fig. 2*b*. This results in LF and HF currents mainly flowing in load-1 and load-2, respectively. The impedance for the LF current path is

$$Z_{eq1} = R_{eq1} + j\left(2\pi f_l L_{r1} - \frac{1}{2\pi f_l C_{r1}}\right) \tag{2}$$

The impedance for the HF current path is

$$Z_{eq2} = R_{eq2} + j\left(2\pi f_h L_{r2} - \frac{1}{2\pi f_h C_{r2}}\right) \tag{3}$$

2.3 Expression for output power

Dual frequency inverter output voltage v_{AB} is the combination of v_{LF} and v_{HF} as shown in Fig. 3*a*. v_{AB} switches between $\pm V_{DC}$ whereas v_{LF} and v_{HF} can be considered to switch between $\pm V_{DC}/2$ with LF and HF, respectively. v_{LF} powers LF load and v_{HF} powers HF load only. This shows that dual frequency inverter can be represented as the combination of two half-bridge inverters as shown in Fig. 3*b*. Each half-bridge inverter operates at LF and HF. Here, v_{LF} and v_{HF} are v_{AO} and v_{BO}, respectively. Waveforms related to the half-bridge comprising of Q_1, Q_2, and so on, with ADC control are shown in Fig. 3*c*. In Fig. 3*b*, as each half-bridge can be independently controlled, the proposed dual frequency inverter can also provide independent control of each load. Elimination of two bulky capacitors (C) of Fig. 3*b* is the advantage of dual frequency inverter. It also fulfils the requirement of independent control of both loads.

Output power of proposed inverter configuration is the heat dissipated in R_{eq1} and R_{eq2} of the two series resonant loads. Output power of load-1 and load-2 can be computed as $I_1^2 R_{eq1}$ and $I_2^2 R_{eq2}$, respectively.

I_1 and I_2 are the rms values of the LF and HF currents in the two loads, respectively. Since, the LF and HF currents are close to sine waves, it can be assumed that other harmonics are negligibly small and $I_1 \cong I_{11}$ and $I_2 \cong I_{21}$. I_{11} and I_{21} are fundamental components of I_1 and I_2.

Total output power of the proposed inverter is equal to the output powers of individual half-bridge inverters. Output power expressions for ADC controlled inverter feeding series resonant load is presented in [11]. The output power for a half-bridge inverter is expressed as

$$P_o = \frac{2V_{DC}^2 \cos^2 \emptyset_1}{\pi^2 R_{eq}} \cos^2 \frac{\theta}{2} \tag{4}$$

The phase lag $\emptyset_1$ between the voltage v_{A01} and the load current i_0 can be obtained as

$$\emptyset_1 = \tan^{-1}\left[\frac{\omega_s L_r - (1/\omega_s C_r)}{R_{eq}}\right] = \tan^{-1}\left[Q\left(\omega_n - \frac{1}{\omega_n}\right)\right] \tag{5}$$

Parameters mentioned in the above expression are shown in Fig. 3*c* and θ is the control angle to vary duty-ratio. In (4) for constant switching frequency, all parameters are constant except θ. By varying θ, duty-ratio of the output voltage waveform can be controlled which in turn controls output power. P_o is proportional to $\cos^2(\theta/2)$. For dual frequency inverter, P_{o1} and P_{o2} are output powers of load-1 and load-2, respectively

$$\begin{aligned}\text{Total output power} &= P_{o1} + P_{o2} = I_1^2 R_{eq1} + I_2^2 R_{eq2} \\ &= \left[\frac{2V_{DC}^2 \cos^2 \emptyset_{1l}}{\pi^2 R_{eq1}} \cos^2 \frac{\theta_l}{2}\right] + \left[\frac{2V_{DC}^2 \cos^2 \emptyset_{1h}}{\pi^2 R_{eq2}} \cos^2 \frac{\theta_h}{2}\right]\end{aligned} \tag{6}$$

$\emptyset_{11}$ is the phase-lag between the fundamental component of $v_{LF}(=v_{AO})$ and load current i_1 and $\emptyset_{1\,h}$ is the phase-lag between the fundamental component of $v_{HF}(=v_{BO})$ and load current i_2, respectively. θ_l and θ_h are control angles for LF and HF loads, respectively.

2.4 Analysis of the proposed inverter

The inverter output voltage V_{AB} can have three voltage levels as $+V_{dc}$, 0, $-V_{dc}$. Equivalent circuit of the inverter for different modes of operation are shown in Fig. 4. In the proposed configuration, LF leg switching frequency is 30 kHz and HF leg switching frequency is 150 kHz. The switching frequencies are above its respective resonant frequencies for ZVS operation.

Mode-1 operation: During this period, the switching devices Q_1 and Q_4 are turned-on. Inverter output voltage will be equals to $+V_{DC}$.

During mode-1, the loop equation for load-1 circuit can be written as

$$L_{r1}\frac{di_1(t)}{dt} + \frac{1}{C_{r1}}\int i_1(t)dt + v_{C_{r1}}(t=0) + R_{eq1} i_1(t) = v_{AB} \tag{7}$$

with initial values of $i_1 = I_{10}$ and $v_{C_{r1}} = V_{C_{r10}}$. The solution of this

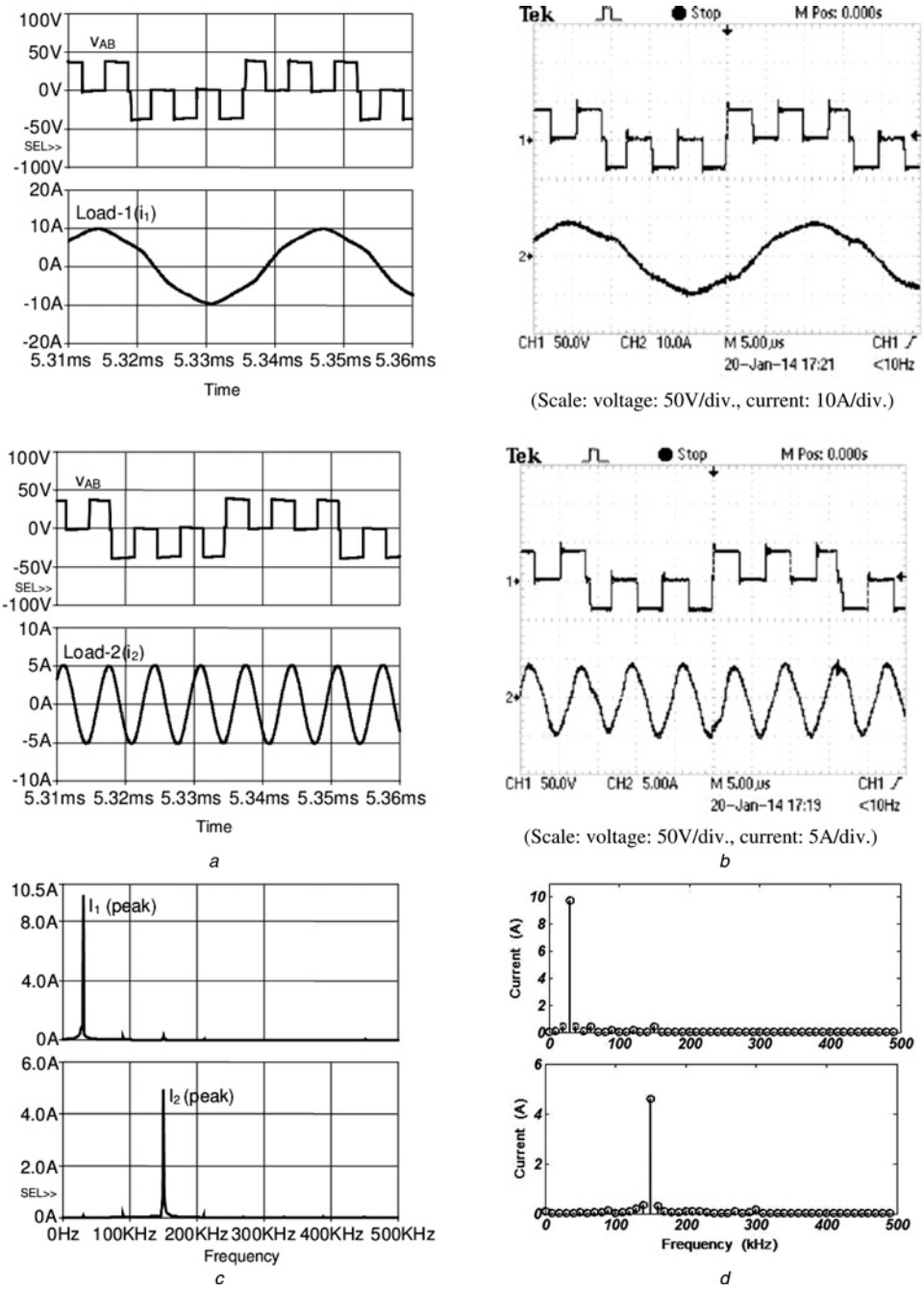


Fig. 8 *v_{AB} with LF and HF load currents and their FFTs for $D_l = 0.95$ and $D_h = 0.95$*

a v_{AB} with LF and HF load currents under simulation
b v_{AB} with LF and HF load currents under experiment
c FFT for LF and HF load currents under simulation
d FFT for LF and HF load currents under experiment

equation is

$$i_1(t) = \left[\frac{v_{AB} - V_{C_{r10}}}{\omega_n L_{r1}}\right] e^{-\alpha t} \sin \omega_n t + \left[I_{10} e^{-\alpha t}\left(\cos \omega_n t - \frac{\alpha}{\omega_n} \sin \omega_n t\right)\right] \tag{8}$$

and

$$v_{C_{r1}}(t) = V_{C_{r10}} + (v_{AB} - V_{C_{r10}})\left[1 - e^{-\alpha t}\left(\cos \omega_n t + \frac{\alpha}{\omega_n} \sin \omega_n t\right)\right] + \frac{I_{10}}{\omega_n C_{r1}} e^{-\alpha t}(\sin \omega_n t) \tag{9}$$

where $\alpha = R_{eq1}/2L_{r1}$ and $\omega_n = \sqrt{(1/L_{r1}C_{r1})}$.

During this mode, the loop equation for load-2 circuit can be written as

$$L_{r2} \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} + \frac{1}{C_{r2}} \int i_2(t)\mathrm{d}t + v_{C_{r2}}(t = 0) + R_{eq2} i_2(t) = v_{AB} \tag{10}$$

with initial values of $i_2 = I_{20}$ and $v_{C_{r2}} = V_{C_{r20}}$. The solution of this equation is

$$i_2(t) = \left[\frac{v_{AB} - V_{C_{r20}}}{\omega_n L_{r2}}\right] e^{-\alpha t} \sin \omega_n t + \left[I_{20} e^{-\alpha t}\left(\cos \omega_n t - \frac{\alpha}{\omega_n} \sin \omega_n t\right)\right] \tag{11}$$

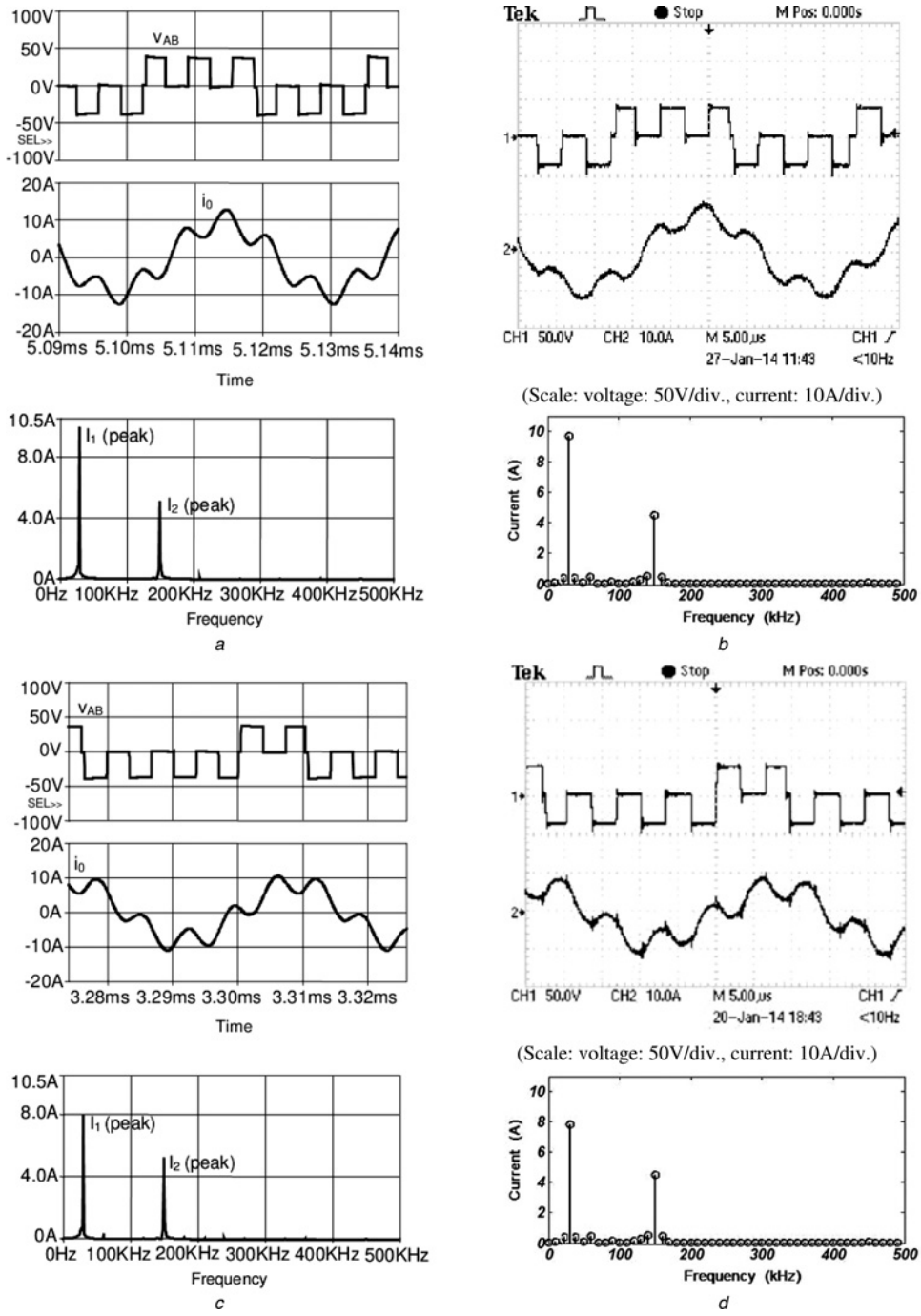


Fig. 9 *Inverter output voltage, total load current and FFT for total load current*

a v_{AB} and i_0 and FFT for i_0 under simulation at $D_l = 0.95$ and $D_h = 0.95$
b v_{AB} and i_0 and FFT for i_0 under experiment at $D_l = 0.95$ and $D_h = 0.95$
c v_{AB} and i_0 and FFT for i_0 under simulation at $D_l = 0.6$ and $D_h = 0.95$
d v_{AB} and i_0 and FFT for i_0 under experiment at $D_l = 0.6$ and $D_h = 0.95$
e v_{AB} and i_0 and FFT for i_0 under simulation at $D_l = 0.95$ and $D_h = 0.6$
f v_{AB} and i_0 and FFT for i_0 under experiment at $D_l = 0.95$ and $D_h = 0.6$

and

$$v_{C_{r2}}(t) = V_{C_{r20}} + (v_{AB} - V_{C_{r20}})\left[1 - e^{-\alpha t}\left(\cos\omega_n t + \frac{\alpha}{\omega_n}\sin\omega_n t\right)\right] + \frac{I_{20}}{\omega_n C_{r2}} e^{-\alpha t}(\sin\omega_n t) \tag{12}$$

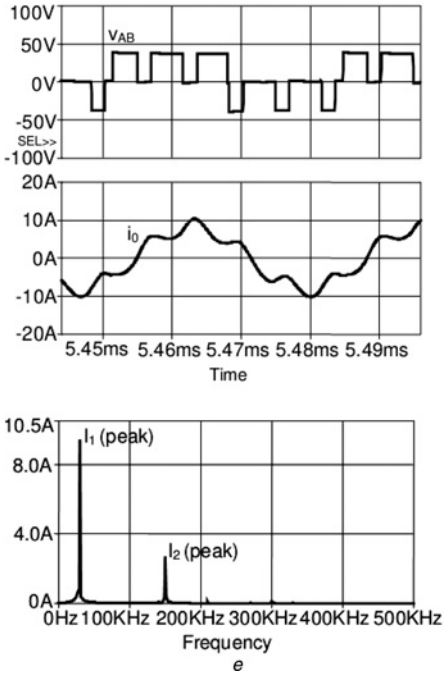
where $\alpha = R_{eq2}/2L_{r2}$ and $\omega_n = \sqrt{1/L_{r2}C_{r2}}$.

Hence, the instantaneous value of inverter total output current can be expressed as

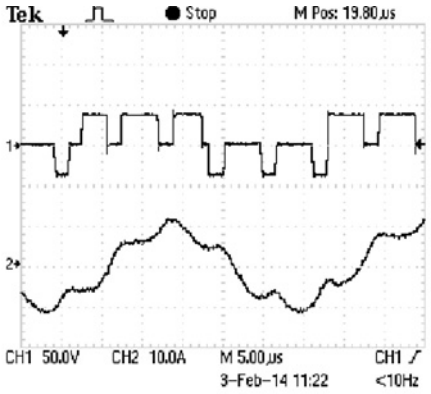
$$i_0(t) = \left(i_1(t) + i_2(t)\right) \tag{13}$$

Thus during each mode of operation, by substituting the corresponding value of V_{AB} and initial conditions, equations for load-1 and load-2 resonant currents and respective resonant capacitor voltages can be obtained by using the above equations.

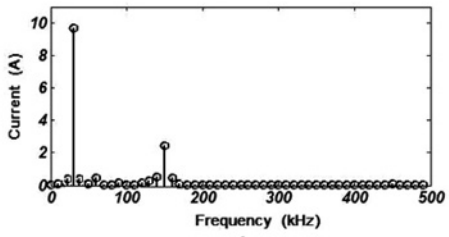
Mode-2 operation: During this period, the switching devices Q_1 and Q_3 are turned-on. Inverter output voltage will be equals to '0'.



e



(Scale: voltage: 50V/div., current: 10A/div.)



f

Fig. 9 *Continued*

Mode-3 operation: During this period, the switching devices Q_2 and Q_3 are turned-on. Inverter output voltage will be equals to $-V_{dc}$.

Mode-4 operation: During this period, the switching devices Q_2 and Q_4 are turned-on. Inverter output voltage will be equals to '0'.

In this configuration, one leg is switched at 30 kHz (LF) and other leg is switched at 150 kHz (HF). ZVS operation is required for high efficiency. Out of the two legs, HF leg is important from ZVS point of view. For ZVS, the switch turn-off currents should be positive when the switch is turning-off. This also ensures ZVS for the other switch in the same leg which is turning-on.

From the equations described above, switch turn-off currents are calculated in the powering mode of positive and negative half-cycles. In the free-wheeling mode, ZVS is not possible. These are shown in Fig. 5. Based on the duty-ratio of LF and HF legs, there can be equal or unequal number of HF pulses in positive and negative half-cycles of the output voltage waveform. As D_l increases from low to high value, number of voltage pulses in the positive half-cycle increased and number of voltage pulses in the negative half-cycle decreased. Hence for different duty-ratios of HF and LF legs, switch turn-off currents are plotted for every pulse during positive and negative half-cycles of the output voltage waveform. In positive half-cycle, positive total load current ensures ZVS for both switches of HF leg and in negative half-cycle, negative total load current ensures ZVS.

Figs. 5*a* and *b* show switch turn-off currents of HF leg for positive and negative half-cycles of output voltage, respectively. In this, $D_l = 0.95$ and D_h varies. Figs. 5*c* and *d* show switch turn-off currents of HF leg for positive and negative half-cycles of output voltage, respectively. In this, $D_h = 0.95$ and D_l varies. Pulses of both positive and negative half-cycles are numbered as pulse 1, 2 and 3 from left to right in the output voltage waveform.

In Figs. 5*a* and *b*, switch turn-off currents for all pulses are positive ensuring ZVS for HF leg. In both these figures, the middle pulse has a larger switch turn-off current because of the symmetric location of total load current waveform with the output voltage waveform. In Figs. 5*c*, as D_l varies from low to high value, the number of pulses is increased from one to three in the positive half-cycle. Switch turn-off currents for all the pulses are positive. In Fig. 5*d*, for low values of D_l, there are five pulses in the negative half-cycle. As D_l increases, the number of pulses decreased to three. Here pulse 5 has negative switch turn-off current for certain range of D_l where ZVS is not ensured.

Peak capacitor voltages are obtained from the above analytical equations and plotted in Figs. 6*a* and *b*. Fig. 6*a* shows these voltages when $D_l = 0.95$ and D_h varies. Fig. 6*b* shows these voltages when $D_h = 0.95$ and D_l varies. This information is useful in selecting resonant capacitor voltage ratings. As Q of the load circuits is high, resonant capacitor voltages of both loads are high. These voltages vary with duty-ratio.

3 Results of proposed dual frequency inverter

3.1 Simulation and experimental results

The proposed inverter configuration for individual output power control with ADC control technique is simulated and experimentally verified using the parameters shown in Table 1. Equivalent resistance and inductance of load-1 and load-2 are taken as the combination of induction heating coil and vessel. An induction heating coil is made with Litz wire.

A dual frequency full-bridge series resonant inverter is designed with the parameters shown in Table 1. Open circuit behaviour of load-1 for HF and load-2 for LF are presented in Section 2.2. This property of load circuits responding to the relevant switching frequency and rejecting other frequency is based on the selection of resonant components and switching frequencies. This helps in isolating the operation of load-1 from load-2 and vice-versa. Proposed dual frequency full-bridge resonant inverter configuration of experimental set-up is shown in Fig. 7. Fig. 7*a* shows the induction heating loads and resonant series capacitors with a single full-bridge inverter circuit. Fig. 7*b* shows the single full-bridge inverter circuit with pulse generator and driver circuit. In control circuit two UC3875 ICs are used for four control pulses.

Table 2 Load currents and output powers for different combinations of D_l and D_h

S. No.	D_l	D_h	I_1 (rms), A	I_2 (rms), A	P_{o1}, W	P_{o2}, W
1	0.95	0.95	6.79	2.99	90	23.24
2	0.6	0.95	5.4	2.99	56.8	23.24
3	0.95	0.6	6.79	2.25	90	13.21

AND/OR logic gates are used for implementation of ADC technique and IR2110 ICs are used as drivers.

The simulation and experimental results are shown in Fig. 8 for $D_l = 0.95$ and $D_h = 0.95$. Fig. 8*a* shows v_{AB}, i_1 and i_2 waveforms under simulation. Fig. 8*b* shows these waveforms under experimental conditions. Fig. 8*c* shows FFT of i_1 and i_2 under simulation. Fig. 8*d* shows them for experimental condition. It has $I_1(\text{rms}) = 6.79$ A and $I_2(\text{rms}) = 2.99$ A.

Fig. 9 shows the simulation and experimental results for different combinations of D_l and D_h. Fig. 9*a* shows v_{AB} and i_0 ($= i_1 + i_2$) with its FFT under simulation for $D_l = 0.95$ and $D_h = 0.95$. Fig. 9*b* shows these waveforms under experimental conditions. Figs. 9*c* and *d* are for $D_l = 0.6$ and $D_h = 0.95$. Similarly, Figs. 9*e* and *f* are for $D_l = 0.95$ and $D_h = 0.6$. The above results are tabulated in Table 2.

From simulation and experimental results, it is observed that both results are in good agreement with each other. FFTs of individual load currents show that they have mainly fundamental component of currents and other harmonics are negligible. Also, individual load currents and powers are independently controllable. LF and HF output powers are dependent on corresponding load currents. These are controlled by varying duty-ratios of their respective legs.

3.2 Comparison with other control techniques

Commonly used control techniques for induction heating are PDM control, square wave control, AVC and ADC control techniques. Every technique has its own merits and demerits, range of output power with high efficiency and ZVS range. PDM control has several control variables like, switching frequency, duty-ratio, time period of PDM and on-time of PDM. Generally, switching frequency is kept constant and on-time is varied. For constant switching frequency operation, PDM provides linear output variation with on-time and also offers ZVS over a wide range. It has certain limitations like lower utilisation, flicker emission and so on. Square wave control uses variable frequency control which offers high efficiency in medium and high power ranges but efficiency decreases for low output power. It is because of the higher switching frequency and increased switching losses. Similarly, AVC and ADC are suitable for medium and high power range with high efficiency. At a reduced output efficiency decreases because of the limitation on ZVS range. In addition ADC has asymmetrical device losses. It has a lower ZVS range than AVC. In addition, hybrid control techniques are also reported where more than one of the above control techniques are combined for improved performance. However, these are more involved.

In this paper, an ADC control technique is used with each leg of the inverter. ZVS is not a serious problem with LF leg as switching frequency is small. HF leg switches several times in one cycle of LF. ZVS is not guaranteed for every switching specially under low duty-ratios as shown in Section 2.4. This may result in reduction in efficiency under light load condition as can be observed in efficiency characteristics in Section 4, Fig. 11. Proposed dual frequency inverter offers good performance for medium and high power range. The proposed method is better in certain aspects in comparison with other multiple load configurations explained in introduction. The number of devices/loads is least in dual frequency inverter. Since a dual frequency inverter is a combination of two half-bridge inverters, split capacitors of half-bridge configuration are avoided. Overall efficiency is comparable in medium and high power range with other configurations proposed in the literature. The constant switching frequency operation is an advantage. The proposed method is simple to implement and cost effective. The added advantage of dual frequency inverter is that the LF heating coil can be used for vessels with magnetic material and HF heating coil can be used for vessels with non-magnetic materials. This avoids use of electro-mechanical switches as presented in the literature for all metal applications.

4 Control of load power

Load power control is achieved using ADC control technique. LF and HF load powers are dependent on corresponding load currents. The simulation and experimental results of LF and HF load currents and output power variation are shown in Figs. 10 and 11, for different duty-ratio combinations of LF and HF legs.

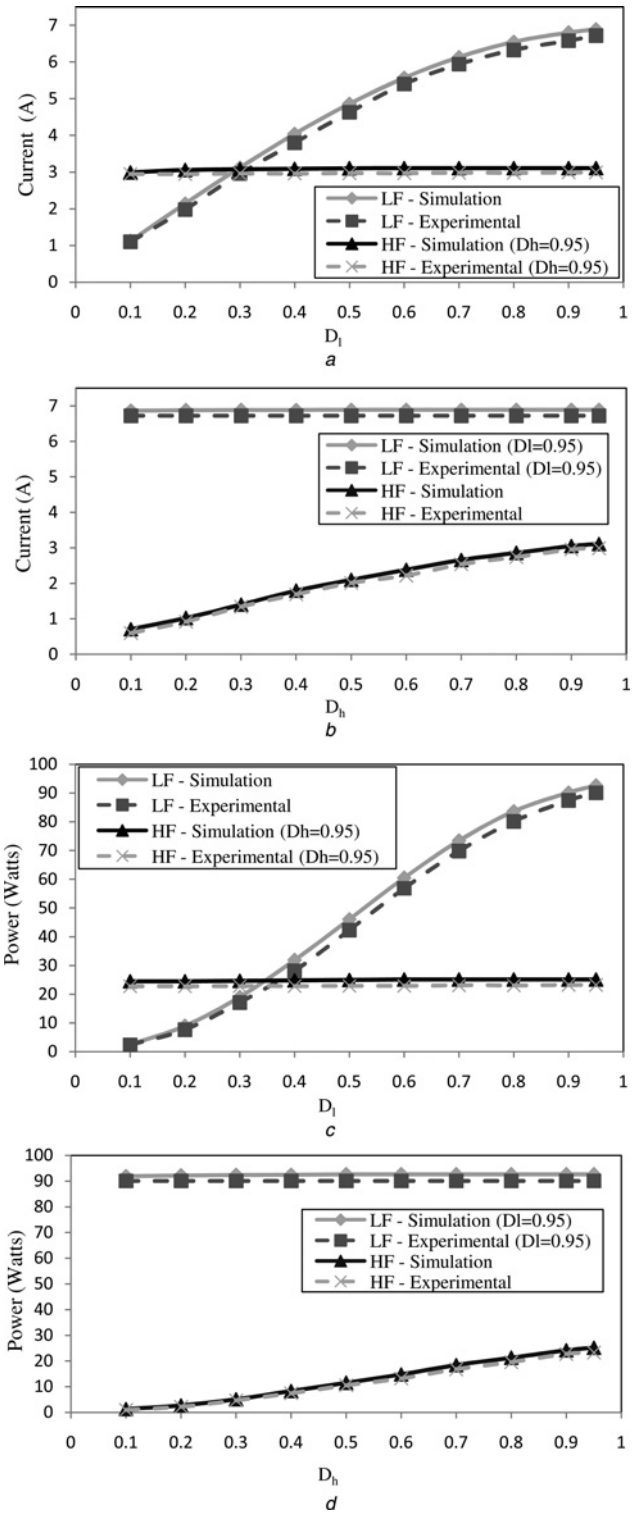


Fig. 10 *LF and HF load currents and output powers against duty-ratio*

a LF current against D_l with $D_h = 0.95$
b HF current against D_h with $D_l = 0.95$
c Load-1 power against D_l with $D_h = 0.95$
d Load-2 power against D_h with $D_l = 0.95$

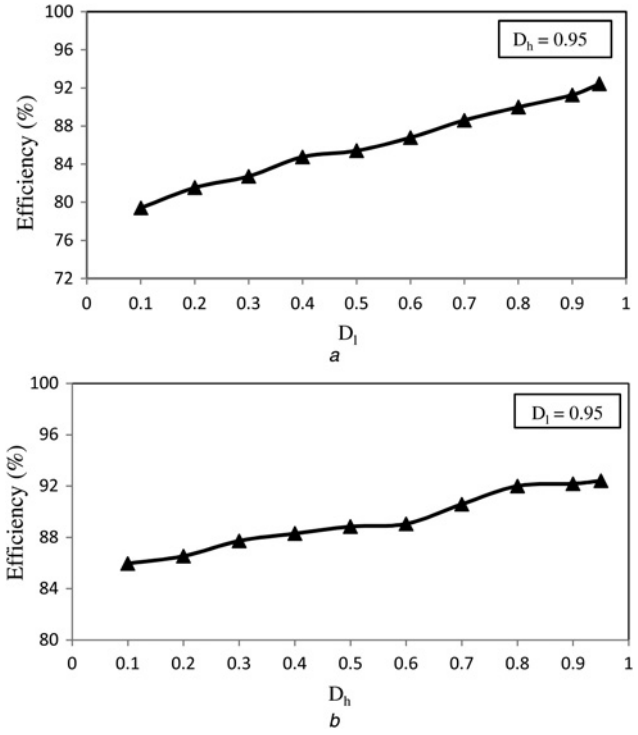


Fig. 11 *Overall efficiencies against duty-ratio*

a Overall efficiency against D_l with $D_h = 0.95$
b Overall efficiency against D_h with $D_l = 0.95$

Variation of LF load current with a variation of D_l from 0.1 to 0.95 is shown in Fig. 10*a*. For this, D_h is kept constant at 0.95. Under this condition, only LF current varies from 1.1 to 6.72 A whereas HF current remains constant at 2.99 A. Similarly, variation of HF load current with a variation of D_h from 0.1 to 0.95 is shown in Fig. 10*b*. For this, D_l is kept constant at 0.95. Under this condition, only HF current varies from 0.6 to 2.99 A whereas LF current remains constant at 6.79 A. This shows that for a given value of D_l and varying D_h, HF current and power varies and vice-versa. This indicates independent control of each load current and power.

Each inverter output is computed as I^2R. 'I' is the r.m.s value of respective LF or HF inverter current. 'R' is the equivalent load resistance of LF or HF load, that is, 1.95 Ω for LF load and 2.6 Ω for HF load. Similarly, output power of LF load varies with the variation of D_l. This is shown in Fig. 10*c*. Output power of HF load varies with the variation of D_h. This is shown in Fig. 10*d*. The simulation and experimental results are in good agreement with each other.

In Fig. 11*a*, LF load power is controlled while HF load power is kept constant at its maximum. In Fig. 11*b*, HF load power is controlled while LF load power is kept constant at its maximum. Under both conditions, overall efficiency is high. Total output power is measured by the addition of individual inverter outputs. Input power is obtained by multiplication of DC input voltage and average input current of the inverter.

In general, efficiency close to 90% and above is desirable. Efficiency characteristics show that when D_l is varying, fall in overall efficiency is more drastic than for D_h variation. It is because of the larger rated LF output power than HF output power and higher switching losses in HF leg. If both rated output powers are equal, an efficiency of about 90% and above can be achieved

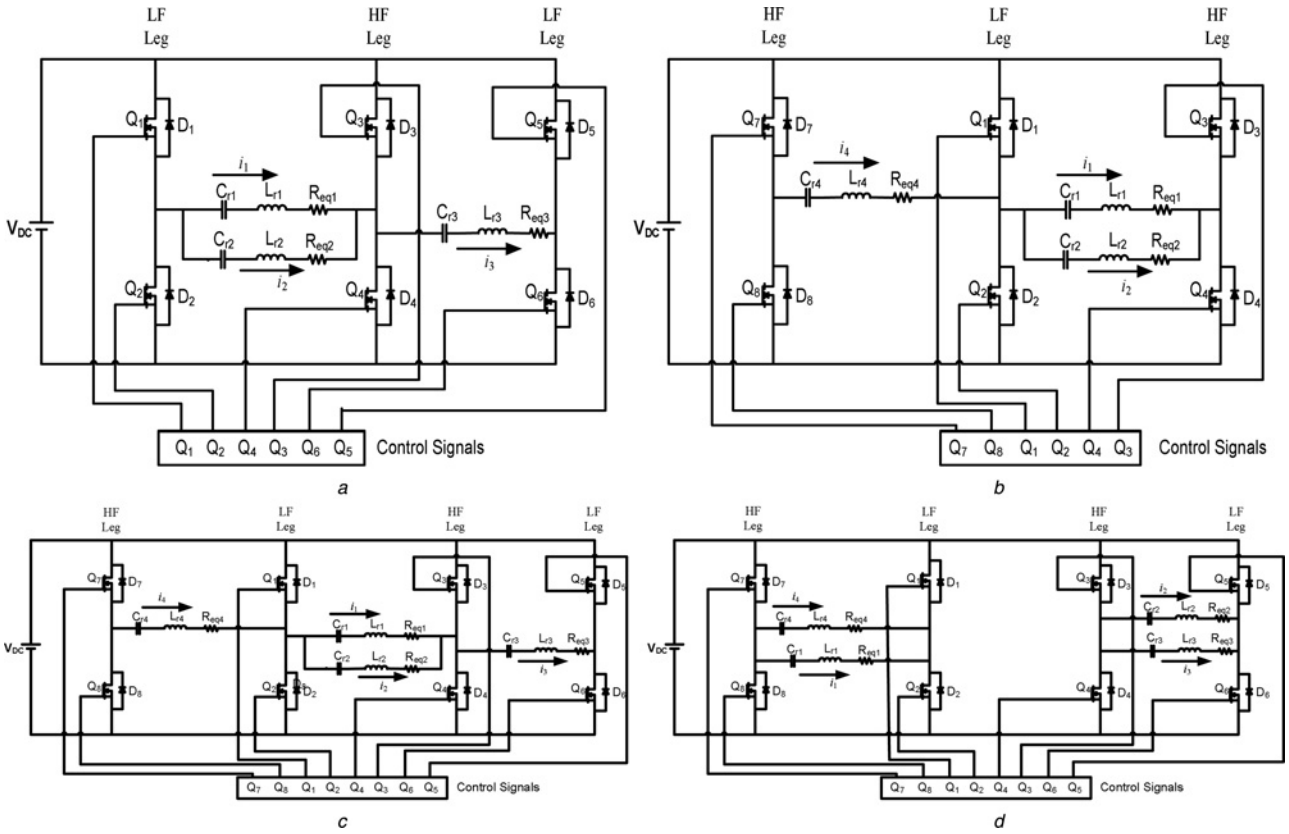


Fig. 12 *Extension of dual frequency series resonant inverter to multiple loads*

a Extension to 3-load configuration with two LF legs
b Extension to 3-load configuration with two HF legs
c Extension to 4-load configuration
d Extension to 4-load configuration with two dual frequency inverters

IET Power Electron., 2015, Vol. 8, Iss. 4, pp. 591–601

for duty-ratios as low as 0.5. A duty-ratio of 0.5 corresponds to 50% of rated power. It may be concluded that proposed configuration can be used for medium and high power applications effectively.

5 Extension of proposed configuration to multiple loads

The proposed configuration requires two switching devices/load or one leg/load. It is achieved without split-capacitor power supply. This configuration is extended for multiple loads as follows. Extension of proposed configuration to multiple loads is shown in Fig. 12.

In Fig. 12*a*, proposed configuration is extended for three loads by adding an additional leg to the right of existing HF leg. This is to be of LF. This LF is same as the existing LF leg. By controlling this leg with ADC control technique, load connected between HF leg and this additional LF leg can be independently controlled. Here also, the number of legs/load is one. For three loads, it is also possible to add one additional leg to the left of existing LF leg. However, it has to be of HF. It is shown in Fig. 12*b*. Again, independent control of this third load is possible with ADC control technique. Hence this method can be extended to four loads also as shown in Fig. 12*c*. An alternate converter configuration of Fig. 10*c* is shown in Fig. 12*d*. In all these configurations, number of legs/load is one.

6 Conclusions

In this paper, dual frequency full-bridge inverter configuration for two load induction cooking application has been proposed. Both loads are independently controlled. It can be extended for more than two loads also. Number of switching devices per load is two (i.e. one leg per load). Two switching frequencies are used for powering the loads. Each load is operated at different switching frequency, that is, 30 and 150 kHz. It is possible to operate more than two loads with two switching frequencies only. Asymmetric duty cycle control technique is used for power control of individual loads. FFT analysis of individual load current shows that harmonic currents in a particular load are negligible. The design and control of the proposed topology are simple. The added advantage of dual frequency inverter is that the LF heating coil can be used for vessels with magnetic material and HF heating coil can be used for vessels with non-magnetic materials. This avoids use of electro-mechanical switches for all metal applications. Simulation and experimental results of the proposed configuration are in good agreement.

7 References

1 Ahmed, N.A., Nakaoka, M.: 'Boost-half-bridge edge resonant soft switching PWM high-frequency inverter for consumer induction heating appliances', *IEE Electr. Power Appl.*, 2006, **153**, (6), pp. 932–938
2 Miyamae, M., Ito, T., Matsuse, K., Tsukahara, M.: 'Performance of a high frequency quasi-resonant inverter with variable-frequency output for induction heating'. IEEE Seventh Int. Power Electronics and Motion Control Conf., Harbin, China, 2012
3 Fujita, A., Sadakata, H., Hirota, I., Omori, H., Nakaoka, M.: 'Latest developments of high-frequency series load resonant inverter type built-in cooktops for induction heated all metallic appliances'. IPEMC' 2009, pp. 2537–2544
4 Ahmed, S.M.W., Eissa, M.M., Edress, M., Abdel-Hameed, T.S.: 'Experimental investigation of full bridge Series resonant inverters for induction-heating cooking appliances'. Fourth IEEE Conf. on Industrial Electronics and Applications, ICIEA, 2009, pp. 3327–3332
5 Sheikhian, I., Kaminski, N., Vob, S., Scholz, W., Herweg, E.: 'Optimisation of the reverse conducting IGBT for zero-voltage switching applications such as induction cookers', *IET Trans. Circuits, Devices Syst.*, 2014, **8**, (3), pp. 176–181
6 Jimenez, O., Lucia, O., Urriza, I., Barragan, L.A., Navarro, D.: 'Design and evaluation of a low-cost high-performance Σ–Δ ADC for embedded control systems in induction heating appliances', *IEEE Trans. Ind. Electron.*, 2014, **61**, (5), pp. 2601–2611
7 Sarnago, H., Lucia, O., Mediano, A., Burdio, J.M.: 'Direct AC–AC resonant boost converter for efficient domestic induction heating applications', *IEEE Trans. Power Electron.*, 2014, **29**, (3), pp. 1128–1139
8 Millan, I., Burdío, J.M., Acero, J., Lucía, O., Llorente, S.: 'Series resonant inverter with selective harmonic operation applied to all-metal domestic induction heating', *IET Trans. Power Electron.*, 2011, **4**, (5), pp. 587–592
9 Meng, L., Cheng, K.W.E., Chan, K.W.: 'Systematic approach to high-power and energy-efficient industrial induction cooker system: circuit design, control strategy, and prototype evaluation', *IEEE Trans. Power Electron.*, 2011, **26**, (12), pp. 3754–3765
10 Shen, J., Ma, H., Yan, W., Hui, J., Wu, L.: 'PDM and PSM hybrid power control of a series-resonant inverter for induction heating applications'. IEEE Conf. on Industrial Electronics and Applications, ICIEA, 2006
11 Burdio, J.M., Barragan, L.A., Monterde, F., Navarro, D., Acero, J.: 'Asymmetrical voltage-cancellation control for full-bridge series resonant inverters', *IEEE Trans. Power Electron.*, 2004, **19**, (2), pp. 461–469
12 Sarnago, H., Lucia, O., Mediano, A., Burdio, J.M.: 'Class D/DE dual-mode-operation resonant converter for improved-efficiency domestic induction heating system', *IEEE Trans. Power Electron.*, 2013, **28**, (3), pp. 1274–1285
13 Jimenez, O., Lucia, O., Urriza, I., Barragan, L.A., Mattavelli, P., Boroyevich, D.: 'An FPGA-based gain-scheduled controller for resonant converters applied to induction cooktops', *IEEE Trans. Power Electron.*, 2014, **29**, (4), pp. 2143–2152
14 Forest, F., Laboure, E., Costa, F., Gaspard, J.Y.: 'Principle of a multi-load/single converter system for low power induction heating', *IEEE Trans. Power Electron.*, 2000, **15**, (2), pp. 223–230
15 Burdio, J.M., Monterde, F., Garcia, J.R., Barragan, L.A., Martinez, A.: 'A two-output series-resonant inverter for induction-heating cooking appliances', *IEEE Trans. Power Electron.*, 2005, **20**, (4), pp. 815–822
16 Zenitani, S., Okamoto, M., Hiraki, E., Tanaka, T.: 'A charge boost type multi output full bridge high frequency soft switching inverter for IH cooking appliance'. 14th Int. Power Electronics and Motion Control Conf. (EPE-PEMC), 2010, pp. T2-127–T2-133
17 Lucia, O., Burdio, J.M., Millan, I., Acero, J., Puyal, D.: 'Load-adaptive control algorithm of half-bridge series resonant inverter for domestic induction heating', *IEEE Trans. Ind. Electron.*, 2009, **56**, (8), pp. 3106–3116
18 Lucia, O., Burdio, J.M., Barragan, L.A., Carretero, C., Acero, J.: 'Series resonant multi-inverter with discontinuous-mode control for improved light-load operation', *IEEE Trans. Ind. Electron.*, 2011, **58**, (11), pp. 5163–5171
19 Lucia, O., Urriza, I., Barragan, L.A., Navarro, D., Jimenez, O., Burdio, J.M.: 'Real time FPGA-based hardware-in-the-loop simulation test bench applied to multiple-output power converters', *IEEE Trans. Ind. Appl.*, 2011, **47**, (2), pp. 853–860
20 Lucia, O., Carretero, C., Burdio, J.M., Acero, J., Almazan, F.: 'Multiple-output resonant matrix converter for multiple induction heaters', *IEEE Trans. Ind. Appl.*, 2012, **48**, (4), pp. 1387–1396
21 Primiani, V.M., Kovyryalov, S., Cerri, G.: 'Rigorous electromagnetic model of an induction cooking system', *IET Trans. Sci. Meas. Technol.*, 2012, **6**, (4), pp. 238–246
22 Carretero, C., Lucia, O., Acero, J., Alonso, R., Burdio, J.M.: 'Frequency-dependent modelling of domestic induction heating systems using numerical methods for accurate time-domain simulation', *IET Trans. Power Electron.*, 2012, **5**, (8), pp. 1291–1297
23 Meng, L.C., Eric Cheng, K.W., Chan, K.W., Lu, Y.: 'Variable turn pitch coils design for heating performance enhancement of commercial induction cooker', *IET Trans. Power Electron.*, 2012, **5**, (1), pp. 134–141
24 Acero, J., Carretero, C., Alonso, R., Burdio, J.M.: 'Quantitative evaluation of induction efficiency in domestic induction heating applications', *IEEE Trans. Magn.*, 2013, **49**, (4), pp. 1382–1389
25 Acero, J., Carretero, C., Millan, I., Lucia, O., Alonso, R., Burdio, J.M.: 'Analysis and modeling of planar concentric windings forming adaptable-diameter burners for induction heating appliances', *IEEE Trans. Power Electron.*, 2011, **26**, (5), pp. 1546–1558