IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Three-leg inverter configuration for simultaneous dual-frequency induction hardening with independent control

ISSN 1755-4535
Received on 11th April 2014
Revised on 24th November 2014
Accepted on 4th March 2015
doi: 10.1049/iet-pel.2014.0290
www.ietdl.org

S. Porpandiselvi ✉, *Neti Vishwanathan*

Department of Electrical Engineering, National Institute of Technology, Warangal, India
✉ *E-mail: porpandiselvi@gmail.com*

Abstract: Parts of certain objects need hardening. Hardening is a heat treatment process which can be achieved by induction heating. Certain objects like gears require alternating source with two different frequencies. Simultaneous application of dual frequencies is desirable for proper hardening of a gear. This study proposes a three-leg inverter topology with a load resonant circuit which can provide independent and simultaneous control of low-frequency (LF) and high-frequency (HF) currents through the load coil. The load circuit is a combination of two series resonant circuits which operates at the desired LF and HF. Power control is achieved with phase modulation and asymmetric duty cycle control techniques. A 240 W prototype of the proposed dual-frequency inverter is implemented and tested. Experimental results obtained are in good agreement with the simulation results.

1 Introduction

Induction heating is a heat treatment process which is extensively used in domestic and industrial applications. A current carrying coil surrounding the work piece induces eddy currents in it, which produces heat. Depth of penetration of induced currents on the surface of the work piece is expressed as $\delta = \sqrt{(\rho/\pi\mu f)}$. μ and ρ are the magnetic permeability and electrical resistivity of the work piece, respectively. Heat from the surface of the work piece gets transferred to the remaining part by conduction. Induction heating has several advantages like cleanliness, controllability, repeatability and high efficiency [1]. Efforts have been made to improve the power converter efficiency [2–5].

Induction heating finds applications in domestic cooking and industrial heating processes like melting, annealing, welding and surface hardening and so on. Multiple induction heating coil systems are used to achieve uniform or desired temperature distribution profile in the load. Power control is achieved with phase angle control [6, 7]. Multi-phase system modelling and current control for metal disc induction heating is proposed in [8]. Variable frequency duty cycle control and high-frequency (HF) pulse density modulation control are used in the multi-inverter system for multiple induction heaters [9]. Same multi-inverter configuration is operated with the discontinuous mode control for improvement under light-load operation [10]. The inductor coil and load system can be modelled using electro-magnetic field analysis softwares. Frequency-dependent modelling of induction heating systems is presented in [11]. Also, modelling of litz wire used in induction heating coils is presented in [12].

In surface hardening process, the surface temperature of the object is raised to its normalising value and then cooled rapidly with an appropriate fluid. It produces hard and wear resistant surface while keeping the inner part relatively soft. Certain mechanical parts such as gears, sprockets, springs and shafts are surface hardened. Unlike the conventional methods such as carburising, nitriding, flame hardening and hard chromium plating, induction surface hardening provides many advantages such as shorter heating time, minimum surface decarburising, oxidation and so on.

For surface hardening of uniform surfaced work pieces such as metal slabs and cylindrical objects, single-frequency source is sufficient [13, 14]. However, for complex surfaced work pieces such as gears and sprockets, single-frequency source is not sufficient. In case of surface hardening of gears, two-frequency or dual-frequency source is required. These two-frequency components are named as low frequency (LF) and HF. If LF alone is used, it results in good fatigue strength at the root of the work piece and abrasion resistance at the tip [15]. It also results in through hardening of the tooth and affects the ductility of the core. Use of only HF current hardens the tooth face. The root cannot be hardened without through hardening of the tooth. Simultaneous application of these two-frequency currents alleviates these difficulties. Typical ranges for the LF and HF are 10–30 and 100–400 kHz, respectively [16]. Spin hardening or tooth-by-tooth hardening method is used in gears based on the size, tooth geometry and the required hardening pattern [17].

Attempts have been made to build circuits that can produce dual-frequency currents in the load coil for gear hardening. A circuit with two resonant capacitors is proposed in [18, 19]. This circuit has a one-way short-circuit switch across one of the resonant capacitors. The on-time of switch is controlled to vary the capacitance value. This helps in changing the resonant frequency. This method offers low harmonic content in the output current and provides an indirect power control. This method has the disadvantage of low output frequency range. In [20], the above circuit is built using power metal–oxide–semiconductor field-effect transistors (MOSFETs) instead of insulated-gate bipolar transistors to increase the operating frequency range to 100 kHz or more. In [21], one more circuit with a two-way short-circuit switch across the resonant capacitor is proposed. This circuit provides HF of about ten times the LF. It gives HF range. However, the output current has harmonics. This problem is reduced by varying the shorting time of the resonant capacitor. In [22], this is further extended by adding a polarity providing circuit. This has more number of switching devices. It offers control of fundamental and third-order currents by variation of shorting time of the resonant capacitor.

In [23, 24], pulse-width modulation (PWM) inverters are reported for dual-frequency source. Single inverter is used for dual-frequency output. HF wave is modulated by medium frequency wave to produce dual-frequency output. Output control is achieved by variation of amplitude of the medium frequency wave and frequency of HF wave.

In [25, 26], multi-level inverters are proposed for dual-frequency output. Two-cell multi-level inverter is proposed and analysed with both equal and unequal sources. In this technique, control of output power is more involved.

In [27], a two inverter configuration has been proposed for dual-frequency output. The outputs of the LF and HF inverters are added and applied to the proposed load resonant circuit. Power control is achieved with phase modulation of LF and HF inverters. This configuration provides dual frequencies simultaneously and independent control of these frequency components is also possible. This configuration is suitable for high-power applications. However, two inverters are involved in the configuration.

Among the limited number of inverter topologies available for dual-frequency induction hardening application, as described above, some of the researchers have attempted to generate the desired dual-frequency outputs alternatively [18–21]. These inverters cannot supply dual-frequency currents simultaneously. The other few circuits that can supply dual-frequency currents simultaneously are also having some limitations. The circuit proposed in [22] has more number of switching devices, which leads to more cost and losses. With the single PWM inverter circuit proposed in [23, 24], during the control of the HF component of output power, output frequency itself may change in a certain range. Multi-level inverter configuration proposed in [25, 26] has more involved control. Two inverters are required in the configurations proposed in [25–27]. This increases cost and complexity.

A three-leg inverter configuration for dual-frequency induction hardening is proposed in this paper. It supplies LF and HF currents simultaneously to the load coil. It is shown in Fig. 1*a*. L_1 is inductance of the load coil around the gear. R_1 and R_2 are LF and HF equivalent resistances, respectively. L_2, C_1 and C_2 are the additional elements used in the load resonant circuit. In the proposed inverter three legs are present. First two legs are switched at LF with phase modulation control. Third leg switches at HF with a asymmetric duty cycle control [28]. The output voltages v_{o1} and v_{o2} corresponding to LF and HF, respectively, are applied to the load resonant circuit as shown in Fig. 1*a*. The load resonant circuit is a combination of two series resonant circuits. It has two resonant frequencies. Low and high switching frequencies used are 30 and 350 kHz, respectively.

2 Proposed three-leg dual-frequency inverter

In [23, 24], the output resonant circuit has load coil inductance in series with a single resistance. In the gear, current paths for LF and HF are different. The corresponding resistances for these frequencies will also be different. Hence, they have to be represented separately. The output resonant circuit of [23, 24] is suitably modified and proposed in this paper. This load resonant circuit is shown in Fig. 1*b*.

Fig. 1*a* shows the schematic diagram of the proposed three-leg dual-frequency inverter. First two legs form one full bridge inverter operating at LF. Power control in this inverter is achieved through phase modulation control. First and third legs form another full bridge inverter. The third leg is switched at HF with asymmetric duty cycle control, whereas first leg remains switched at LF only. v_{o1} and v_{o2} are LF and HF output voltages of the three-leg inverter, respectively. v_{o1} is obtained from first and second legs. v_{o2} is obtained from first and third legs. These voltages are applied to the load resonant circuit as shown in Fig. 1*a*. The load resonant circuit includes the load coil of inductance L_1, resonant capacitors C_1, C_2 and an additional resonant inductor L_2 (not part of the load coil). R_1 and R_2 are the equivalent resistances referred to the load coil for HF and LF current paths of work piece, respectively. The load coil inductance L_1 is connected to first leg, which is common for both output voltages v_{o1} and v_{o2}. V_{DC} is the supply voltage. i_o is the inverter output current, which flows through the load coil. i_{lf} and i_{hf} are the LF and HF components of the load current i_o.

Thus output voltages v_{o1} and v_{o2} can be at any one of the three levels, $+V_{DC}$, 0 or $-V_{DC}$ depending on the switching state of the devices. Fig. 1*c* depicts these voltages along with gate pulses (V_{S_1} to V_{S_6}) of switching devices S_1–S_6 and output currents at $D_l = D_h = 0.5$. Here, D_l and D_h are duty cycles of LF and HF switching devices and are defined as

$$D_l = \frac{t_{lon}}{(t_l/2)}$$

and

$$D_h = \frac{t_{hon}}{(t_h/2)}$$

respectively as shown in Fig. 1*c*. Gating pulses of S_1 and S_2 are fixed with respect to each other. Phase modulation of LF gating pulses of second leg with respect to first leg changes duty cycle of voltage v_{o1}. v_{o2} is controlled by an asymmetric duty cycle control of HF leg. As voltages v_{o1} and v_{o2} are controllable, the corresponding LF and HF current components in inductor L_1 are also controllable. These currents in L_1 regulate LF and HF currents in the load (gear). Thus I^2R loss in LF and HF current paths of the gear is controlled. Root and tip regions of the gear are LF and HF current regions of the gear, respectively. To establish the proposed technique, experimental set up is built with discrete components of suitable values, as listed in Table 1. Actual gear is not used.

3 Proposed load resonant circuit

Proposed load resonant circuit is shown in Fig. 1*b*. This circuit can be considered as a combination of two series resonant circuits, one corresponding to low switching frequency (ω_l) and the other corresponding to high switching frequency (ω_h) with resonant frequencies of ω_{rl} and ω_{rh}, respectively. Low and high switching frequencies can be up to 10% higher than the corresponding resonant frequencies. As the difference between low and high switching frequencies is large (about ten times), the difference between the corresponding resonant frequencies is also of the same magnitude. Hence, the values of reactive elements of the LF resonant circuit are much larger than those of the HF resonant circuit.

At $\omega = \omega_l$, the reactance of capacitor C_1 is $|X_{C_{1l}}| = (1/\omega_l C_1)$. As C_1 is much smaller than C_2, it offers considerably higher reactance to the LF components and can be considered as an open circuit for LF components present in the voltage v_{o2}. The equivalent circuit as seen by LF components is shown in Fig. 2*a*. Thus the LF current from v_{o1} flows through the elements L_1, L_2, C_2 and R_2. The impedance of this LF current path is expressed as

$$Z_{2l} = R_2 + j\left(\omega_l(L_1 + L_2) - \frac{1}{\omega_l C_2}\right) \quad (1)$$

Hence the values of L_2 and C_2 are selected such that $L_1 + L_2$ and C_2 resonate at low resonant frequency (ω_{rl}) of the circuit. At LF resonance

$$\omega_{rl}(L_1 + L_2) = \frac{1}{\omega_{rl} C_2} \quad (2)$$

and the impedance of the LF current path at this frequency becomes Z_{2rl}=R_2. Thus the elements L_1, L_2, C_2 and R_2 form a series resonant circuit at LFs.

At $\omega = \omega_h$, the reactance of L_2 is $|X_{L2h}| = \omega_h L_2$. As the value of L_2 is large, its reactance is considerably high and this inductor can be considered as an open circuit for HF components present in v_{o1}. The equivalent circuit as seen by the HF components in v_{o2} is shown in Fig. 2*b*.

Thus the HF current component flows through elements L_1, C_1 and R_1. The impedance of this HF current path is expressed as

$$Z_{1h} = R_1 + j\left(\omega_h L_1 - \frac{1}{\omega_h C_1}\right) \quad (3)$$

IET Power Electron., 2015, Vol. 8, Iss. 9, pp. 1571–1582

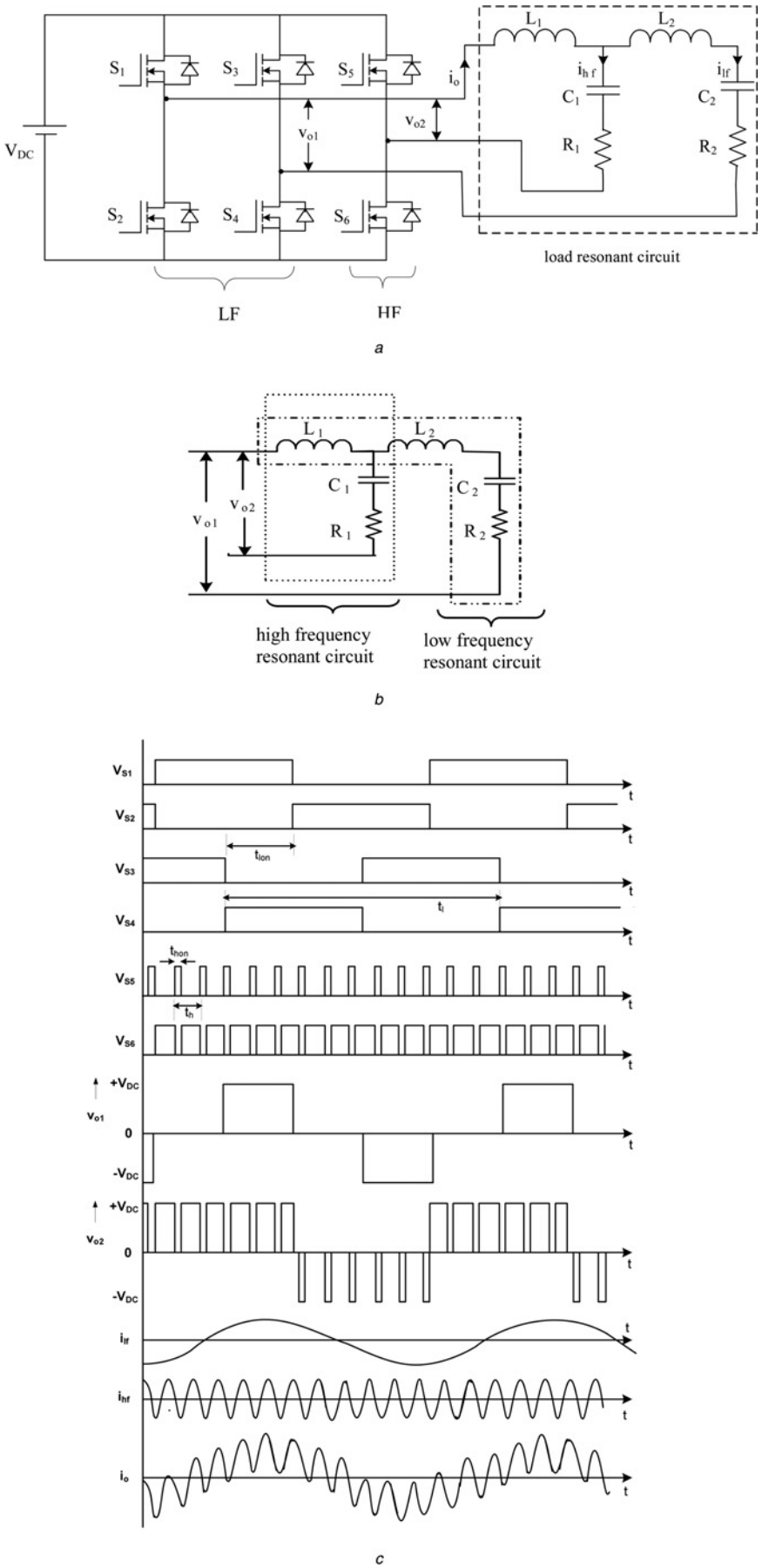


Fig. 1 *Proposed inverter circuit*

a Proposed three-leg dual frequency inverter with load resonant circuit
b Load resonant circuit
c Gate pulses, v_{o1}, v_{o2}, i_{lf}, i_{hf} and i_o at $D_l = D_h = 0.5$

Table 1 Parameters of the proposed dual frequency inverter

Inductance of the load coil, L_1	6.09 μH
HF resonant capacitor, C_1	0.036 μF
HF equivalent resistance, R_1	8.2 Ω
LF resonant inductor, L_2	47.63 μH
LF resonant capacitor, C_2	0.604 μF
LF equivalent resistance, R_2	5.39 Ω
Low switching frequency, f_l	30 kHz
High switching frequency, f_h	350 kHz
Switching devices used	MOSFET IRF540
Control and driver ICs used	UC 3875, MC 4424 and IR 2110

Hence L_1 and C_1 values are selected such that they resonate at high resonant frequency (ω_{rh}) of the circuit. At HF resonance

$$\omega_{rh}L_1 = \frac{1}{\omega_{rh}C_1} \tag{4}$$

and the impedance of the HF current path at this frequency becomes $Z_{1rh}=R_1$. Thus at HFs, the elements L_1, C_1 and R_1 form a series resonant circuit.

Hence the load resonant circuit can be considered as a combination of LF and HF series resonant circuits as shown in Fig. 1*b*. When voltages v_{o1} and v_{o2} are applied to this proposed load resonant circuit, both LF and HF currents flow through the load coil L_1.

The admittance characteristics of LF and HF paths of the load resonant circuit are shown in Figs. 2*c* and *d*, respectively. These admittance characteristics justify the description given above for the load resonant circuit when operated under dual-frequency supply. The quality factors of LF and HF resonant circuits are expressed as

$$Q_l = \frac{1}{R_2}\sqrt{\frac{(L_1+L_2)}{C_2}} \tag{5}$$

$$Q_h = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} \tag{6}$$

The circuit parameters of Fig. 1*b* are shown in Table 1.

3.1 Load circuit design

In practice, for the design of the complete load resonant circuit, low and high switching frequencies ω_l and ω_h may be selected based on depth of hardening required. Low and high resonant frequencies ω_{rl} and ω_{rh} are to be selected slightly below their switching frequencies. L_1 and L_2 are calculated for selected values of C_1, C_2 and two resonant frequencies using (4) and (2), respectively. L_1 is formed by winding the coil around the gear with suitable wire size. As mentioned earlier, L_2 is an additional inductance used. It is not part of the load coil L_1. For calculation of the power, R_1 and R_2 need to be measured.

In this load resonant circuit, the low and high switching frequencies f_l and f_h are selected as 30 and 350 kHz, respectively. The corresponding resonant frequencies are assumed to be 27.94 and 339.91 kHz, respectively. The LF and HF circuit resonant capacitors C_2 and C_1 are selected as 0.604 and 0.036 μF, respectively. Now, the equivalent inductance of the load coil, L_1

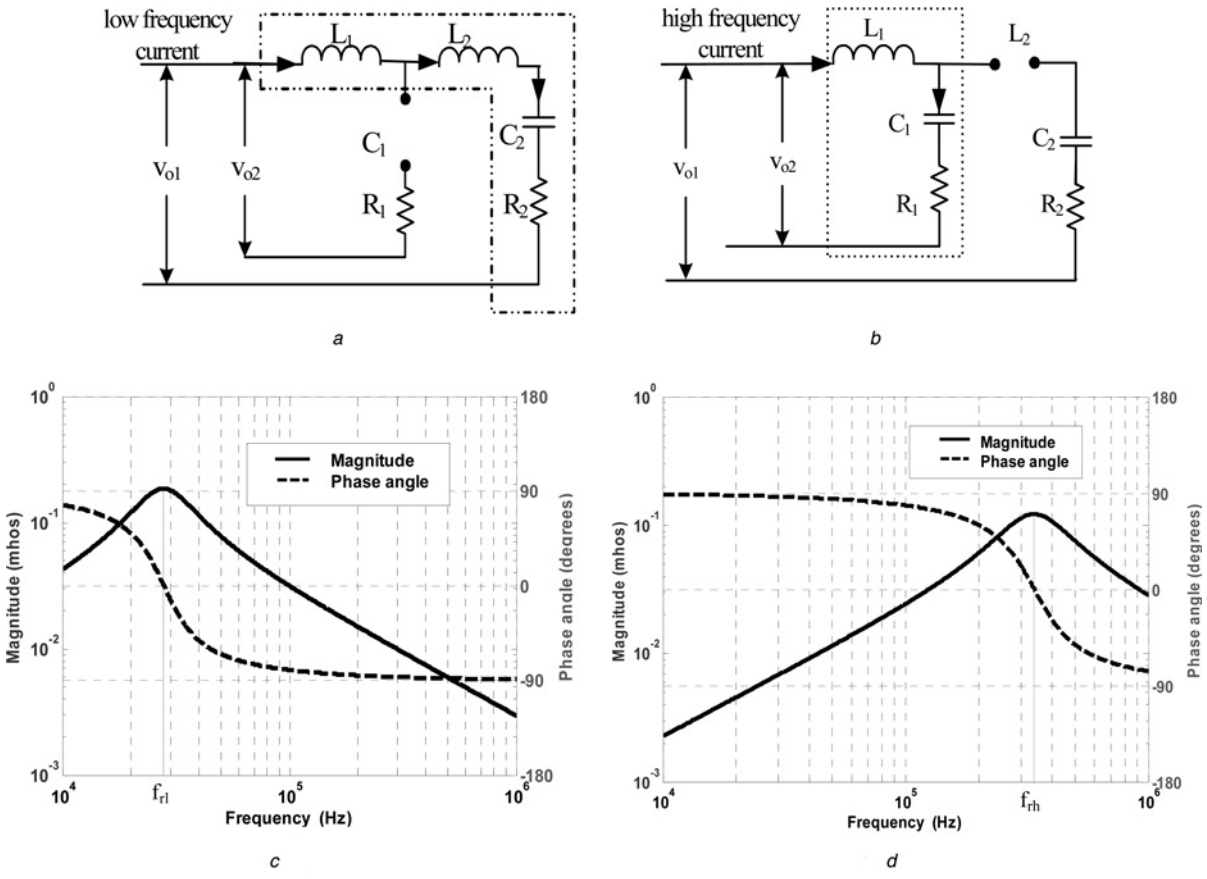


Fig. 2 *LF and HF load equivalent circuits and its characteristics*

a Equivalent circuit for LF component
b Equivalent circuit for HF component
c Admittance characteristic of LF path
d Admittance characteristic of HF path

IET Power Electron., 2015, Vol. 8, Iss. 9, pp. 1571–1582

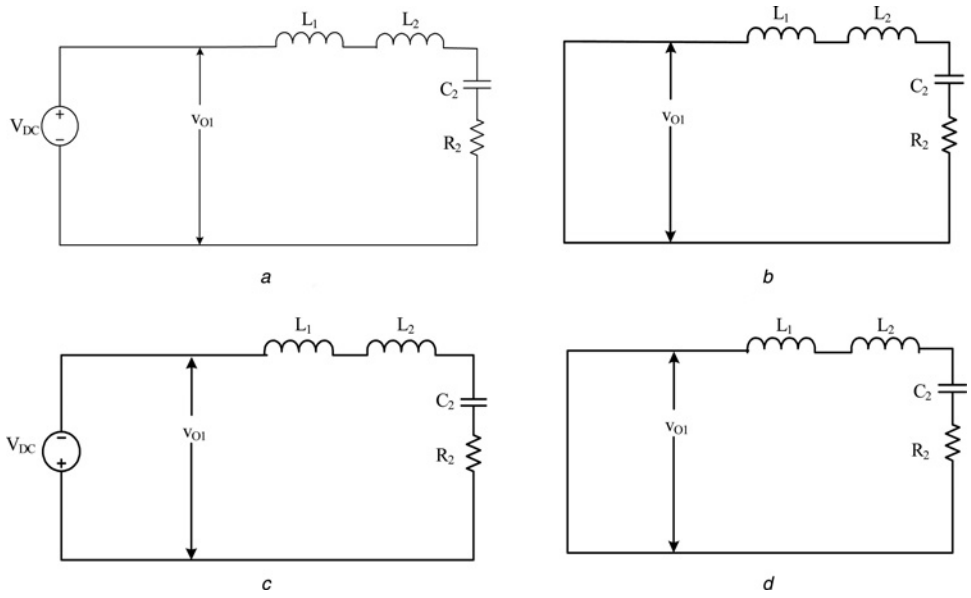


Fig. 3 *Equivalent circuits of inverter for different modes of LF operation*

a Mode 1: S_1 and S_4 are ON
b Mode 2: S_2 and S_4 are ON
c Mode 3: S_2 and S_3 are ON
d Mode 4: S_1 and S_3 are ON

and LF resonant inductor L_2 can be calculated using (4) and (2) as 6.09 and 47.63 μH, respectively.

4 Inverter operation

As explained in the previous section, the load circuit can be considered as two independent series resonant circuits, namely HF and LF resonant circuits as shown in Figs. 2*a* and *b*. The inductor L_1 is the common element in these two circuits. Each of these two circuits is operating as an RLC series resonant circuit at different intervals of time corresponding to a particular value of v_{o1} or v_{o2}. As shown in Fig. 1*c*, at any instant of time, the three-leg inverter output voltages v_{o1} and v_{o2} attain any one value among the three levels of $+V_{DC}$, 0 and $-V_{DC}$. Equivalent circuits of the three-leg inverter for different modes of operations are shown in Figs. 3 and 4.

4.1 LF operation of the inverter

The instantaneous value of LF output voltage v_{o1} depends on the switching states of first and second leg devices. When S_1 is ON, v_{o1} can be zero or V_{DC} depending on whether S_3 or S_4 is ON, respectively. When S_2 is ON, v_{o1} is $-V_{DC}$ or zero when S_3 or S_4 is ON, respectively. These four different modes are shown in Fig. 3.

For understanding the operation of this circuit under different modes, the switching pulses to the devices of LF legs, LF output voltage v_{o1} and LF output current i_{lf} are shown in Fig. 1*c* at a duty cycle of $D_l = 0.5$. As shown in Fig. 3, the circuit operation during different modes is analysed below.

4.1.1 Mode 1 ($t_1 \le t \le t_2$): This mode starts when S_1 and S_4 are turned on and the corresponding equivalent circuit is shown in Fig. 3*a*. Let $t' = t - t_1$ so that during mode 1, $0 \le t' \le (t_2 - t_1)$. During this interval $v_{o1} = +V_{DC}$. Now, the instantaneous LF current i_{lf} is expressed as

$$(L_1 + L_2)\frac{di_{lf}(t')}{dt'} + \frac{1}{C_2}\int i_{lf}(t')\,dt' + v_c2(t' = 0) + R_2 i_{lf}(t') = +V_{DC} \tag{7}$$

where $i_{lf}(t' = 0) = i_{lf}(t_1) = I_{lf1}$ and voltage across capacitor C_2 at $t' = 0$ is $v_{c2}(t_1) = V_{c21}$.

Solving (7)

$$i_{lf}(t') = I_{tl1}\, e^{-\alpha t'} \sin \omega_n t' + I_{lf1}\, e^{-\alpha t'}\left(\cos \omega_n t' - \alpha_n \sin \omega_n t'\right) \tag{8}$$

and

$$v_{c2}(t') = V_{c21} + (V_{DC} - V_{c21})\left(1 - e^{-\alpha t'}\left(\cos \omega_n t' + \alpha_n \sin \omega_n t'\right)\right) + V_{tl1}\, e^{-\alpha t'} \sin \omega_n t' \tag{9}$$

where

$$\omega_n = \sqrt{\frac{1}{(L_1 + L_2)C_2} - \left(\frac{R_2}{2(L_1 + L_2)}\right)^2} \tag{10}$$

$$\alpha = \frac{R_2}{2(L_1 + L_2)} \tag{11}$$

$$\alpha_n = \frac{\alpha}{\omega n} \tag{12}$$

$$I_{tl1} = \left(\frac{V_{DC} - V_{c21}}{\omega_n (L_1 + L_2)}\right) \tag{13}$$

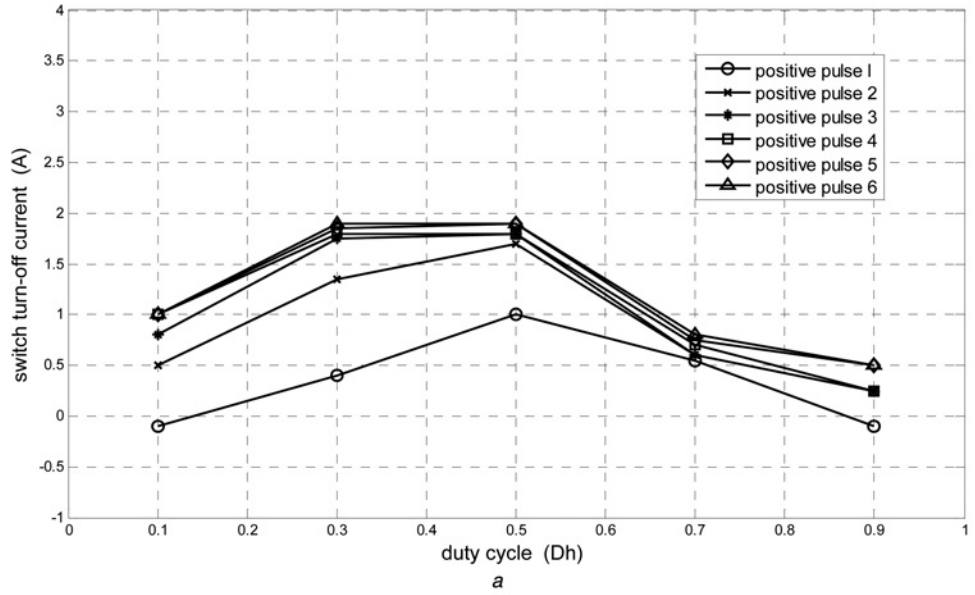
and

$$V_{tl1} = \frac{I_{lf1}}{\omega_n C_2} \tag{14}$$

This mode ends at $t = t_2$.

4.1.2 Mode 2 ($t_2 \le t \le t_3$): This mode starts when S_2 and S_4 are turned on and the corresponding equivalent circuit is shown in Fig. 3*b*. Let $t'' = t - t_2$ so that during mode 2, $0 \le t'' \le (t_3 - t_2)$. During this interval $v_{o1} = 0$.

$i_{lf}(t_2) = I_{lf2}$ and voltage across capacitor C_2 at $t'' = 0$ is $v_{c2}(t_2) = V_{c22}$.



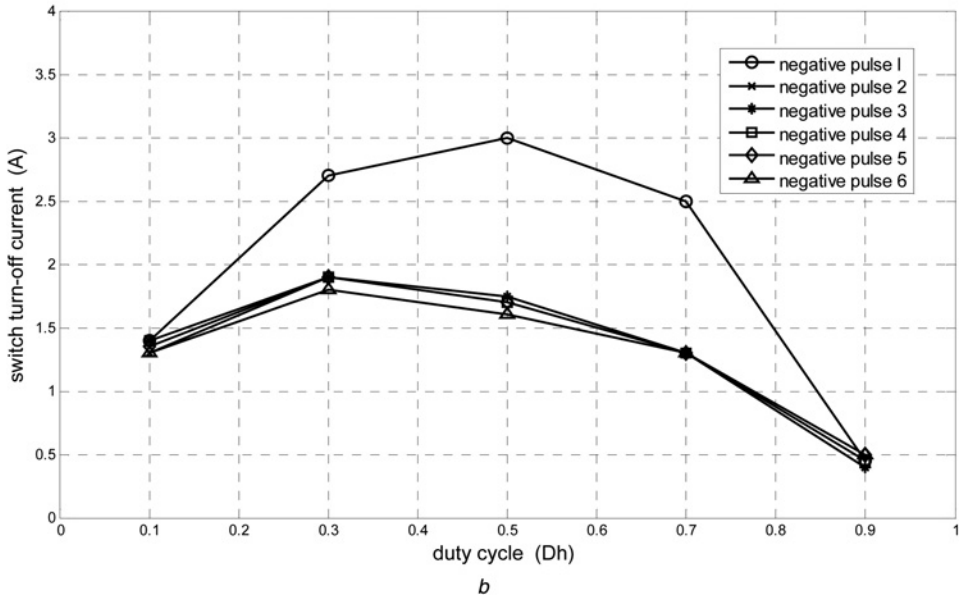


Fig. 4 *Switch turn-off currents of S_5 at $D_l = 0.9$*

a During positive half cycle
b During negative half cycle
c Waveforms of v_{o2} and i_{hf} for $D_l = D_h = 0.9$
d Waveforms of v_{o2} and i_{hf} for $D_l = D_h = 0.5$

Now the instantaneous current is described by

$$i_{lf}(t'') = I_{tl2}\,e^{-\alpha t''}\sin\omega_n t'' + I_{lf2}\,e^{-\alpha t''}\left(\cos\omega_n t'' - \alpha_n \sin\omega_n t''\right) \quad (15)$$

and

$$v_{c2}(t'') = V_{c22} - V_{c22}\left(1 - e^{-\alpha t''}\left(\cos\omega_n t'' + \alpha_n \sin\omega_n t''\right)\right) + V_{tl2}\,e^{-\alpha t''}\sin\omega_n t'' \quad (16)$$

where

$$I_{tl2} = \left(\frac{-V_{c22}}{\omega_n(L_1 + L_2)}\right) \quad (17)$$

and

$$V_{tl2} = \frac{I_{lf2}}{\omega_n C2} \quad (18)$$

This mode ends at $t = t_3$.

4.1.3 Mode 3 ($t_3 \le t \le t_4$): This mode starts when S_2 and S_3 are turned on and the corresponding equivalent circuit is shown in Fig. 3*c*. Let $t'' = t - t_3$ so that during this mode, $0 \le t'' \le (t_4 - t_3)$. During this interval $v_{o1} = -V_{DC}$.

$i_{lf}(t'' = 0) = i_{lf}(t_3) = I_{lf3}$ and voltage across capacitor C_2 at $t'' = 0$ is $v_{c2}(t_3) = V_{c23}$

$$i_{lf}(t''') = I_{tl3}\,e^{-\alpha t'''}\sin\omega_n t''' + I_{lf3}\,e^{-\alpha t'''}\left(\cos\omega_n t''' - \alpha_n \sin\omega_n t'''\right) \quad (19)$$

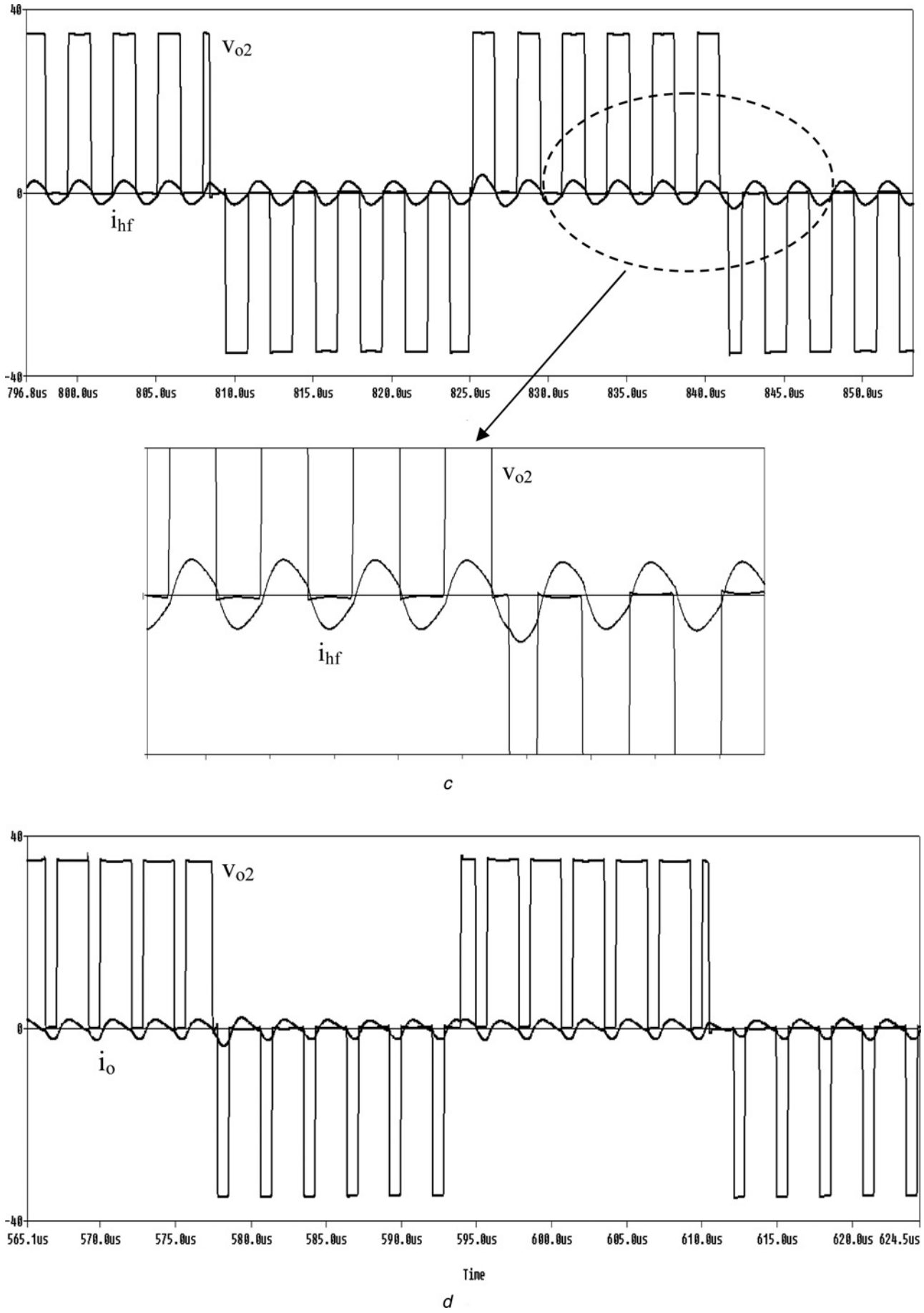


Fig. 4 *Continued*

Table 2 Prototype specifications

Output power	240 W
Input voltage	35 Vdc
Low switching frequency, f_l	30 kHz
High switching frequency, f_h	350 kHz
LF output current, I_{lf}	6.3 A
HF output current, I_{hf}	1.8 A

and

$$v_{c2}(t''') = V_{c23} - (V_{DC} + V_{c23})\left(1 - e^{-\alpha t'''}\left(\cos \omega_n t''' + \alpha_n \sin \omega_n t'''\right)\right) + V_{tl3}\, e^{-\alpha t'''} \sin \omega_n t''' \quad (20)$$

where

$$I_{tl3} = \left(\frac{-V_{DC} - V_{c23}}{\omega_n(L_1 + L_2)}\right) \quad (21)$$

and

$$V_{tl3} = \frac{I_{lf3}}{\omega_n C_2} \quad (22)$$

This mode ends at $t = t_4$.

4.1.4 Mode 4 ($t_4 \le t \le t_5$): This mode starts when S_1 and S_3 are turned on and the corresponding equivalent circuit is shown in Fig. 3*d*. Let $t^{iv} = t - t_4$ so that during this mode, $0 \le t^{iv} \le (t_5 - t_4)$. During this interval again v_{o1} becomes zero.

$i_{lf}(t^{iv} = 0) = i_{lf}(t_4) = I_{lf4}$ and voltage across capacitor C_2 at $t^{iv} = 0$ is $v_{c2}(t_4) = V_{c24}$.

$$i_{lf}(t^{iv}) = I_{tl4}\, e^{-\alpha t^{iv}} \sin \omega_n t^{iv} + I_{lf4}\, e^{-\alpha t^{iv}}\left(\cos \omega_n t^{iv} - \alpha_n \sin \omega_n t^{iv}\right) \quad (23)$$

and

$$v_{c2}(t^{iv}) = V_{c24} - V_{c24}\left(1 - e^{-\alpha t^{iv}}\left(\cos \omega_n t^{iv} + \alpha_n \sin \omega_n t^{iv}\right)\right) + V_{tl4}\, e^{-\alpha t^{iv}} \sin \omega_n t^{iv} \quad (24)$$

where

$$I_{tl4} = \left(\frac{-V_{c24}}{\omega_n(L_1 + L_2)}\right) \quad (25)$$

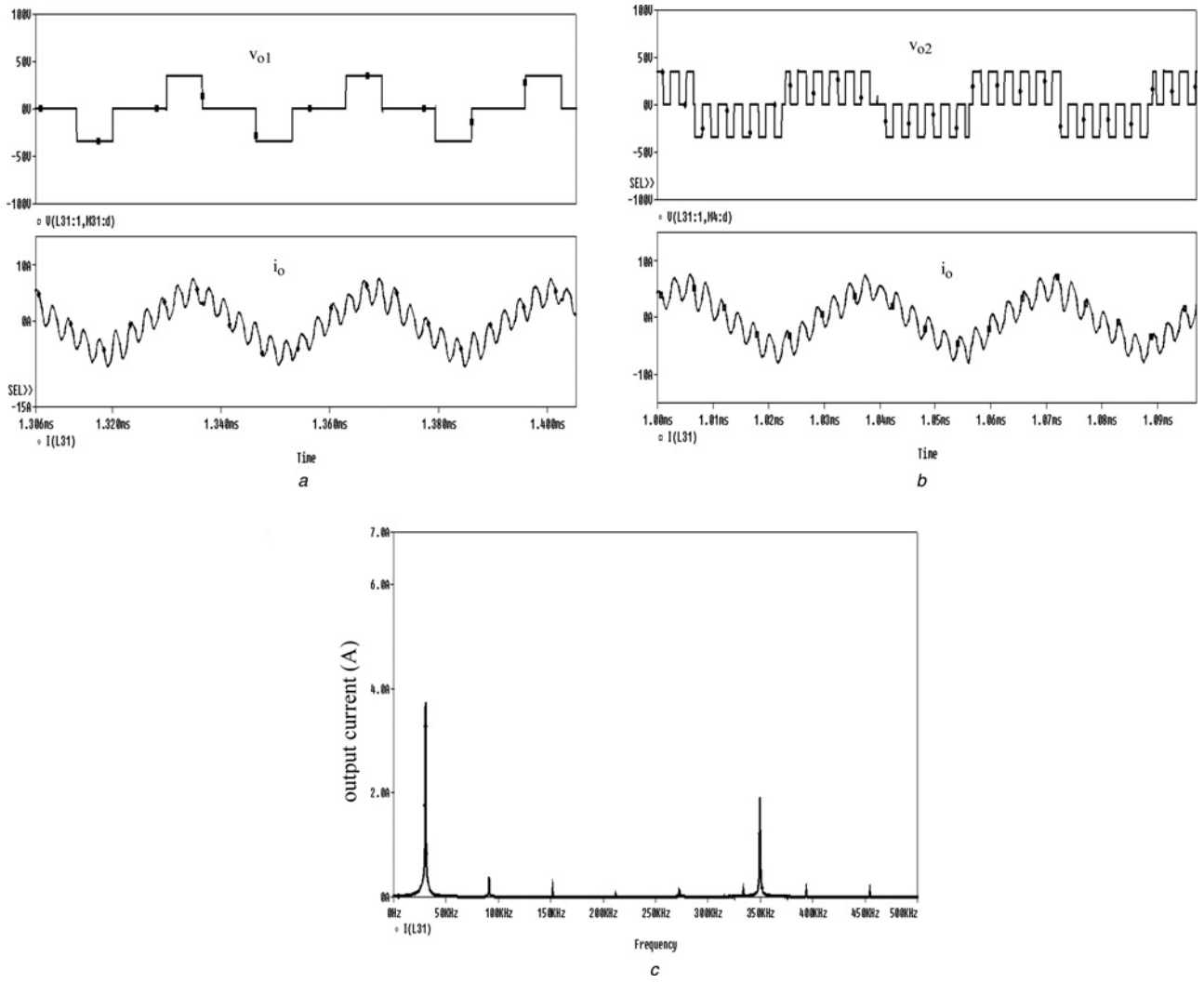


Fig. 5 *Simulation results for $D_l = 0.4$, $D_h = 0.9$*

a Simulation waveforms of v_{o1} and i_o
b Simulation waveforms of v_{o2} and i_o
c FFT of simulated output current i_o

IET Power Electron., 2015, Vol. 8, Iss. 9, pp. 1571–1582

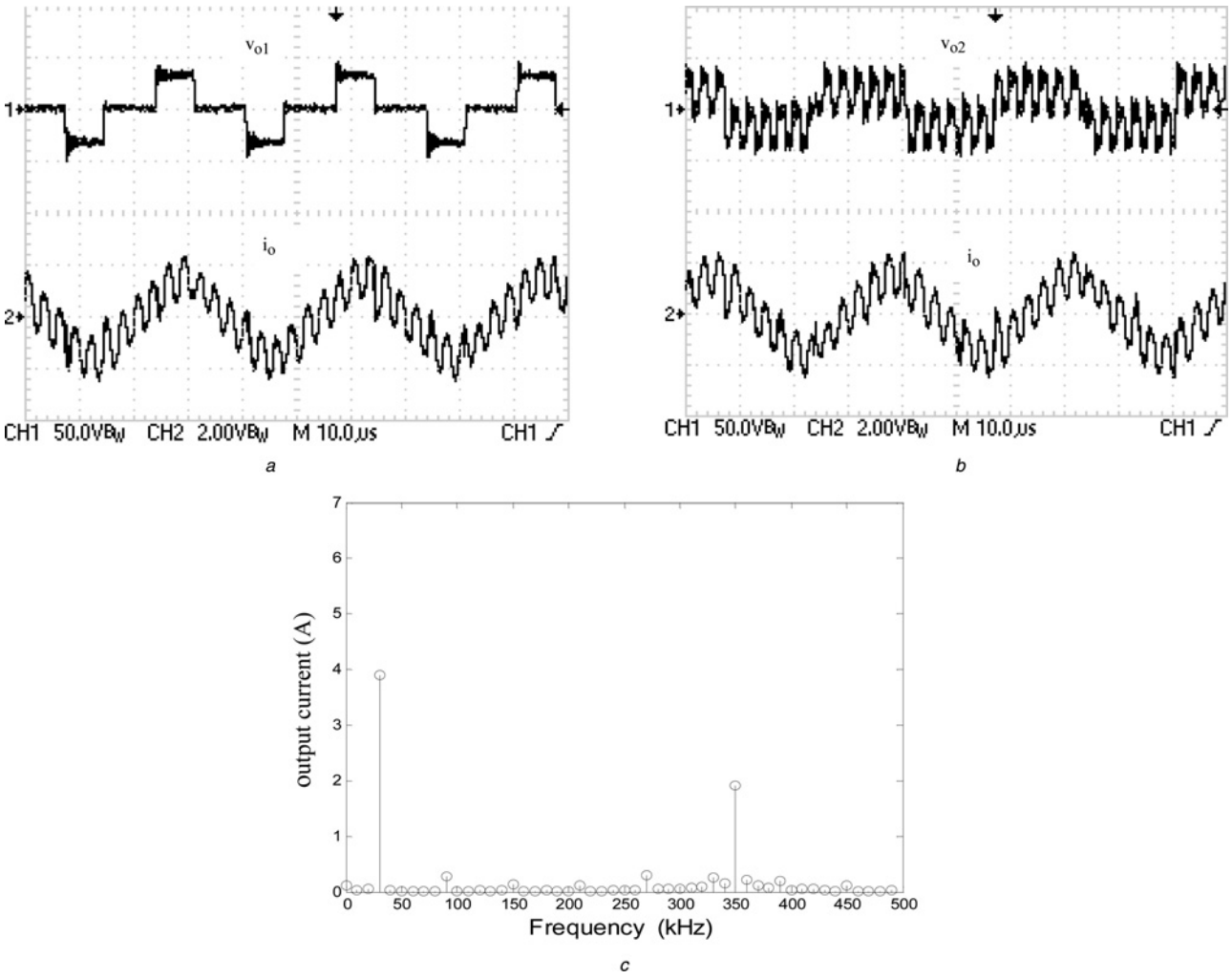


Fig. 6 *Experimental results for $D_l = 0.4$, $D_h = 0.9$*

a Experimental waveforms of v_{o1} and i_o (v_{o1}: 50 V/div, i_o: 8 A/div, t: 10 µs/div)
b Experimental waveforms of v_{o2} and i_o (v_{o1}: 50 V/div, i_o: 8 A/div, t: 10 µs/div)
c FFT of experimental output current i_o

and

$$V_{tl4} = \frac{I_{lf4}}{\omega_n C_2} \tag{26}$$

This mode ends at $t = t_5$.

Thus the current through LF resonant circuit $i_{lf}(t)$ has been expressed through (8), (15), (19) and (23) during different modes of operations.

In Fig. 1*c*, the switching pulses used in the first two legs of the inverter which are operating at LF are shown. These waveforms are shown at a duty cycle of $D_l = 0.5$. These first and second leg devices S_1–S_4 are controlled with phase shift control of switching pulses as shown in this figure. Switching pulses to the devices in the same leg should be always 180° shifted. Switching pulses to the opposite devices are shifted in phase as shown in this figure. Thus the pulse width of the resultant voltage v_{o1} and thereby the magnitude of the LF current i_{lf} are controlled through the phase shift control of switching pulses as explained above. These switching pulses have been derived using UC 3875 Phase Shift Resonant Controller and the driver IC used is MC4424.

4.2 HF operation of the inverter

The HF output voltage v_{o2} is independent of switching states of second leg devices. When S_1 is ON, v_{o2} is zero or V_{DC} depending on whether S_5 or S_6 is ON, respectively. Similarly, when S_2 is ON, v_{o2} is $-V_{DC}$ or zero based on whether S_5 or S_6 is ON, respectively. Similar to LF operation the HF operation also has four different modes. Equivalent circuits of inverter for these different modes of HF operation are similar to LF equivalent circuits shown in Fig. 3 with HF circuit components and input voltage V_{02}. The switching pulses to the devices of the first and third legs of the inverter and the corresponding HF output voltage v_{o2} and HF output current i_{hf} are shown in Fig. 1*c* at a duty cycle of $D_h = 0.5$.

During different modes of operation, the expressions for instantaneous HF current i_{hf} and capacitor voltages can be derived from the loop equation in a similar way like LF current expressions.

In general, during any interval, the loop equation of HF resonant load circuit can be written as

$$L_1 \frac{\mathrm{d}i_{hf}(t)}{\mathrm{d}t} + \frac{1}{C_1}\int i_{hf}(t)\,\mathrm{d}t + v_{c1}(t=0) + R_1 i_{hf}(t) = v_{o2} \tag{27}$$

With initial values of $i_{hf} = I_{hfo}$ and $v_{c1} = V_{c1o}$, the solution of this equation is

$$i_{hf}(t) = I_{th0}\,\mathrm{e}^{-\alpha t}\sin\omega_n t + \left(I_{hf0}\,\mathrm{e}^{-\alpha t}\left(\cos\omega_n t - \alpha_n \sin\omega_n t\right)\right) \tag{28}$$

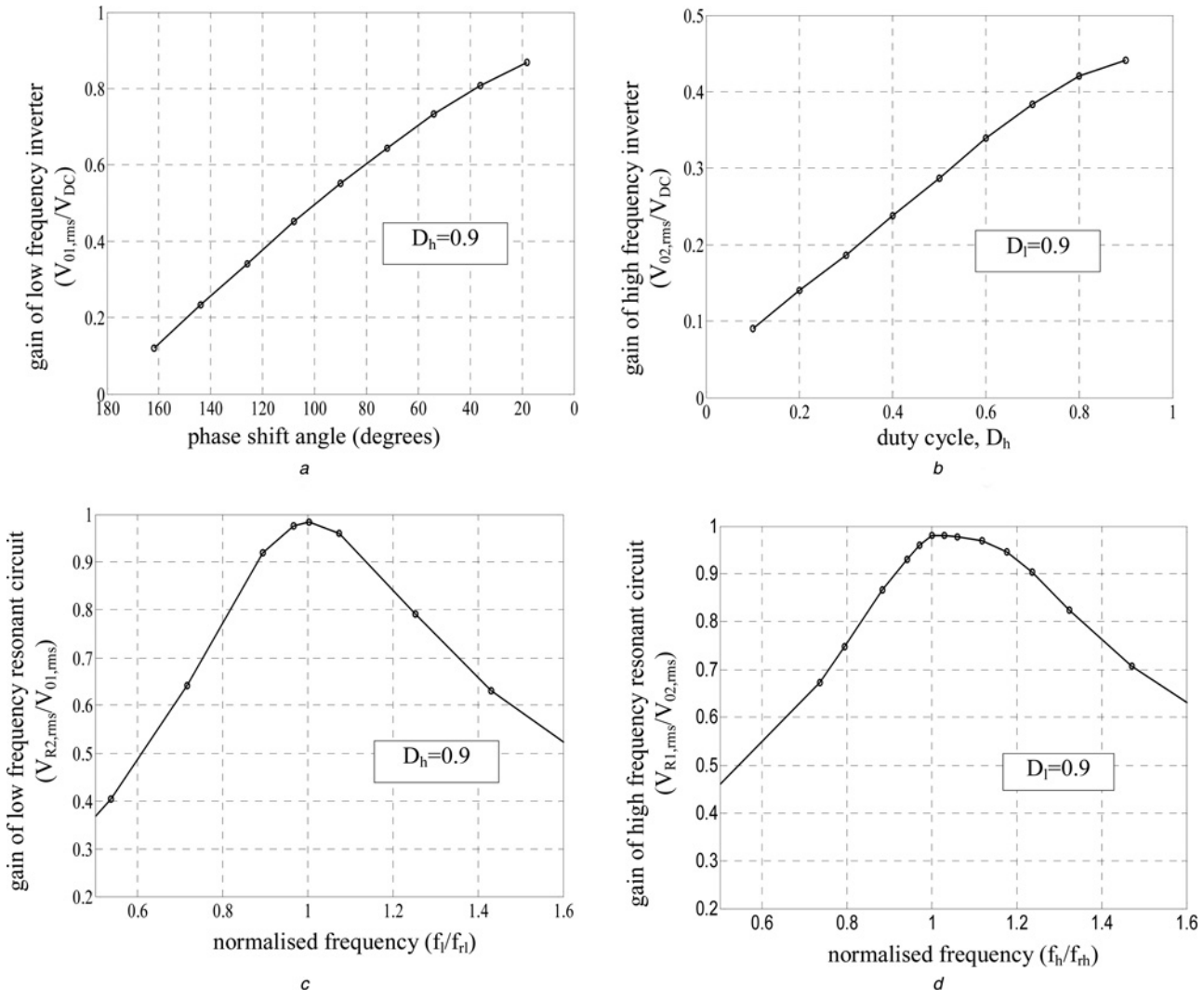


Fig. 7 *Gain characteristics of inverter*

a Gain of LF inverter ($V_{01,rms}/V_{DC}$) against phase shift angle
b Gain of HF inverter ($V_{02,rms}/V_{DC}$) against duty cycle (D_h)
c Gain of LF resonant circuit ($V_{R2,rms}/V_{01,rms}$) against normalised frequency (f_l/f_{rl})
d Gain of HF resonant circuit ($V_{R1,rms}/V_{02,rms}$) against normalised frequency (f_h/f_{rh})

and

$$v_{c1}(t) = V_{c10} + (v_{o2} - V_{c10})\left(1 - e^{-\alpha t}\left(\cos \omega_n t + \alpha_n \sin \omega_n t\right)\right) + V_{th0}\, e^{-\alpha t} \sin \omega_n t \quad (29)$$

where

$$\alpha = \frac{R_1}{2L_1} \quad (30)$$

$$\omega_n = \sqrt{\frac{1}{L_1 C_1} - \left(\frac{R_1}{2L_1}\right)^2} \quad (31)$$

$$\alpha_n = \frac{\alpha}{\omega_n} \quad (32)$$

and

$$V_{th0} = \frac{I_{hf0}}{\omega_n C_1} \quad (33)$$

Thus during each mode, by substituting the corresponding value of v_{o2} and initial conditions, the HF resonant circuit current $i_{hf}(t)$ expressions can be obtained using the above equations.

Thus, the instantaneous value of current through the load coil can be expressed as

$$i_o(t) = i_{lf}(t) + i_{hf}(t) \quad (34)$$

Total power loss in the inverter circuit may be expressed as

$$P_{Loss} = V_{DC} I_{DC} - \left(I_{1hf}^2 R_1 + I_{1lf}^2 R_2\right) \quad (35)$$

where I_{1lf} and I_{1hf} are the fundamental components of the LF and HF resonant circuit currents, respectively.

On the basis of the above analysis, ZVS conditions are analysed and plotted in Figs. 4*a* and *b*. ZVS of third leg is determined by waveforms v_{o2} and i_{hf}. Fig. 4*c* shows waveforms of v_{o2} and i_{hf} for $D_l = D_h = 0.9$. Fig. 4*d* shows waveforms of v_{o2} and i_{hf} for $D_l = D_h = 0.5$. v_{o2} contains positive and negative half cycles. In each half cycle, the certain number of pulses is present, which depend on the duty cycle of the LF leg (leg-1). Figs. 4*a* and *b* show switch turn-off currents of S_5 for positive and negative half cycles, respectively. These figures are shown for $D_l = 0.9$ of leg-1 and different values of D_h.

For positive half cycle, switch turn-off current of each pulse increases with increasing duty cycle and then it reduces. Switch turn-off currents are positive for all pulses. For pulse-1, at minimum and maximum duty cycles, switch turn-off current is negative. This is because of the change of polarity of pulses at the cross over. For negative half cycle also, switch turn-off currents increase with increasing duty cycle and then decrease. The increase of switch turn-off current for pulse-1 with duty cycle is more compared to other pulses. Again, this is because of the change of polarity of pulses at the cross over. As switch turn-off currents of S_5 are positive in most of the conditions, ZVS can be achieved. From this figure, it is also observed that for any given D_h, switch turn-off currents are different from pulse to pulse in both positive and negative half cycles. Hence complete ZVS may not be possible for every pulse. A similar condition will exist for switch S_6 also.

The first leg of the inverter operates at LF and the third leg operates at HF. The first leg switching pulses are always at 180° phase shift. Third leg devices S_5 and S_6 are controlled with asymmetric duty cycle control. When the ON period of switching pulse to S_5 is 't_{hon}', the ON period of switching pulse to S_6 is (t_h–t_{hon}) as shown in Fig. 1*c*. Thus the HF pulse width of the resultant voltage v_{o2} and thereby the magnitude of the HF current i_{hf} are controlled through the asymmetric duty cycle control of HF switching pulses as explained above. These HF gating pulses have been derived using UC 3875 Phase Shift Resonant Controller and logic gates. The driver IC used is IR2110.

As shown in Figs. 2*a* and *b*, the load coil inductor is the common element for both these LF and HF currents. Thus at any instant of time the current through the load coil is the sum of LF and HF currents.

5 Experimental and simulation results

A 240 W prototype of the proposed dual-frequency inverter has been implemented. The low and high switching frequencies are 30 and 350 kHz, respectively. IRF540 Power MOSFETs are used as switching devices. The input voltage $V_{DC} = 35$ V. The prototype specifications are shown in Table 2.

LF and HF output currents and corresponding output powers are controlled by phase modulation and asymmetric duty cycle control of the corresponding legs of the inverter, respectively. Simulation and experimental results are shown below. Figs. 5*a–c* show simulation waveforms for $D_l = 0.4$ and $D_h = 0.9$. Figs. 6*a–c* show experimental waveforms for $D_l = 0.4$ and $D_h = 0.9$. In the experimental waveforms, channel 1 corresponds to 50 V/div and channel 2 corresponds to 8 A/div.

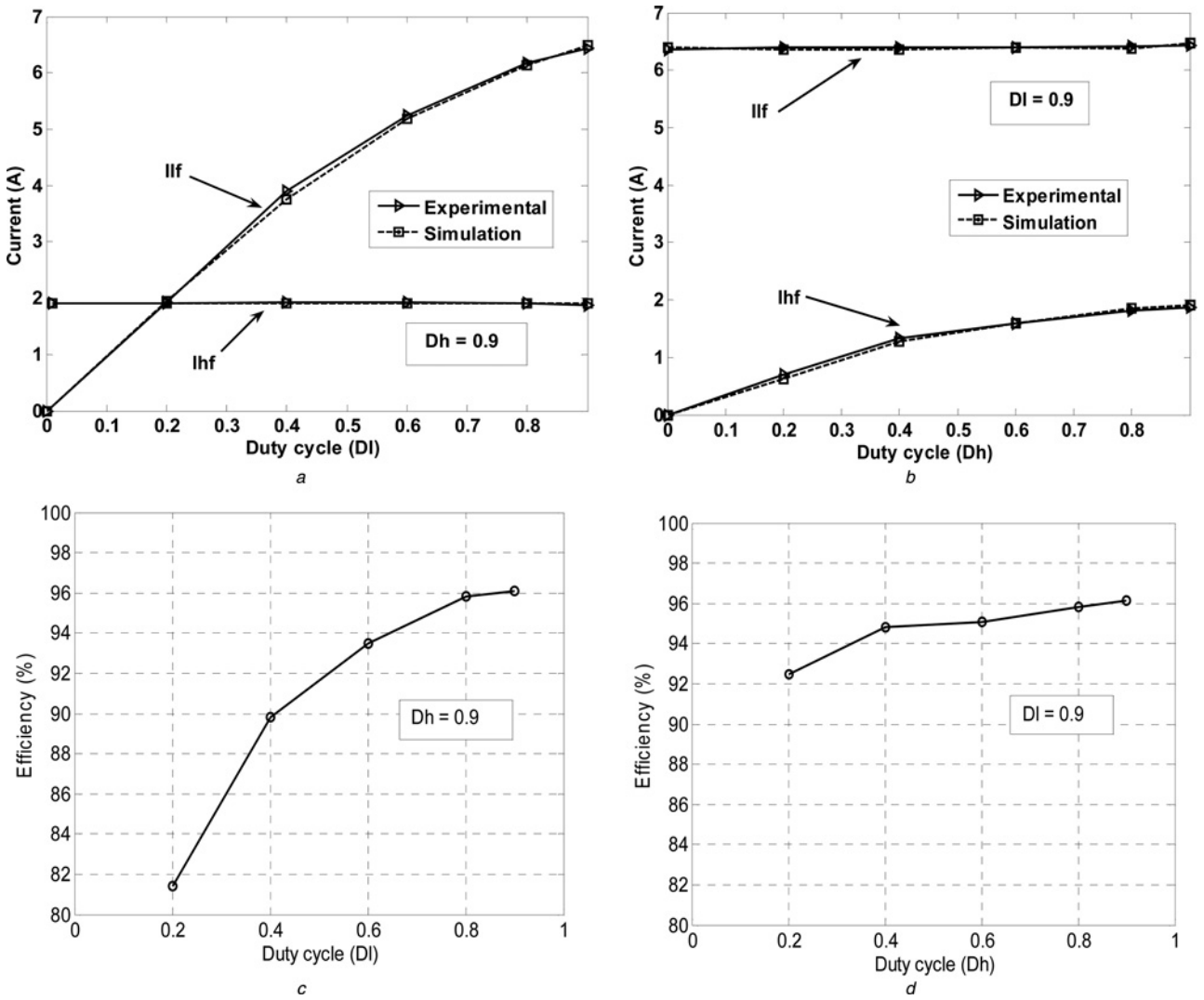


Fig. 8 *Graphs showing independent control and efficiencies*

a i_{lf} and i_{hf} against LF inverter duty cycle (D_l)
b i_{lf} and i_{hf} against HF inverter duty cycle (D_h)
c Overall efficiency against LF duty cycle
d Overall efficiency against HF duty cycle

From the above figures, it is observed that the experimental results obtained are in good agreement with simulation results. It is also seen that the proposed inverter can supply dual-frequency currents through the load coil.

6 Output power control and overall efficiency

In the experimental setup, instead of actual gear, an equivalent inductance L_1 is used. Equivalent resistances of the load at LF and HF, that is, R_2 and R_1 are obtained with discrete non-inductive resistors.

In the proposed dual-frequency inverter, power control is achieved through phase modulation and asymmetric duty cycle control. The normalised LF inverter output voltage (i.e. LF inverter gain) is plotted in Fig. 7*a* with varying phase shift angle of LF leg devices at $D_h = 0.9$. The HF inverter gain with varying duty cycle D_h is shown in Fig. 7*b* for $D_l = 0.9$. These characteristics show the control over LF and HF components of output voltages. The LF output voltage V_{01} is a quasi-square wave of LF. Hence at maximum duty cycle (minimum phase shift) the maximum gain of LF inverter ($V_{01,\ rms}/V_{DC}$) is 0.9. The HF output voltage V_{02} contains both LF and HF components. Hence the maximum gain ($V_{02,\ rms}/V_{DC}$) for HF component is 0.45. The variation of LF resonant circuit gain ($V_{R2,\ rms}/V_{01,\ rms}$) with normalised low switching frequency (f_l/f_{rl}) is shown in Fig. 7*c*. Fig. 7*d* shows the variation of HF resonant circuit gain ($V_{R1,\ rms}/V_{02,\ rms}$) with normalised high switching frequency (f_h/f_{rh}). These graphs show the frequency selection nature of the load resonant circuits.

LF and HF output powers are dependent on the corresponding current components. The useful power that generates heat in the gear is calculated as the power dissipation in the equivalent resistances of the gear, that is, $I_{1lf}^2 R_2$ and $I_{1hf}^2 R_1$. I_{1lf} and I_{1hf} are rms values of the fundamental components of LF and HF currents.

LF and HF currents with varying D_l and constant D_h are shown in Fig. 8*a*. It can be observed that while LF current is varying with its duty cycle, HF current remains almost constant. Similarly, Fig. 8*b* shows LF and HF currents with varying D_h and constant D_l. It can be observed that HF current varies with its duty cycle, whereas, LF current remains constant. Hence independent control of LF and HF currents is possible. This is true for any other values of D_l and D_h. Experimental and simulation results shown in these figures are found to be in good agreement with each other.

In order to calculate the power, current in load coil L_1 is measured. This is a combination of both LF and HF components. By performing fast Fourier transform (FFT) analysis of this waveform, fundamental components of low and HF rms currents are obtained. Output powers for LF and HF are calculated as I^2R losses for discrete resistors R_2 and R_1, respectively. Input power is calculated as the product of input voltage and input current. Overall efficiency is calculated from input power and total output power.

Overall efficiency curves of the proposed inverter are shown in Figs. 8*c* and *d*. In Fig. 8*c*, LF output power is varied while HF output power is kept constant. In Fig. 8*d*, HF output power is varied while LF output power is kept constant. It can be observed that the overall efficiency remains considerably high for a wide variation of duty cycle under both situations.

7 Conclusions

Dual-frequency currents are produced in the load coil with the proposed inverter configuration. Experimental results obtained are in good agreement with simulation results. This inverter provides independent control of LF and HF currents through the load coil. Any ratio of LF and HF currents can be obtained by duty cycle variation. FFTs of load currents show that magnitudes of frequency components other than the desired values (30 and 350 kHz) are negligible. The design and control of the proposed circuit are simple. Load resonant circuit parameters can be easily designed for any values of LF and HF. The proposed topology provides high overall efficiency.

8 References

1 Lucía, O., Maussion, P., Dede, J., Burdío, J.M.: 'Induction heating technology and its applications: past developments, current technology, and future challenges', *IEEE Trans. Ind. Electron.*, 2014, **61**, (5), pp. 2509–2520
2 Kifune, H., Hatanaka, Y., Nakaoka, M.: 'Quasi-series-resonant-type soft-switching phase shift modulated inverter', *Proc. Inst. Elect. Eng., Electr. Power Appl.*, 2003, **150**, (6), pp. 725–732
3 Ahmed, N.A., Nakaoka, M.: 'Boost-half-bridge edge resonant soft switching PWM high-frequency inverter for consumer induction heating appliances', *Proc. Inst. Elect. Eng., Electr. Power Appl.*, 2006, **153**, (6), pp. 932–938
4 Ogura, K., Gamage, L., Ahmed, T., *et al.*: 'Performance evaluation of edge-resonant ZVS-PWM high-frequency inverter using trench-gate IGBTs for consumer induction cooking heater', *Proc. Inst. Elect. Eng., Electr. Power Appl.*, 2004, **151**, (5), pp. 563–568
5 Sarnago, H., Lucia, O., Mediano, A., Burdio, J.M.: 'High efficiency parallel quasi-resonant current source inverter featuring SiC MOSFETs for induction heating systems with coupled inductors', *IET Power Electron.*, 2013, **6**, (1), pp. 183–191
6 Fujita, H., Uchida, N., Ozaki, K.: 'A new zone-control induction heating system using multiple inverter units applicable under mutual magnetic coupling conditions', *IEEE Trans. Power Electron.*, 2011, **26**, (7), pp. 2009–2017
7 Pham, H., Fujita, H., Ozaki, K., Uchida, N.: 'Dynamic analysis and control of a zone-control induction heating system'. IEEE Energy Conversion Congress and Exposition (ECCE), 2011, pp. 4093–4100
8 Egalon, J., Caux, S., Maussion, P., Souley, M., Pateau, O.: 'Multiphase system for metal disc induction heating: modeling and RMS current control', *IEEE Trans. Ind. Appl.*, 2012, **48**, (5), pp. 1692–1699
9 Lucía, O., Burdío, J.M., Barragán, L.A., Acero, J., Millán, I.: 'Series-resonant multiinverter for multiple induction heaters', *IEEE Trans. Power Electron.*, 2010, **24**, (11), pp. 2860–2868
10 Lucía, O., Burdío, J.M., Barragán, L.A., Acero, J., Carretero, C.: 'Series resonant multi-inverter with discontinuous-mode control for improved light-load operation', *IEEE Trans. Ind. Electron.*, 2011, **58**, (11), pp. 5163–5171
11 Carretero, C., Lucia, O., Acero, J., Alonso, R., Burdio, J.M.: 'Frequency-dependent modeling of domestic induction heating systems using numerical methods for accurate time-domain simulation', *IET Power Electron.*, 2012, **5**, (8), pp. 1291–1297
12 Wojda, R.P., Kazimierczuk, M.K.: 'Winding resistance of litz-wire and multi-strand inductors', *IET Power Electron.*, 2012, **5**, (2), pp. 257–268
13 Schwenk, W.R.: 'Simultaneous dual-frequency induction hardening'. Heat Treating Progress, April 2003, vol. 3, pp. 35–38
14 Biasutti, F., Krause, C., Lupi, S.: 'Induction hardening of complex geometry and geared parts'. Heat Processing, 2012, vol. 3, pp. 60–70
15 Hammond, M.: 'Simultaneous dual-frequency gear hardening'. Induction Heat Treating, June 7, 2001
16 Schwenk: 'Surface hardening using the simultaneous dual frequency method'. Metallurgia, 2003, pp. 8–9
17 Rudnev, V.: 'Recent inventions and innovations in induction hardening of gear and gear-like components' (American Gear Manufacturers Association, 2012)
18 Okudaira, S., Matsuse, K.: 'Power control of an adjustable frequency quasi-resonant inverter for dual frequency induction heating'. Proc. of IPEMC-2000, S-34-2, 2000, pp. 968–973
19 Okudaira, S., Matsuse, K.: 'Adjustable frequency quasi-resonant inverter circuits having short-circuit switch across resonant capacitor', *IEEE Trans. Power Electron.*, 2008, **23**, (4), pp. 1830–1838
20 Ishimaru, Y., Oka, K., Sasou, K., Matsuse, K., Tsukahara, M.: 'Dual high frequency quasi-resonant inverter circuit by using power MOSFET for induction heating'. IPEMC-2009, 2009, pp. 2545–2550
21 Okudaira, S., Matsuse, K.: 'A new quasi-resonant inverter with two-way short-circuit switch across a resonant capacitor'. PCC-Osaka 2002, 2002, pp. 1496–1501
22 Okudaira, S., Matsuse, K.: 'Dual frequency output quasi-resonant inverter for induction heating', *Trans. Inst. Electric. Eng. Jpn. D*, 2001, **121-D**, (5), pp. 563–568
23 Esteve, V., Pardo, J., Jordan, J., Dede, E.J., Sanchis-Kilders, E., Maset, E.: 'High power resonant inverter with simultaneous dual-frequency output'. Proc. 36th Annual IEEE (PESC'05), 2005, pp. 1278–1281
24 Esteve, V., Jordan, J., Dede, E.J., Sanchis-Kilders, E., Maset, E.: 'Induction heating inverter with simultaneous dual frequency output'. Proc. of Applied Power Electronics Conf. and Exposition, March 2006, pp. 1505–1509
25 Diong, B., Corzine, K., Basireddy, S., Lu, S.: 'Multilevel inverters based dual-frequency power supply', *IEEE Power Electron. Lett.*, 2003, **1**, (4), pp. 115–119
26 Diong, B., Basireddy, S., Corzine, K., Familiant, Y.: 'Multilevel inverters with equal or unequal sources for dual-frequency induction heating'. Proc. 19th Annual IEEE (APEC'04), 2004, vol. 2, pp. 825–831
27 Porpandiselvi, S., Vishwanathan, N.: 'Inverter configuration for simultaneous dual frequency induction hardening with independent control', *Eur. Power Electron. Drives J.*, 2013, **23**, (1), pp. 13–20
28 Burdio, J.M., Barragan, L.A., Monterde, F., Navarro, D., Acero, J.: 'Asymmetrical voltage cancellation for full bridge series resonant inverters', *IEEE Trans. Power Electron.*, 2004, **19**, (2), pp. 461–469