# Optimized Dual Active Bridge Bi-Directional DC-DC Converter for UPS Application

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***Abstract*— With the growing emphasis on smaller compact and efficient power system there is increasing interest in the possibility of using Bi-directional converters especially in DC based power applications. Having the capability of bilateral power flow, that provides the functionality of two uni-directional converters in single converter unit; Bidirectional converters have the increased industrial applications; demand optimized study of topologies and feasibility, critical feature study for the considered application. This document suggests an optimized implementation of Bidirectional DC-DC converter to fit the present day UPS application. Key issues like compact design, utilisation of transformer core, optimised topology for low power (2.5kW) applications were discussed.**

**Keywords— Bi-directional DAB converter, UPS applications**

## I. INTRODUCTION

Power electronic circuits primarily process the energy supplied by a source to match the form required by the load, by means of using semi conductor devices to control the voltage and current. The energy is usually available from the utility grid or from a bank of batteries with the applications ranging from high-power conversion equipment processing megawatts to everyday low power equipment with requirement of a few milliwatts. The majority of power converters are unidirectional with the power being supplied from the source to the load. But a number of applications require the additional exchange of energy from the load to the source. One of the applications where the Bidirectional power flow is an especially attractive proposition and the weight and physical size of the power processing modules are a critical aspect of design will be the UPS applications. Most designs follow the unidirectional dc-dc controller methodology because of topological changes and associated operating principles involved in the two power flow directions. Thus, two independent controllers are needed for battery charging and discharging respectively.

For these UPS applications, Bidirectional DC-DC converters are employed as a link between low voltage battery and high voltage DC bus. Batteries of low voltage are preferred because of the reliability, cost and availability factors. Whereas half bridge inverters to be connected to the bus voltage demands high voltages to generate 230V ac output. Hence bidirectional converters with high voltage gains are gaining importance. This very requirement invoked the institution of transformer into the DC-DC converter [1-2], with involvement of stages of inversion and rectification. From all the state-of-art topologies [7], the single-phase Dual Active Bridge topology (DAB) is considered most promising with respect to the achievable converter efficiency [2] and the achievable power density (due to the low number of inductors and due to the employed capacitive filters on the HV side and on the LV side [5], i.e. the DC capacitor $C_{DC2}$ is used instead of the DC inductor $L_{DC2}$). Therefore, the DAB is considered as the base circuit for the present application with further modifications. With the increase in number of electronic applications output power requirements of UPS are also on an extension. While the charging power capabilities are limited by the charging current, life constraints of batteries. This mismatch or variation in intended power flow for both directions (involving transformer) impose a fine design issues of improper core utilization, compelled usage of over-rated device, un-optimized losses.

## II. PROPOSED TOPOLOGY

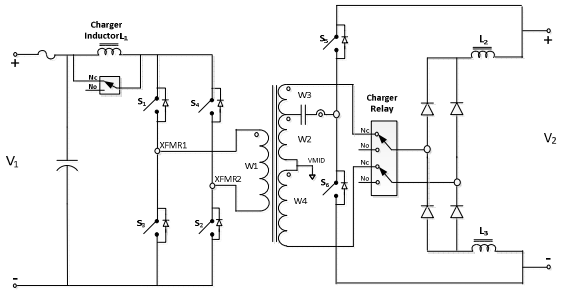


Fig.1 Proposed Topology

The proposed topology is as show in Fig.1 It consist of full bridge at LV side formed by switches with body diodes, Whereas on HV side both the windings are connected in series aiding and then to HV DC bus through diode rectifier bridge circuit for the forward direction (discharge direction). And for the reverse direction (charging direction), HV port is connected to the only a part of transformer through controlled half bridge circuit. Inductors are provided at output port, for directions, suggesting voltage source input and current source output. Terminals of HV port are connected to two individual buses (+400V, -400V reference to the ground connected to the interconnection of $W_2$ and $W_3$) maintained by two separate

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boost converters external to the present DC-DC system. In the half bridge implementation, a situation may arise where average volt-seconds applied to the winding for all the positive going pulse is not equal to that of all the negative going pulses, causing runaway saturation of the transformer core. This case is more likely in our case where the two buses are power by two independent converters. A DC blocking capacitor ($C_2$) in series to the transformer winding has been suggested in [4]. As per the indexed problem (in the previous section) of inefficient transformer design due to difference in power transfer requirements, transformer is provided with tapping to enable different turn's ratio for both direction. Depending on the direction of flow, HV side connections are altered with a control operated relay.

## III. OPERATION

### *A. Reverse or charging direction*

For the reverse direction operation all the relays are connected NO terminal, $V_2$ port powered while $V_1$ is connected to the battery terminals. Switch $S_5$ is trigged at $t_0$, applying $V_2$ voltage across $W_2$, transformer forward biases diodes $D_1$ and $D_2$ and inductor $L_1$ energises at a rate of $(V_{W1}-V_1)/L_1$. At $t_2$, pulse for the $S_3$ is removed; transformer leakage tries to keep the current $i_{C1}$ from sudden falling to zero charging the negative terminal through $D_6$. Even negative voltage is applied to $W_2$ due to negative current slope from $D_1$ and $D_2$ still remain in conduction. This mode of operation exists only for minuscule period of time.

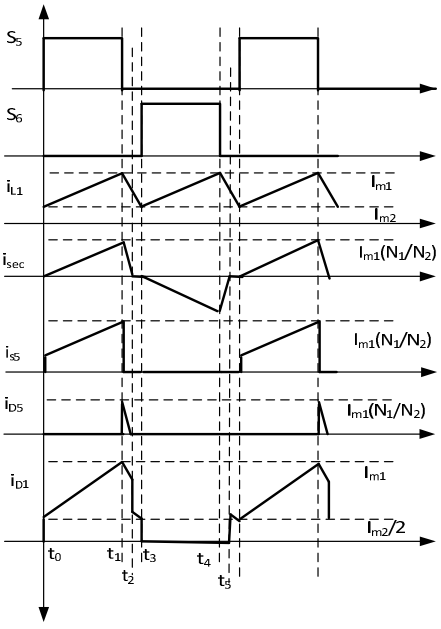



Fig.2 Waveforms of operation-Charging

By the time $t_2$, leakage inductance is completely de-energized; transformer current dies down and $L_1$ starts driving all the diodes to conduction. As soon as $S_6$ is triggered at $t_3$, negative voltage $V_2$ is impressed on $W_2$, in this case diodes $D_1$ and $D_2$ are reverse biased and current through them is forced to transfer entirely to $D_3$, $D_4$. During this transfer whatever the reverse recovery current of $D_1$ or$D_2$ is flows through $D_3$ or $D_4$ and transformer in the direction adding to actual current. After the duty of $S_6$ is completed, at $t_4$ gate pulse is removed and $D_5$ comes to conduction and the cycle of operation repeats. Waveforms and operating modes in reverse or charging direction are show in Fig.2 and Fig.3.

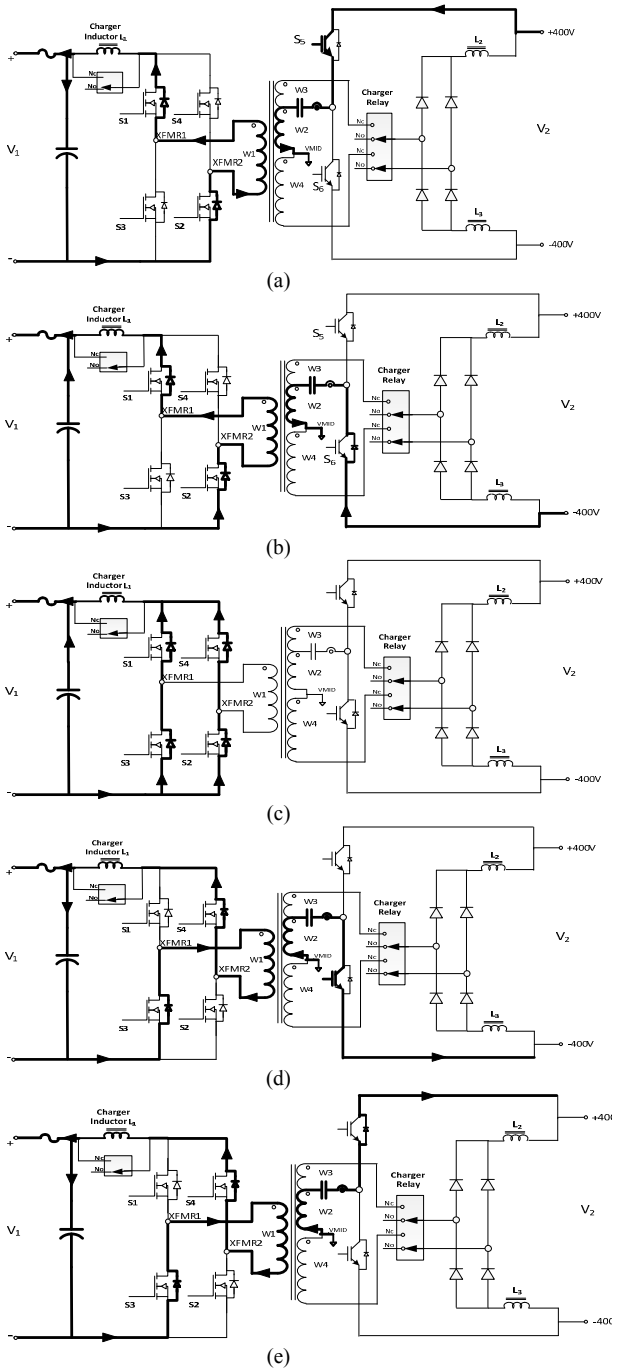



Fig.3 operating modes of reverse or charging direction
(a) Mode1: $t_0<t<t_1$, (b) Mode2: $t_1<t<t_2$,(c) Mode3: $t_2<t<t_3$, (d) Mode4: $t_3<t<t_4$, (e) Mode5: $t_4<t<t_5$

*B. Forward dicharge direction*

During the forward direction of power flow, all the relays are connected to the NC terminals; $L_1$ is bypassed and on the HV side Diode Bridge is connected to the transformer. Whenever switches $S_1$ and $S_2$ are triggered $+V_1$ is impressed on the $W_1$; $D_7$ and $D_8$ are forward biased, current in $L_2/L_3$ rises with a slope of $V_2/L_2$. At $t_1$, pulse for the $S_1$ and $S_2$ are removed; $L_2/L_3$ forces the current to fall with negative slope making $D_3$ and $D_4$ to conduct. Waveforms and operating modes in forward or discharge direction are shown in Fig.4 and Fig.5.

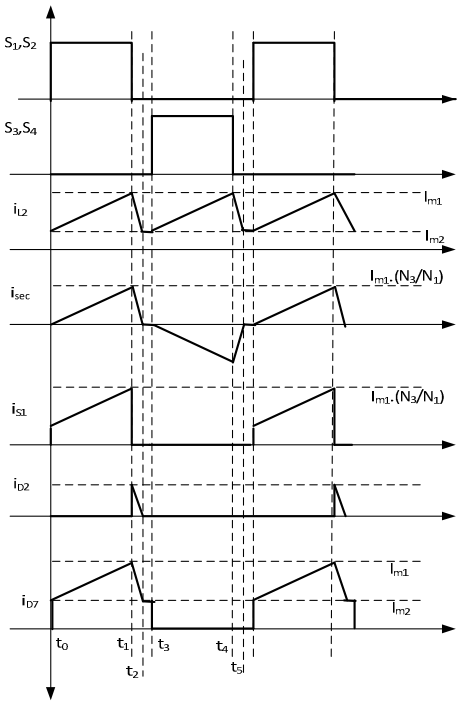
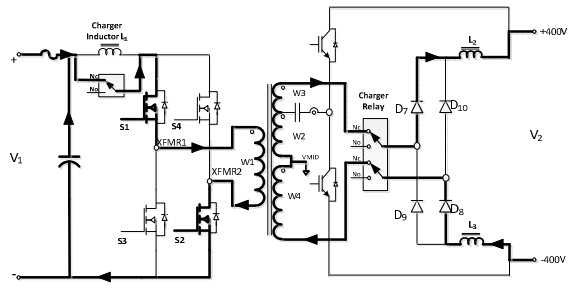
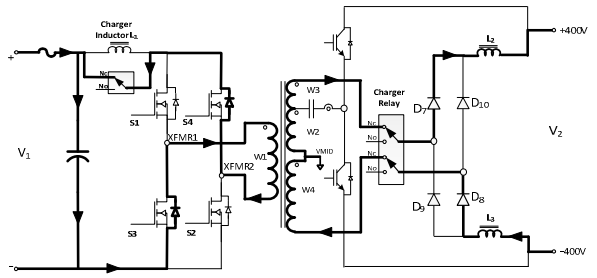



Fig.4 Waveforms of operation-Discharge

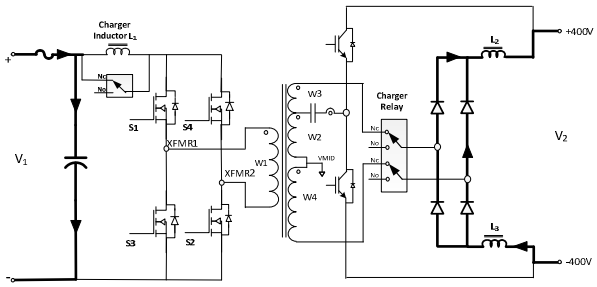
Even though Zero voltage switching for $S_3$, $S_4$ is made available, non zero transformer current, opposes the current reversal. During this period capacitor $C_2$ starts charging. During the period $t_2$ to $t_3$, $i_{sec}$ or $i_{pri}$ lies at zero, meanwhile load current is free wheeled and $C_1$ continues charging. No sooner $S_3$ and $S_4$ are triggered, reverse currents flow through the transformer; energy in the inductors $L_2$, $L_3$ starts building through $D_9$, $D_{10}$. Gate pulse is removed at $t_4$, $D_1$ and $D_2$ starts conducting until $i_{sec}$ or $i_{pri}$ dies to zero.



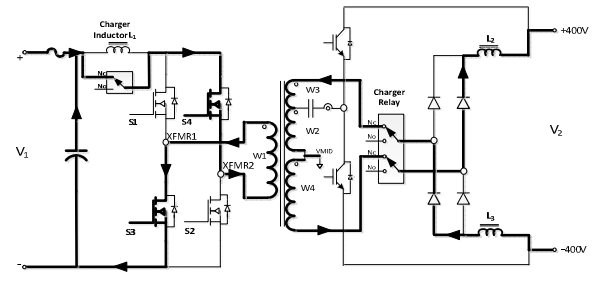

(a)



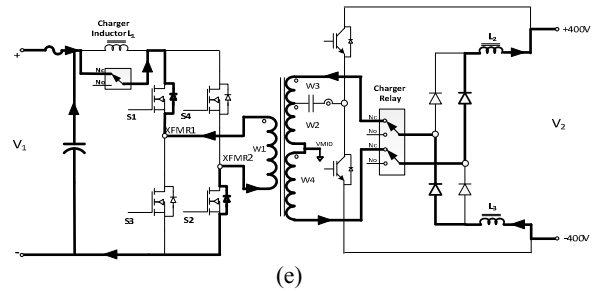

(b)




(c)




(d)




(e)

Fig.5 operating modes of forward or discharging direction (a) Mode1: $t_0<t<t_1$, (b) Mode2: $t_1<t<t_2$, (c) Mode3: $t_2<t<t_3$, (d) Mode4: $t_3<t<t_4$, (e) Mode5: $t_4<t<t_5$

*C. Gain of the converter*

The gain of the converter will be the product of turns ratio and operating duty of the bridge circuit.

The output voltage for the forward direction $V_2$

$$V_2 = \left[V_1 * \frac{N_4}{N_1} * (D_f)\right] \quad (3.1)$$

Where $D_f$ is operating duty of the full bridge circuit.

$$V_1 = \left[V_2 * \frac{N_3}{N_1} * (D_r)\right] \quad (3.2)$$

Where $D_r$ is operating duty of the HV side half bridge circuit.

Leakage inductance effect is omitted in the above equation. Gain decreases with leakage inductance because

negative voltage period is applied for a due period reducing the magnitude output voltage. However capacitor $C_2$ gain has no effect of leakage inductance.

### *D. Voltage stresses*

Voltage stresses across the switches $S_5$ and $S_6$ are $2V_2$ as during the mode 2 of reverse operation both the bus voltages were blocked the single switch. Even though voltage on the LV side is limited to battery voltage (72V) due to high stress during the recovery period of diode, high breakdown voltage switches are preferred. Switching frequency is fixed to 40 kHz owing to limitation of IGBT switches on the HV side.

### *E. Inductors*

For the charging purpose discontinuous mode avoided to avert the ringing while switch is turning ON.
The minimum inductances for avoiding DCM are

$$L_{1,min} = \frac{\left(V_2 * \frac{2N_1}{N_2} - V_1\right) * duty_{max}}{2F_{sw} * 2I_{bat}} \quad (3.3)$$

$$L_{2,min} = \frac{\left(V_2 - 2V_1 \frac{N_2}{N_1}\right) * duty_{max}}{2F_{sw}} \quad (3.4)$$

### *F. Switching losses*

MOSFET on the LV side are hard switched and loss is estimated with the test data from the data sheets. Approximated formula for the switch OFF and ON losses are

$$\frac{V_1}{2} * I_{S1_{on}} * T_r * \frac{V_1}{V_{Test}} * F_{sw} + \frac{V_1}{2} * I_{S1_{off}} * T_f * \frac{V_1}{V_{Test}} * F_{sw} \quad (3.5)$$

Where $T_r$ and $T_f$ are the current rise and fall time from the test data at test condition $V_{Test}$.

In case of reverse direction, IGBT losses are estimated from the loss graphs given. Whereas MOSFET body diodes having high requirement of reverse recovery charge results in considerable contribution to the total losses.
Reverse recovery for D1 is $\frac{V_2}{n} * Q_{rr} * F_{sw}$ in which $Q_{rr}$ is recovery charge given in data sheet.

## IV. SIMULATION RESULTS

TABLE I
PARAMETERS USED FOR THE SIMULATION

| Parameter | Value |
|---|---|
| Battery voltage $V_1$ | 72V |
| Bus Voltage $V_2$ | 400V |
| Charging power $P_{reverse}$ | 1000W |
| Switching Frequency $F_{sw}$ | 40kHz |
| Blocking Capacitor $C_2$ | 1pF |
| Filter Capacitor $C_1$ | 1200uF |
| Inductor $L_1$ | 16uH |
| Turns ratio $N_2/N_1$ | 20/5 |
| Leakage $L_{leakage}$ | 1uH |

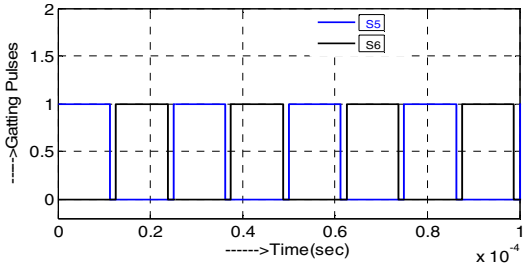


Fig.6 Gating pulses for the switches S5 and S6

Voltage across the switches may experience spikes and specifically need snubber design or over rated switches. Capacitor C1 charges during the current zero period or mode 3 of operation.

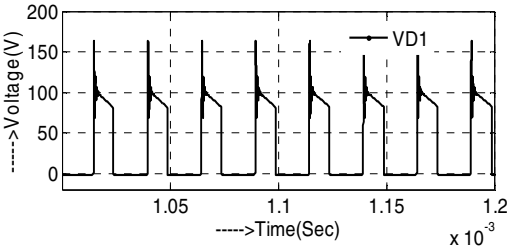


Fig.7 Voltage stresses across LV side switches.

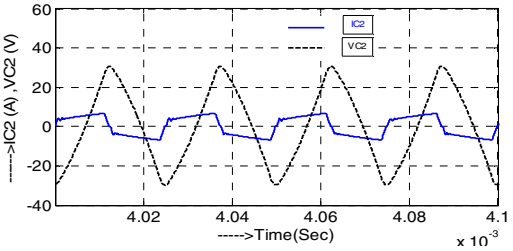


Fig.8 Voltage and current of the capacitor C2

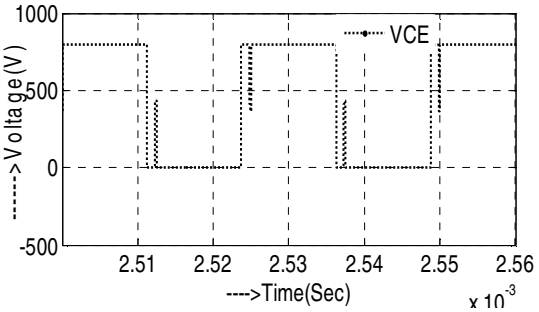


Fig.9 Voltage across switches S5/S6

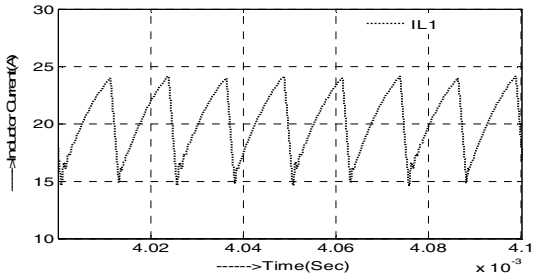


Fig.10 Inductor ($L_1$) current

## V. HARDWARE IMPLEMENTATION

The control logic is implemented with the DSP processor TMS320F28027. Programming of these modules is executed with the interface 'Code Composers Studio$^{TM}$'. Sample code for the generation of pulses of duty ratio 0.25

```
EPwm1Regs.TBCTL.bit.CTRMODE=TB_COUNT_UPDOWN;
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm1Regs.TBCTR = 0x0000;                  // Clear counter
EPwm1Regs.TBPRD = 1000;
EPwm1Regs.CMPB = 750;
EPwm1Regs.AQCTLA.bit.CBU = 1        // Set PWM1A on event B, up count
EPwm1Regs.AQCTLA.bit.CBD = 0;       // Set PWM1A on event B, down count
```

QCPL-3120 gate drive with opto-coupler is used for the $S_5$ and $S_6$ IGBTs. Gate resistances used are 20 ohm for turn on process and 10 ohm for turn off process.

TABLE III
COMPONENTS USED FOR THE IMPLEMENTATION

| Parameter | Value |
|---|---|
| $L_m$ | 200uH |
| $L_{lk}$ | 1uH |
| $L_1$ | 24uH |
| Inductor Core | 0077935A7 |
| $N_1$ | 5turns |
| $N_2$ | 9turns |
| $N_3$ | 20turns |
| $N_4$ | 29turns |
| Transformer Core | EE65/32/22 |
| $C_1$ | 1pF |
| $C_2$ | 1200uF |
| $S_5$ ,$S_6$ | IRG7PH42UDPbF |
| $S_1$, $S_2$, $S_3$, $S_4$ | IRFB4127PbF |

The power circuit is tested in laboratory with the battery pack of specified parameters as LV port of the converter and positive and negative bus of 400V as HV port. HV port is maintained by capacitor of 400uF and grounds are interconnected. Flyback converter with output voltage of 12V is connected to the control board to power up the processor and other sensors. The waveforms are captured from the oscilloscope and the results are shown in the following section.

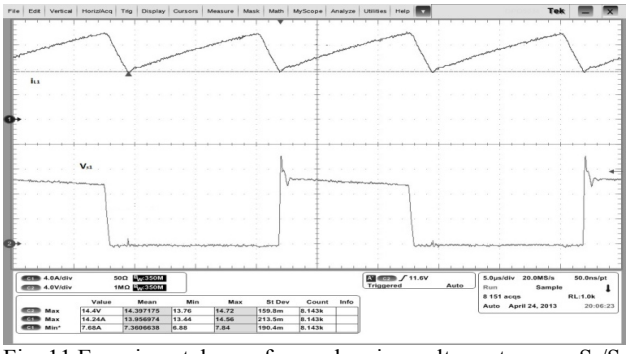


Fig. 11 Experimental waveforms showing voltage stress on $S_1$/$S_3$

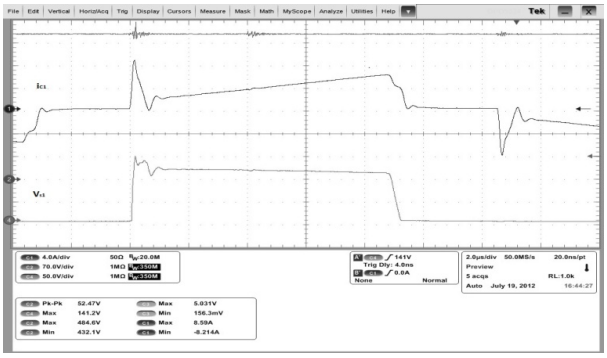


Fig. 12 Experimental waveform showing current spike in the transformer current

Inductor ripple oscillated from 7.3A to 13.9A at an battery current of 11.17A. Voltage spike across the switch S1 is 144V while it is rated to 200V. Currents in the transformer are having spike at the switching due to diode D1/D3 turn off involves reverse recovery current to flow through the transformer and hence introducing spike in the transformer currents. Leakage is having the least effect on the switch voltage and the stress levels are at 400V.

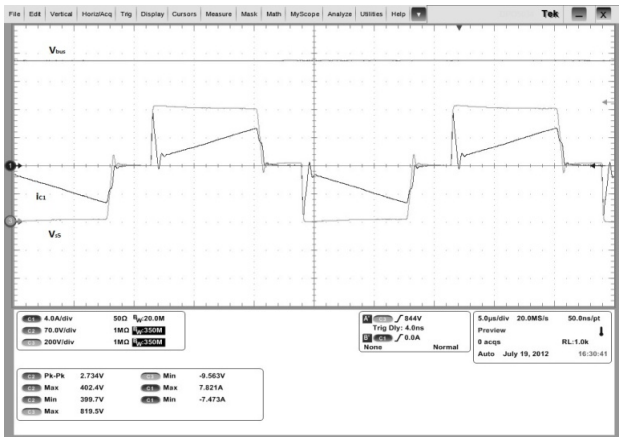


Fig. 13 Experimental waveform showing voltage stress on the switches $S_4$/$S_6$

## VI. CONCLUSION

In this paper, Bi-directional DC–DC converter with a low voltage/high current port is investigated. The construction of the LV side full bridge is challenging with respect to low conduction losses and low switching losses; furthermore, the LV side DC capacitor $C_1$ is subject to large RMS currents and the calculation of applicable modulation parameters (D1, D2, and ˜ ) is considerably complex. These difficulties are avoided with the full bridge converter topologies [7] with one or more DC inductors on the LV side: the DC inductors reduce the RMS current through the DC capacitor ($C_1$). Due to the large volume of the filter inductors ($L_2$ or $L_3$), the achievable power density is considered to be less. In future more efforts are needed to implement combined control logic for both directional flow and smooth mode transition without causing large current or voltage stress on device.

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