A Novel Four Level Cascaded Z-Source Inverter

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***Abstract*—This paper presents a novel four-level cascaded Z-source inverter based on space vector pulse width modulation (SVPWM) technique. The proposed model provides high gain output voltage compared to the conventional four-level inverter and wide range of control using SVPWM. This effectively utilizes the DC sources for varying modulation index while synthesizing output voltage with lower harmonic distortion and high gain. Besides, it alleviates the voltage balancing problem and lower components count compared to NPC and cascaded multilevel inverters. The proposed model finds application in industrial, domestic and automobile sectors. To validate the theoretical concept, the proposed model is developed in MATLAB/Simulink environment and the results are presented and compared with the conventional four level inverter.**

***Keywords*—Voltage gain, Cascade multilevel inverter, Space vector modulation (SVM), Z-source Inverter, Total harmonic distortion (THD)**

I. INTRODUCTION

Recently Z-source converter based multilevel inverter getting more popularity for industrial, electric vehicle, PV cell, fuel cell based power generation etc., due to the advantages of higher boost gain without the need of additional circuits compared to traditional voltage source and current source inverters. The traditional converters produce lower output voltage than the input and always operated in buck mode which requires a bulky high gain low frequency transformer. In order to produce the required output voltage and to reduce current stresses across the inverter a DC-DC boost converter stage is introduced between the input DC source and Inverter as shown in Fig.1. However, the two stage conversion produces lower efficiency due to increased components, system cost has the limitations of boosting capability due to inductor saturation problems. Hence, F.Z. Peng [1] developed a high gain zig-zag connected Z-source converter using inductors and capacitors to boost the input DC voltage. It provides immune to EMI and shoot-through or mis-gating problem unlike traditional inverters.

The Z-source converter is applied for various conversion operations such as ac-to-dc, dc-to-ac, ac-to-ac, two-level and multilevel inverters explored by various researchers are available in the literature [2-5]. This concept is also applied for multilevel inverter with reduced number of switches [6]. The different control algorithms of simple boost control, maximum boost control, and constant boost maximum control is discussed and compared for Z-source operation [7]. All the above said systems are developed based on components counts, complex control, reduced inductor ripple currents, lower %THD etc.. For example increasing in level requires more

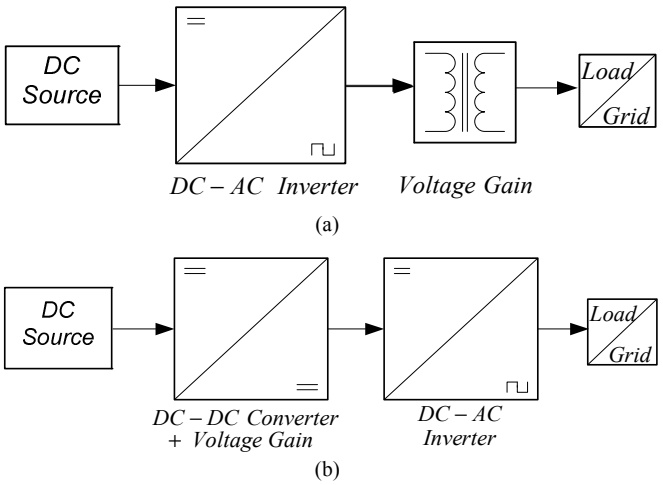

Fig. 1. Power Supply System (a) Single-Stage (b) Multi-Stage.

number of components and difficulties in implementation of control algorithm. Each topology has its own merits and demerits and can be used based on its adaptability to particular applications. The merits of the multilevel inverter with z-source network and that of without it is ability to synthesize output voltage to required range and effective utilization of DC sources with less complex circuitry. The main reason behind choosing cascaded topological multi-level inverter is the source utilization minimization w.r.t to the operating modulation index and reduced stress on switches of non-operating inverter level, which can't be obtained in other type of multi-level topologies. Moreover, Z-source network has been applied to many other multi-level topologies like diode-clamped, flying capacitor, cascaded H-bridge inverter topologies and cascaded inverter topologies but in only in cases where the number of levels is odd.

Therefore, in this paper, a novel cascaded four-level Z-source inverter is proposed with the objective of high voltage gain and better control. The modified structure of the proposed four level inverter with Z-source inverter is developed in MATLAB/Simulink environment and the control signals are generated using state vector pulse width modulation (SVPWM) with shoot-through technique. The insertion of shoot through states is applied between active and zero states as in a traditional simple boost control. The developed model is analyzed for various modulations index. In addition, the performance of the proposed cascaded four-level inverter is compared with and without Z-source converter.

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II. PROPOSEDTOPOLOGY

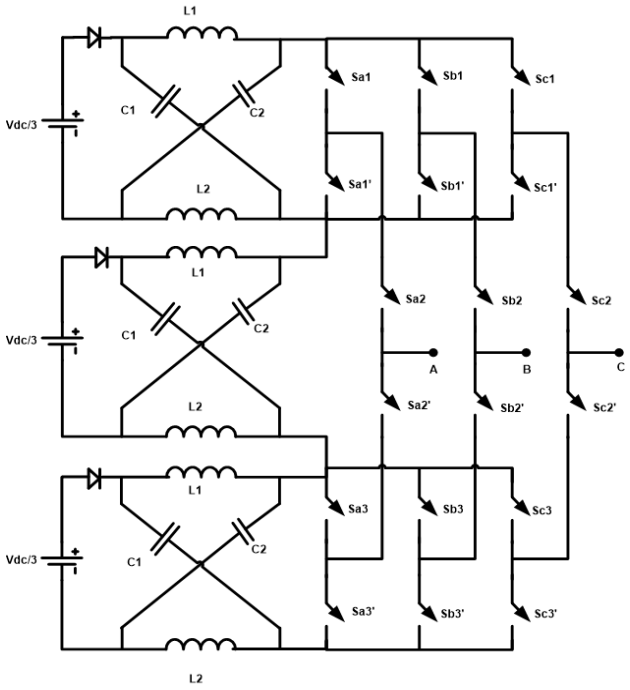

Fig. 2. Proposed four-level cascaded Z-source inverter.

Multi-level inversion can be achieved by retrofitting existing two-level inverters with a cascaded connection. In general, (n+1) distinct voltage levels can be produced by employing 'n' equal DC-links and two-level inverters with this connection. The number of voltage levels at the output of a multi-level inverter can be further increased by introducing unequal DC sources. Fig. 2 shows a proposed four-level z-source inverter topology by cascading three two-level inverters. In this topology there are total of eighteen switches with six switches for each phase and two of them are for legs in a two-level inverter. The top and the bottom two-level inverters are fed with a DC voltage where are the middle inverter legs are connected between the pole points of the upper and lower two-level inverters. In order to produce the desirable output voltage a high gain Z-source converter is cascaded between the dc source and inverter to acquire any required voltage independent of the input voltage. The boosting technique of conventional two-level three leg inverter is explained in [8]. The equivalent circuit of Z-source inverter during shoot through state and active state are given Fig.3 (a) & (b).

The input voltage, dc link voltage and z-source output voltage expressions during shoot through state and active states are;

$V_L=V_C$; $V_d=2V_C$; $V_i=0$ *(1)*

$V_L=V_0-V_C$; $V_d=V_0$; $V_i=Vc-V_L=2V_C-V_0$ *(2)*

Applying volt second balance of inductor

$$V_L=\frac{T_0 v_C+T_1(v_0-v_C)}{T}=0;\quad \frac{v_C}{v_0}=\frac{T_1}{T_1-T_0} \qquad (3)$$

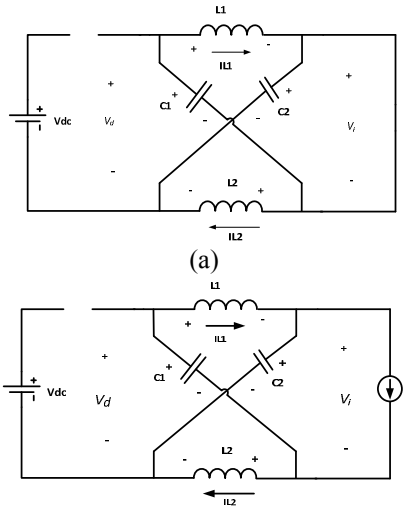

Fig 3. Equivalent circuit of Z-source inverter during (a) Shoot through state and (b) Active state

and average DC link across inverter is

$$v_i=\frac{T_0.0+T_1(2v_C-v_0)}{T}=\frac{T_1}{T_1-T_0}.v_0=v_C \qquad (4)$$

Peak dc link voltage across inverter is

$$v_i=v_{C-}v_l=2(v_C-v_0)=\frac{T_1}{T_1-T_0}.v_0=B.v_0 \qquad (5)$$

Where

$$B=\frac{T_1}{T_1-T_0}.=\frac{1}{1-2\frac{T_0}{T_1}}\geq 1 \qquad (6)$$

B is the boosting factor

Output peak phase voltage is expressed as

$$B.\frac{v_i}{2} \qquad v_{ac}=M.B.\frac{v_i}{2} \qquad (7)$$

This topology is free from capacitor voltage balancing issues and it does not require any clamping diodes like NPC inverter and doesn't have capacitor precharging issues. The advantages in this topology is that less voltage stress on the switches as the no. of voltage levels increases, although it requires more no of switches when compared to lower levels but the voltage rating required will be less. With increase in number of levels in multilevel inverters the synthesized voltage waveform approaches to near sinusoidal which makes it produce waveform with low harmonic distortion. The salient features of the proposed topology are:

- Obtain required output voltage without additional circuitry
- Obtained without much change in THD
- Immune to mis-gating
- Less expensive when compared to conventional two state power conversion.

III. CONTROL SCHEME

In any modular system only the implementation of suitable control scheme will give better quality of supply. The three main categories of modulation schemes available in the literature for multilevel output voltage are (i) Fundamental frequency switching, (ii) Space vector PWM and (iii) Sinusoidal PWM. Among these, the popular schemes for industrial applications are SVPWM and SPWM techniques. However SVPWM is the most popular scheme compared to SPWM as it gives 15% more DC bus utilization. Of the two types of SVPWM techniques kim-sul algorithm [9,10] is chosen besides conventional SVPWM technique as it does not depend on the magnitude of reference voltage space vector and its relative angle w.r.t reference axis and also the technique is implemented based on the instantaneous values of reference voltages. The imaginary switching time periods proportional to the instantaneous values of reference phase voltages are defined as;

$$T_{as} = \left(\frac{T_s}{V_{dc}}\right) va^*;\ T_{bs} = \left(\frac{T_s}{V_{dc}}\right) vb^*;\ T_{cs} = \left(\frac{T_s}{V_{dc}}\right) vc^* \qquad (8)$$

From which the maximum and minimum of the imaginary switching time periods at every sample time calculated based on the following expressions;

$$T_{max} = max\ (T_{as},\ T_{bs},\ T_{cs})\ and\ T_{min} = min\ (T_{as},\ T_{bs},\ T_{cs}) \qquad (9)$$

The effective time period is calculated as

$$T_{eff} = T_{max} - T_{min} \qquad (10)$$

The offset time period that has to be added for each imaginary switching time period to make it a center spaced pwm technique

$$T_{offset} = T_0/2 - T_{min} \qquad (11)$$

Where

$$T_0 = (T_s - T_{eff}) \qquad (12)$$

Which gives actual switching times for each inverter leg as

$$T_{ga} = T_{as} + T_{offset};\quad T_{gb} = T_{bs} + T_{offset};\quad T_{gc} = T_{cs} + T_{offset} \qquad (13)$$

The modulating waves that are produced using the above technique are compared with the three carriers of equal magnitude placed one over the other.

A) Shoot through state insertion

The technique uses for implementing shoot through state using inserting shoot through state between active and zero state in alternate manner as shown in Fig. 4. In this technique a maximum and minimum of the modulating waves at every sample time has to be calculated and then an offset is given to a required level at the top and bottom of two level inverters and then compared with the respective carrier waves. The relational pulse has to be added to the corresponding phase leg switch which has the maximum and minimum modulating wave at particular sample time. Then according to this shoot through will occur in one phase leg per inverter at a time. The middle inverter is free from the shoot through level comparison.

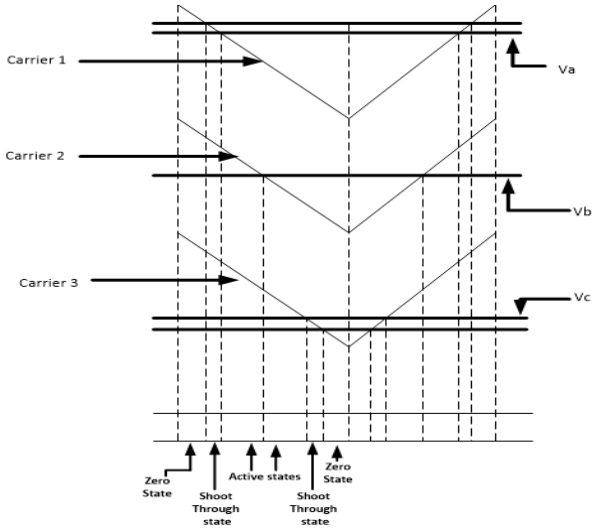

Fig. 4 Shoot through state insertion technique.

Table I gives an exhaustive idea of the different switching states along with the shoot through state that has to be implemented when using a Z-source inverter. The shoot through state can be implemented in seven different ways in a two-level inverter. But the proposed model consists of three two-level inverters so the possible number of combinations can be expressed as *7^N* where *N* is the total number of two-level inverters presents in the module. However, any one type of shoot through technique can be implemented at a time which results three ways for two-level inverter at any instant. Therefore, only 9 combinations are possible for the proposed topology.

TABLE I SWITCHING STATES OF FOUR LEVEL CASCADED Z-SOURCE INVERTER

Pole Voltage ***(V_{A0})***	**State of switch**					
	Sa1	**Sa1'**	**Sa2**	**Sa2'**	**Sa3**	**Sa3'**
Vdc	ON	OFF	ON	OFF	OFF	OFF
2Vdc/3	OFF	ON	ON	OFF	OFF	OFF
Vdc/3	OFF	OFF	OFF	ON	ON	OFF
0	OFF	OFF	OFF	ON	OFF	ON
Shoot through	ON	ON	OFF	OFF	OFF	OFF
Shoot through	OFF	OFF	ON	ON	OFF	OFF
Shoot through	OFF	OFF	OFF	OFF	ON	ON

The above Table I gives the states of the switching devices of A-phase operation. To obtain maximum output voltage V_{dc} the switches SX1 and SX2 should be turned on and the complimentary action for the switches SX1' & SX2'and SX3 & SX3' states are negligible. The switches SX2 and SX1' are to be turned on and the complimentary action for SX1 and SX2' to obtain a voltage range of 2Vdc/3 and similarly the switching state of SX3 and SX3' are negligible in this case. Similarly to obtain a voltage range of Vdc/3 the switches SX2' and SX3 are turned on and the complimentary are given to SX2 and SX3', in this case switch state of SX1, SX1' are negligible. At last to obtain a voltage range of 0 SX2' and SX3' are turned

on and the complimentary are given to SX2, SX3. Here the X represents the switching states of a, b and c phases.

IV. Simulation Results

To verify the concept and for validation of the simulation results, the proposed topology and the generation of control signals using SVPWM with shoot through states is developed in MATLAB/Simulink environment. The values of passive components, operating voltage level and switching frequency considered for the simulation study are given in Table II. The simulation work is carried for the shoot through duty ratio of T_0/T =0.04. The generated control pulses for the upper, middle and bottom switches of inverter leg-A are given in Fig. 5. The simulated line voltage, phase voltage, pole voltage and line currents for different modulations index of 0.8, 0.5 and 0.2 are given in Figs. 6-8. From these results it is observed that the proposed model is operated in different output voltages of four-level, three-level and two-level for the corresponding modulation index of 0.8, 0.5 and 0.2 respectively. The THD of the line current supplied by the four level Z-source inverter is better compared to two-level and three level operations and also %THD output voltage waveform with and without z-source four level cascaded inverter is given in Fig. 9(a)&(b). From the above results, it is evident that the harmonic profile is almost equal and output voltage of Z-source converter is higher compared to the conventional four-level cascaded inverter. Moreover, Table III shows the comparison of output voltage and %THD for different modulation values of four-level cascaded inverter with and without Z-source inverter.

TABLE II SPECIFICATIONS OF THE INDUCTOR AND CAPACITOR VALUES USED DURING SIMULATION

Parameters	Values
DC voltage	V_{dc}=400V
Inductor (L)	10mH
Capacitor (C)	300µF
RL-Load	185 Ω, 15mH
Frequency	2.4kHz

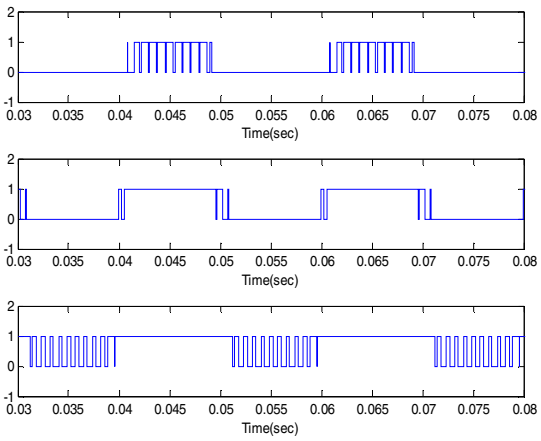

Fig. 5. Switching pulses for upper, middle and lower devices of inverter leg A respectively.

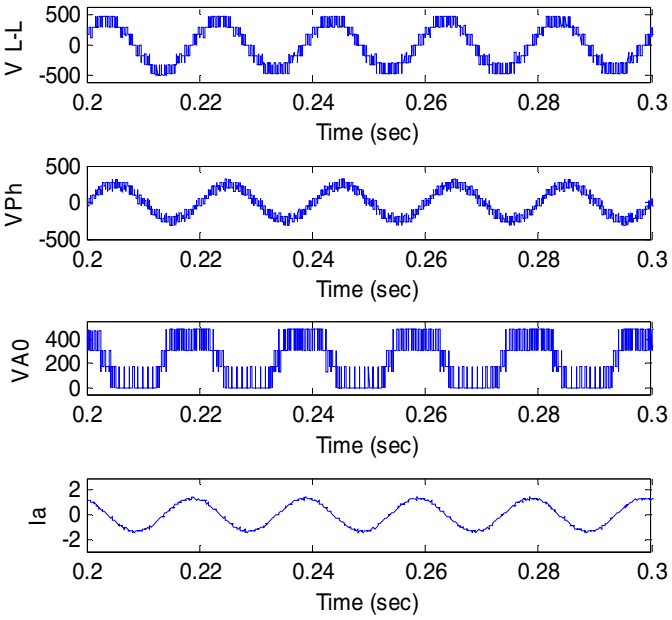

Fig. 6. Line voltage, phase voltage, pole voltage and line current for RL load for ma of 0.8.

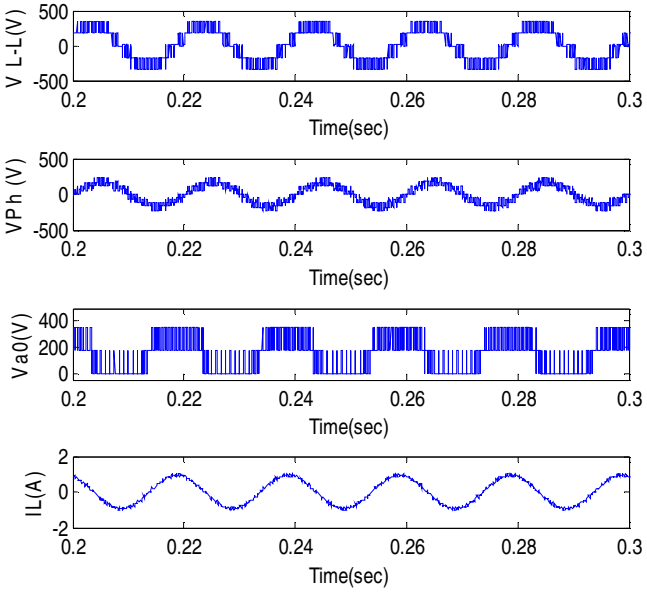

Fig. 7. Line voltage, phase voltage, pole voltage and line current for RL load for ma of 0.5.

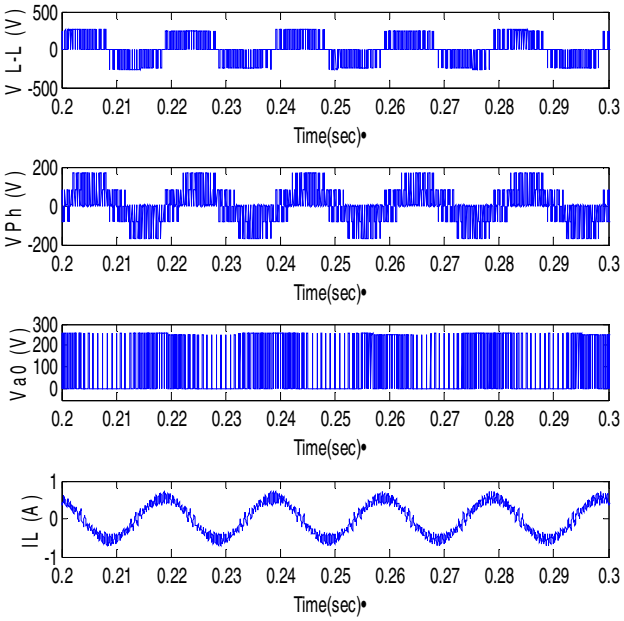

Fig. 8. Line voltage, phase voltage, pole voltage and line current for RL load for ma of 0.2.

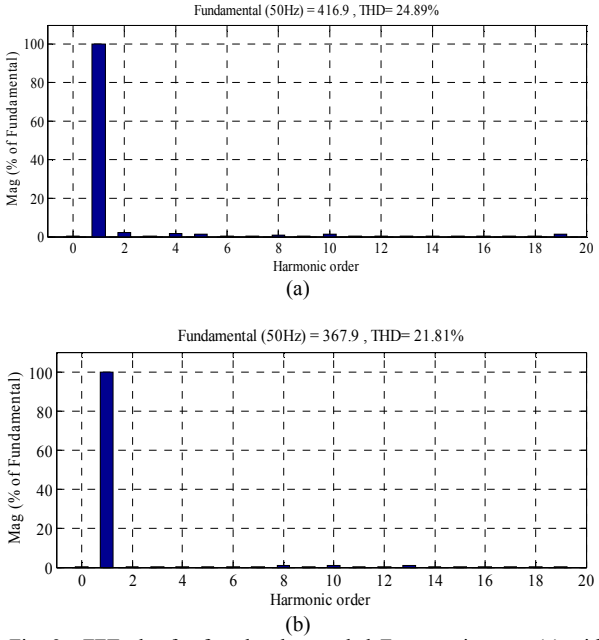

Fig. 9. FFT plot for four level cascaded Z-source inverter (a) with Z-source network and (b) without Z-source network

TABLE III COMPARISON OF MODULATION WITH LINE VOLTAGES AND %THD FOR CASCADED FOUR-LEVEL INVERTER WITH AND WITHOUT Z-SOURCE NETWORK

ma	Four level cascaded Z-source inverter			Four level cascaded inverter		
	%THD	***RMS***	***PEAK***	***%THD***	***RMS***	***PEAK***
0.8	24.79	293	401.98	21.78	260.8	368.8
0.7	27.10	251.4	351.43	24.48	228.3	322.8
0.6	34.22	211.1	300.6	25.58	195.6	276.7

V. CONCLUSION

In this paper a new topology of four level cascaded Z-source inverter is presented. The operation and control signals generated using SVPWM with shoot through states inserted between actives and zero states have been presented. The proposed model is simulated in MATLAB environment and their results have been presented for different modulation index. The four-level cascaded Z-source inverter gives higher output voltage gain compared to conventional four-level cascaded inverter with similar harmonic distortion and with less complex circuitry and control logic. The simulation results reveal the validity of theoretical concepts and can be implemented for various applications.

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