A New Low Cost and High Efficiency Cascaded Half-Bridge Multilevel Inverter with Reduced Number of Switches

[1]Venu sonti
Department of Electrical Engineering
NIT Warangal
Warangal-506 004, INDIA
Email: venu312@nitw.ac.in

[2]Sachin Jain
Department of Electrical Engineering
NIT Warangal
Warangal-506 004, INDIA
Email: jsachin@nitw.ac.in

[3]Vivek Agarwal
Department of Electrical Engineering
IIT Bombay
Mumbai - 400 076, INDIA
Email: agarwal@ee.iitb.ac.in

***Abstract*— This paper presents a new low cost and efficient cascaded multilevel inverter (MLI) configuration. The proposed MLI requires less number of switching devices and isolated power supplies compared to the basic MLIs. It eliminates the problem of neutral point fluctuations, DC offset current, diode reverse recovery problem etc. as observed in conventional NPC and Flying capacitor configurations. Further, the given MLI also has the advantage of low conduction and switching losses. Thus, the proposed MLI has the advantages of low cost and better efficiency. This paper also gives the generalised version of proposed configuration for (2m+1) levels. All the details regarding circuit schematic, modes of operation and simulation results are presented in this paper.**

Keywords*— *Cascaded multilevel inverter, conduction and switching losses, efficiency.

I. INTRODUCTION

Multilevel Inverter (MLI) topologies [1]-[8] are popular for their applications in medium and high voltage drives. Also, these topologies are finding their applications in renewable energy system applications [9]-[14]. Thus, with the increasing applications, demand with respect to low cost, high performance and higher reliability in multilevel inverters is escalating. It has increased the research for different configurations of multilevel inverter using basic diode clamped, flying capacitor and cascaded H-bridge configurations. This has also led to the development of highly efficient multilevel inverter configuration.

The configuration proposed by Ruiz-Caballero *et.al.* [15] reduces the switching losses by using four switches operating at fundamental cycle of the output voltage. Another, recent proposals based on cascaded multilevel inverters was given by E.Babaei *et.al.* [16] - [19]. In the given proposals, authors have used cascaded H-bridge with series/ parallel connection of DC sources. However proposal [16] based on cascaded H bridge inverter configuration requires reduced number of switches and isolated input DC sources. The given configuration has the advantage of reduced number of switching devices with low conduction losses as compared to conventional configurations. The authors have also given the generalized configuration for the proposed MLI configuration.

This paper presents a new generalized cascaded hybrid MLI configuration. The topology can be used in both symmetric and asymmetric operations. The proposed configuration have the advantages of low conduction and switching losses with reduced number of switches. The manuscript is divided into five sections. Section II gives the details of circuit schematic with its two modes of operation. Section III describes the generalised configuration for the proposed MLI. Section IV deals with comparison of proposed MLI with the various existing MLIs and Section V gives the details of simulation results obtained using MATLAB.

II. OPERATION OF THE PROPOSED MLI

Circuit schematic for the proposed nine level MLI configuration for symmetrical operation is given in Fig. 1. The given topology consists of ten switches and four isolated power supplies. The pair of switches in each leg (S1, S2), (S3, S4), (S5, S6) and (S7, S8) are operated in complimentary mode with high frequency and the switches S9 and S10 are operated at fundamental frequency of the reference voltage or at low frequency. Thus, these switches have negligible switching loss. Further, switches S1 (S5) and S2 (S6) are used to connect the total or half of the total input voltage respectively to terminal A (N) through switch S3 (S7). Other switches S3 (S7), S4 (S8) and S9 (S10) are operated to give basic three levels at the output i.e. +V(-V) and 0. Further, as only five switches are conducting in a given state, proposed configuration also have the advantage of lower conduction losses compared to configuration given by E.Babaei et.al [16].

In all, the proposed MLI is the low cost solution with higher efficiency and performance. Further, the proposed configuration can be used for symmetrical and asymmetrical operation. Details of symmetrical and asymmetrical operation is discussed in the next sub- section.

A. Proposed MLI in symmetrical operation

In symmetrical MLI topology, the value of all the DC voltage sources are taken or considered as equal For example V_1, V_2, V_3 and V_4 are four DC voltage sources then for symmetrical configuration

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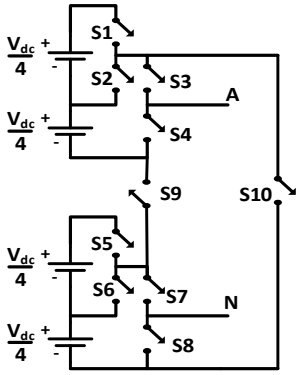

Fig. 1 Proposed cascaded multilevel inverter configuration with reduced switches.

$$V_1 = V_2 = V_3 = V_4 = \frac{V_{dc}}{4} \quad (1)$$

Equal value of DC voltages limits the number of levels of the proposed configuration. There are nine levels in the output voltage for the symmetrical topology. Output phase voltage attains the value $+V_{dc}$, if switches S1, S3, S5, S8, S9 are turned ON. Fig. 2 shows the operation of the symmetrical multilevel inverter topology for phase voltage levels of $+V_{dc}$, 0 and $-V_{dc}$ and table I gives the details of the switching states and their respective voltage levels for the proposed topology in symmetrical operation.

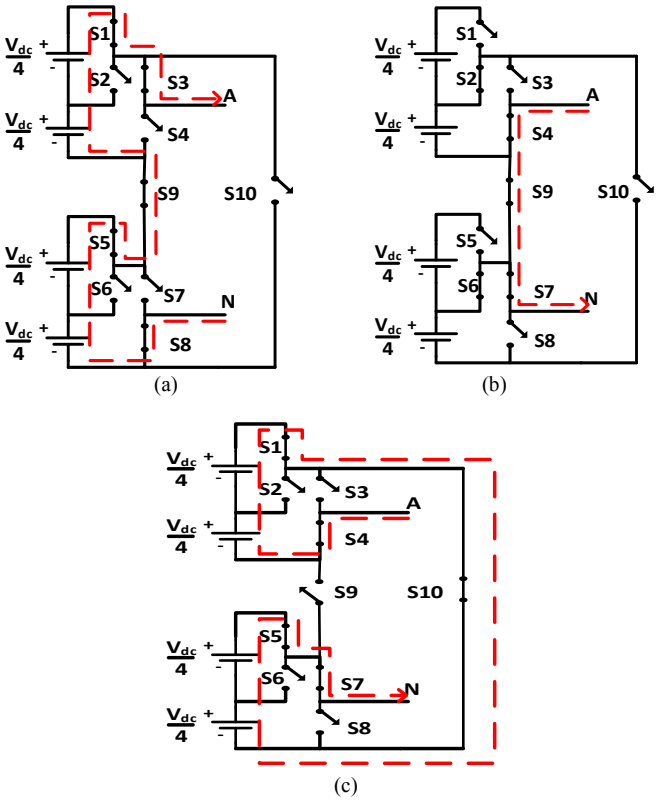

Fig. 2 Operation of proposed cascaded multilevel inverter in symmetrical configuration for phase voltage levels (a) + V_{dc} (b) 0 (c) -V_{dc}.

TABLE I. SWITCHING STATES AND THEIR RESPECTIVE VOLTAGE LEVELS IN SYMMETRICAL OPERATION.

S1	*S3*	*S5*	*S7*	*S9*	*Phase Voltage Level*
1	1	1	0	1	$+V_{dc}$
0	1	1	0	1	$+3/4\ V_{dc}$
0	1	0	0	1	$+1/2\ V_{dc}$
0	1	0	1	1	$+1/4\ V_{dc}$
0	0	0	1	1	0
0	1	0	0	0	0
0	0	0	0	0	$-1/4\ V_{dc}$
0	0	0	1	0	$-1/2\ V_{dc}$
0	0	1	1	0	$-3/4\ V_{dc}$
1	0	1	1	0	$-V_{dc}$

B. Proposed MLI in symmetrical operation

In asymmetrical multilevel inverter topology, the values of all the DC voltage sources are not necessary to be equal. For example, for asymmetrical configuration the voltage values of DC sources can be taken as

$$V_1 = V_2 = \frac{V_{dc}}{3} \text{ and } V_3 = V_4 = \frac{V_{dc}}{6} \quad (2)$$

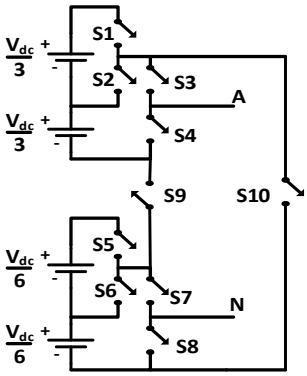

Fig. 3 Proposed thirteen level cascaded multilevel inverter in asymmetrical operation.

Fig. 3 shows the proposed asymmetrical multilevel inverter topology for thirteen levels. The phase voltage attains the value $+5/6\ V_{dc}$, if switches S1, S3, S6, S8, S9 are turned ON. Fig. 4 shows the operation of the asymmetrical multilevel inverter topology for output phase voltage levels of $+5/6\ V_{dc}$, 0 and $-5/6\ V_{dc}$. To summarize all possible voltage levels with their details of the switching states are given in table II for the proposed topology in asymmetrical operation.

III. GENERALISED CONFIGUARTION OF PROPOSED MLI FOR SYMMETRICAL OPERATION

The proposed configuration can be extended to 2m+1 levels by cascading the individual two level inverters where m is the number of DC sources used in topology. The value of m is an even number and its starts from m=2. Fig. 5 shows the generalised configuration of proposed MLI for symmetrical operation.

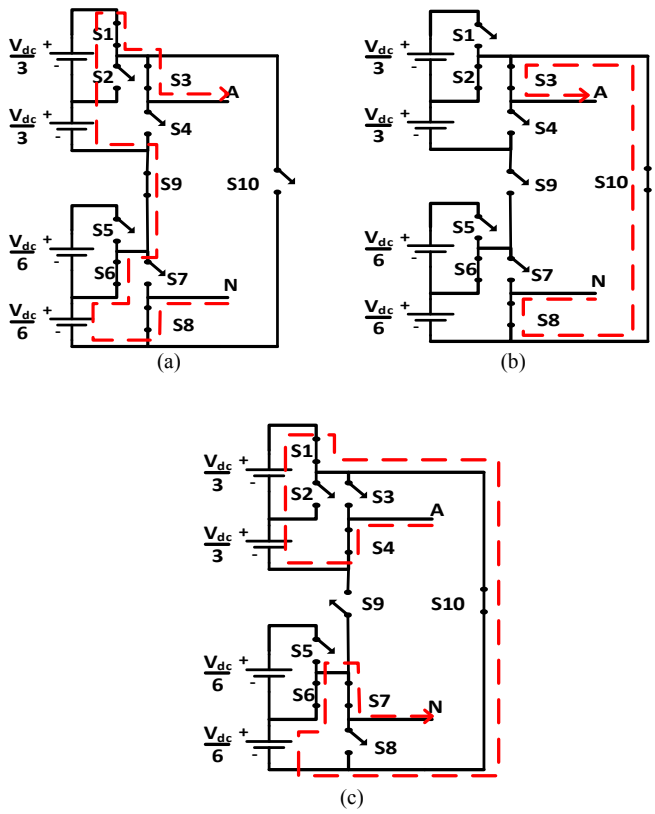

Fig. 4 Operation of proposed cascaded multilevel inverter in asymmetrical configuration for phase voltage levels (a) + $5/6V_{dc}$ (b) 0 (c) $-5/6V_{dc}$.

TABLE II. SWITCHING STATES AND THEIR RESPECTIVE VOLTAGE LEVELS IN ASYMMETRICAL OPERATION.

S1	*S3*	*S5*	*S7*	*S9*	*Phase Voltage Level*
1	1	1	0	1	$+V_{dc}$
1	1	0	0	1	$+5/6\ V_{dc}$
1	1	0	1	1	$+4/6\ V_{dc}$
0	1	0	0	1	$+3/6\ V_{dc}$
0	0	1	0	1	$+2/6\ V_{dc}$
0	0	0	0	1	$+1/6\ V_{dc}$
0	0	0	0	1	0
0	1	0	0	0	0
0	1	0	0	0	$-1/6\ V_{dc}$
0	1	1	1	0	$-2/6\ V_{dc}$
0	0	0	0	0	$-3/6\ V_{dc}$
0	0	1	1	0	$-4/6\ V_{dc}$
1	0	0	0	0	$-5/6\ V_{dc}$
1	0	1	1	0	$-V_{dc}$

The expression for output voltage V_{AN} is given by

$$V_{AN}=(V_1S_1+V_2S_3+.....V_{m/2}S_{m-1}+.....V_m\overline{S_{2m-1}})S_{2m+1}-(V_1S_1+V_2S_3+.....V_{m/2}\overline{S_{m-1}}+.....V_mS_{2m-1})\overline{S_{2m+1}} \quad (3)$$

where V_1, V_2,…..V_m are the magnitudes of DC voltage sources used and S_1, S_3,……..S_{2m+1} are the switches whose value is equal to 1 if switch is closed else equal to 0.

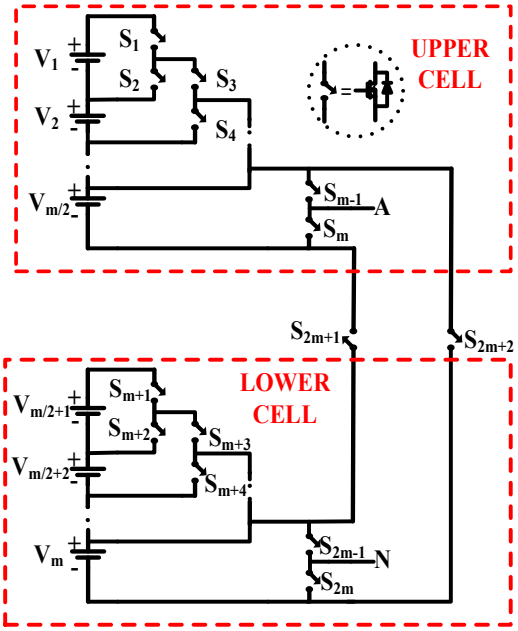

Fig. 5 Proposed cascaded multilevel inverter with reduced switches.

The expression for the number of switches used in proposed MLI for (2m+1) levels is given by

$$N_{switch}=2(m+1) \quad (4)$$

As there are (m+1) pairs of complementary switches so the number of switches conducting are always half of the total number of switches used in the configuration.

The expression for number of switches conducting in the MLI is given by

$$N_{conducting}=m+1 \quad (5)$$

The blocking voltage V_{Block} for switches used in the topology are given in the "(6)" to "(8)"

For the low frequency switches S_{2m+1} and S_{2m+2}

$$V_{Block}=\sum_{k=1}^{m}V_k \quad (6)$$

Blocking voltage of upper cell switches S_e and S_{e-1} is given by

$$V_{Block}=\sum_{k=1}^{e/2}V_k \quad (7)$$

Where e=2, 4, ..m/2

Similarly, the blocking voltage of lower cell switches S_{2e} and S_{2e-1} is given

$$V_{Block}=\sum_{k=e/2+1}^{e}V_k \quad (8)$$

Where e=m/2+2,m/2+4,…m.

IV. COMPARISION OF PROPOSED MLI WITH THE EXISTING TOPOLOGIES

The proposed MLI is compared with the various existing MLIs with respect to power devices count, switches conducting etc. Fig.6 shows the number of voltage levels versus number of switches for different inverter topologies in the symmetrical operation.

For a thirteen level inverter, the number of switches used are fourteen which is very less when compared to the other MLIs where the number of switches used are 24 in case conventional MLIs and eighteen in case configuration proposed by E.Babaei *et.al* [16]. The proposed configuration eliminates the requirement of clamping diodes, balancing capacitors which are used in basic MLI.

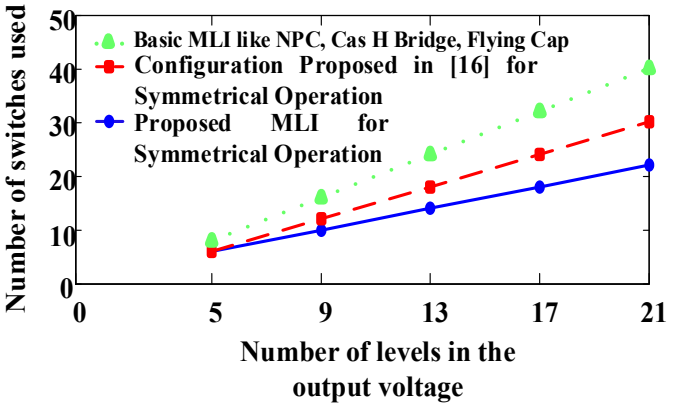

Fig. 6 Comparison of number of switches used in proposed topology with other MLIs.

Fig.7 shows the number of voltage levels versus number of switches for different inverter topologies. For a nine level inverter the number of switches conducting are five. The number of switches conducting in the configuration proposed by E.Babaei *et.al* [16] are six whereas in the other basic nine level MLIs the number of switches conducting are sixteen. Hence the proposed configuration have the advantages of low conduction loss and reduced number of switches.

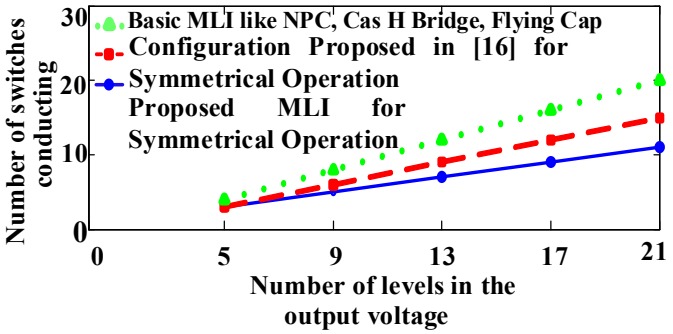

Fig. 7 Comparison of number of switches conducting in proposed topology with other MLIs.

The switches S_{2m+1}, S_{2m+2} are operated at low switching frequency i.e. at the frequency of reference wave. So the configuration have less switching losses when compared to configuration proposed by E.Babaei *et.al* [16]. Fig.8 shows the number of levels in the output versus number of switches used for proposed inverter and cascaded H bridge in asymmetrical operation.

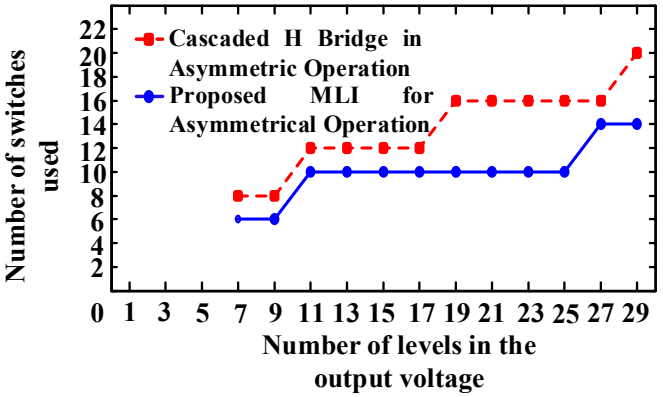

Fig. 8 Comparison of number of switches used in proposed topology with cascaded H bridge in asymmetrical operation.

For a nine level asymmetrical inverter, the number of switches used are six which is less when compared to the nine level asymmetrical cascaded H bridge inverter with eight switches. The maximum number of levels in the output voltage during the asymmetrical operation of proposed inverter is given by

$$N_{level} = (h+1)^2 \quad (9)$$

where h is equal to number of H bridges used in the topology.

Hence the proposed configuration is economical as the number of components used are less and it is efficient because of reduced switching and conduction losses which is observed from the Fig. 6, Fig. 7 and Fig. 8.

V. SIMULATION RESULTS

The simulation was conducted in MATLAB/SIMULINK to verify the operation of proposed cascaded multilevel inverter configuration in symmetrical and asymmetrical mode. The proposed cascaded multilevel inverter is connected to a RL load of value R=100Ω and L=1mH. The switching frequency of inverter is at 10kHZ. The input DC voltage V_{dc} is equal to 100V.

A. Proposed MLI in symmetrical operation

The waveforms shown in Fig. 9 are the phase voltages of proposed inverter for different modulation indices in symmetrical mode. For this configuration in symmetrical operation as the value of 'ma' increases from zero to one the number of levels in the phase voltage increases from three to nine.

The blocking voltage of the switches used in the proposed nine level inverter is shown in Fig. 10. The switches S1, S2, S5 and S6 are rated for one fourth of the total DC bus voltage. The switches S3, S4, S7 and S8 are rated for half of the DC bus voltage. The remaining two switches S11 and S12 are rated for total DC bus voltage.

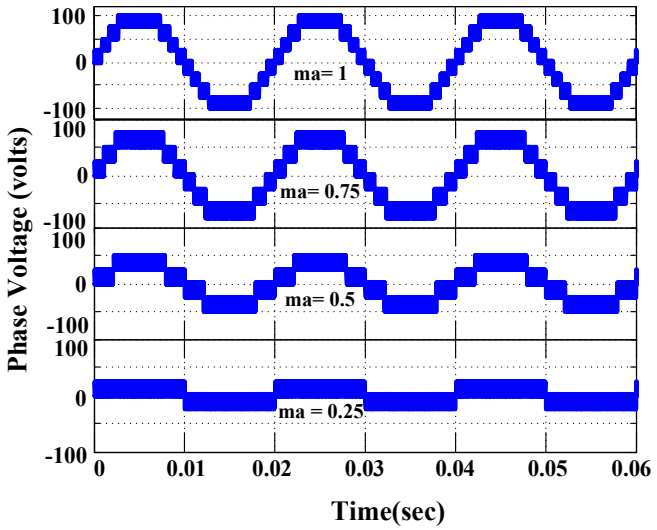

Fig. 9 Phase Voltage waveform for different modulation indices (ma) in symmetrical configuration.

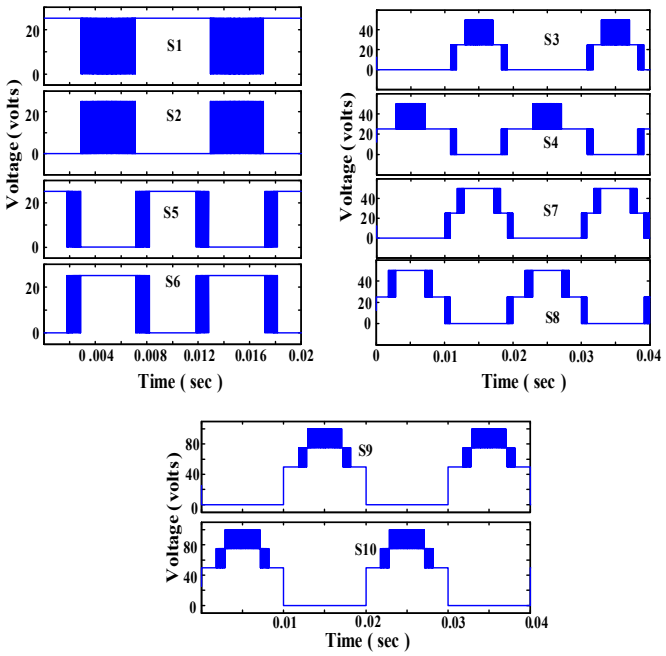

Fig. 10 Blocking Voltage waveforms of the switches in symmetrical configuration.

B. Proposed MLI in asymmetrical operation

Fig. 11 shows the phase voltage waveforms of the proposed inverter for different modulation indices. With the increase of 'ma', the number of levels in the output voltage will increase from three to thirteen in the asymmetrical operation of proposed inverter.

The blocking voltages of all the switches during asymmetrical operation are shown in Fig. 12. As shown in the figure, the switches S5 and S6 are rated for one sixth of the total DC bus voltage, the switches S1, S2, S7 and S8 are rated for one third of total DC bus voltage, the switches S3 and S4 are rated for two thirds of the DC bus voltage and remaining

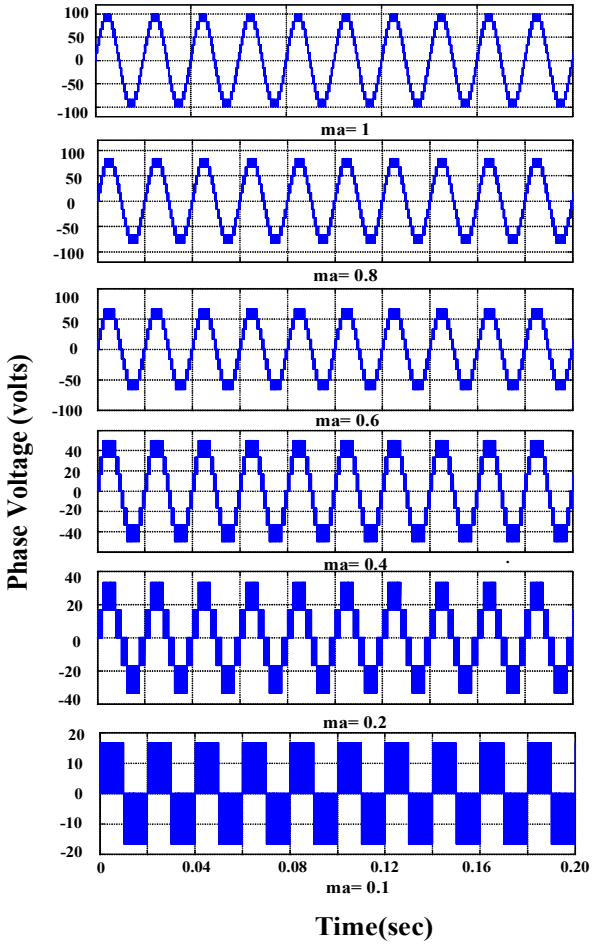

Fig. 11 Phase Voltage waveform for different modulation indices (ma) in asymmetrical configuration.

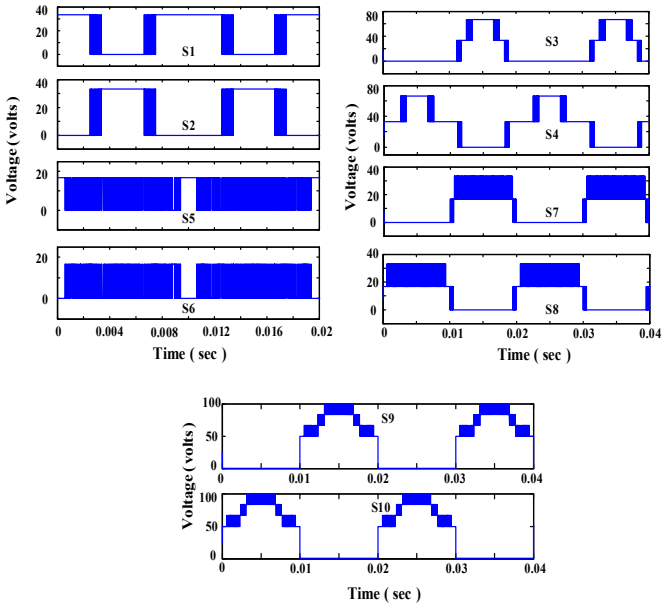

Fig. 12 Blocking Voltage waveforms of switches in asymmetrical configuration.

switches S_{11} and S_{12} are rated for complete DC bus voltage.

VI. CONCLUSION

This paper presents a new generalised cascaded multilevel inverter with reduced number of switches, reduced switching and conduction loss. This proposed configuration can be operated in symmetrical and asymmetrical modes depending on the values of DC voltage source. In the proposed configuration, two switches are operated at low switching frequency so the switching losses are less. From the output results, depending on the value of modulation index the number of levels in the output voltage changes.

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