Hindawi Publishing Corporation
VLSI Design
Volume 2008, Article ID 259281, 7 pages
doi:10.1155/2008/259281

Research Article

A Robust Low-Voltage On-Chip LDO Voltage Regulator in 180 nm

Sreehari Rao Patri and K. S. R. Krishna Prasad

Electronics and Communication Engineering Department, Chip Design Cener, National Institute of Technology, Warangal 506004, India

Correspondence should be addressed to Sreehari Rao Patri, patri_srihari@yahoo.com

Received 10 August 2008; Accepted 23 October 2008

Recommended by Yong-Bin Kim

This paper proposes a capacitor-less LDO with improved steady-state response and reduced transient overshoots and undershoots. The novelty in this approach is that the regulation is improved to a greater extent by the improved error amplifier in addition to improved transient response against five vital process corners. Also entire quiescent current required is kept below 100 μA. This LDO voltage regulator provides a constant 1.2 V output voltage against all load currents from zero to 50 mA with a maximum voltage drop of 200 mV. It is designed and tested using Spectre, targeted to be fabricated on UMC 180 nm.

1. INTRODUCTION

Exponential increase in the usage of the portable hand-held battery-operated devices led the designers to focus on the power management techniques. The low-dropout (LDO) linear regulator is widely used in power management due to its low noise, precision output, and fast transient response. Due to the ever increasing demand for low power consumption, the regulators' specification is to be modified with very low dropout, low quiescent, and fast transient responses. Also "fully integrable system" or "system on chip" has been the most desirable aspect of any design solutions. High current efficiency is one of the major factors as it leads to improvement of battery life. All these factors motivate the designers towards the fully integrable LDO voltage regulators.

Conventional LDOs are inherently unstable at no load currents. A large output capacitor and its equivalent series resistance (ESR) are required to achieve the dominant pole compensation and insert a zero to cancel the nondominant pole. This method has two drawbacks: first, the large off-chip capacitor increases pin count, and it occupies large board space, thus increasing cost. Thus it is not suitable for SOC. Compensation using R_{ESR} is disadvantageous as it varies with temperature, and R_{ESR} does not have wide range of values. The second drawback is that increasing R_{ESR} increases overshoot while decreasing R_{ESR} moves zero to high frequency, decreasing phase margin. Figure 1 illustrates the process.

The capacitor-less LDO [1] as shown in Figure 2, on the other hand, maintains good stability and transient response at low load currents. A fast transient path is required since the system gain bandwidth was relatively low in frequency. This paper concentrates on the design of the regulator with 180 nm as against 0.35 micrometer in [1]. The proposed regulator design not only overcomes the stability issues in migrating from 0.35 micron process to 180 nm, but also improves line regulation and load regulation by improving the error amplifier.

2. DESIGN ISSUES

Major issues involved in the design of LDO voltage regulator are stability and transient response.

2.1. Stability

Presence of multiple poles definitely degrades the stability of any closed loop system. The uncompensated capacitor-less LDO consists of two major poles, namely, one at the

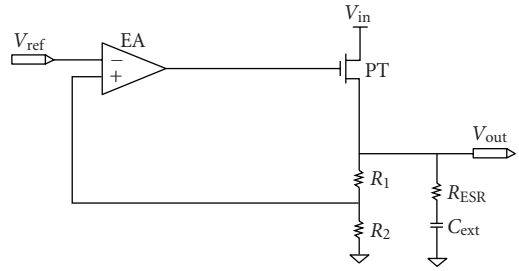


Figure 1: Conventional LDO regulator compensation.

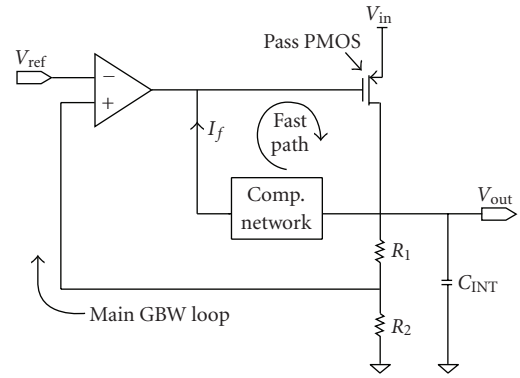


Figure 2: Basic capacitor-less LDO concept.

output of the error amplifier P_1 and the other is the LDO output pole (P_2) which solely depends on the load current. In general, the error amplifier individually has at least one pole at high frequency. The pole at low frequency depends on the output impedance of the error amplifier. The equivalent pass transistor gate to source capacitance along with the C_{GD} which is multiplied by the gain of the pass transistor (miller effect) pulls the error amplifier pole to low frequencies. Thus location of pole P_1 is given by

$$P_1 = \frac{1}{R_1.(C_1 + C_{GS} + A_{\text{pass}}C_{GD})}, \quad (1)$$

where R_1, C_1 are the error amplifier output resistance and capacitance, respectively, and A_{pass} is the gain of the pass transistor. The values of C_{GS} and C_{GD} are in the range of a few tens of picofarads. The value of R_1 is to be chosen to be relatively large to yield large DC gain in order to facilitate better regulation. Though the gain of the pass transistor varies with load current causing the P_1 to vary, it is less sensitive to load current variation when compared to the output pole (P_2). Pass transistor transconductance G_{mp} increases with load current whereas R_{DS} decreases with the same current. This implies that A_{pass} does not change significantly with load current while P_2, which depends mainly on R_{DS}, is very sensitive to load current variations. Therefore, when load current is low, the pole P_2 will be pushed well below the unity gain frequency. Eventually, the capacitor-less LDO tends to be stable at no load condition. In addition, the C_{GD} introduces an RHP zero Z_1 ($= G_{mp}/C_{GD}$). This also degrades stability, since this feed forward zero reduces the phase margin. The RHP zero attracts complex poles to the right-hand side of the S-plane which degrades the loop stability. Hence, RHP zero should be located at high frequencies relative to unity gain frequency. This demands the pole P_1 at the error amplifier output to be made more dominant. This paves the way for the unity gain frequency to be pulled away from the RHP zero.

2.2. Transient response

Transient response consists of two parts: undershoots/overshoots and settling time.

While there is a change in load current demand, error amplifier cannot change the pass transistor gate input voltage quickly due to limited current (power consumption) and large gate capacitance. So the pass transistor cannot supply instantaneously the load current demanded. Had there been a large external capacitor, it would have supplied the demanded current instantaneously that smoothes out the ripple to a major extent. But the on-chip LDO cannot have the luxury of large capacitor. Consequently, output voltage overshoots or dips in response to sudden decrement or increment of load current, respectively.

3. ARCHITECTURE TAILOR-MADE FOR ON-CHIP LDO

The major design issues of the capacitor-less LDO as mentioned in the previous section are as follows. One is to contain the magnitude of overshoots and undershoots. The second one is to improve the regulator's stability. The stability issue is addressed by pushing the pole at the error amplifier output towards the origin. If the error amplifier output impedance is made large, it can be conveniently pushed towards origin. Folded cascode amplifier is proposed to be used as an error amplifier against the conventional two-stage amplifier proposed in [1] for this purpose. Usage of the folded cascode has several benefits. It provides large output resistance for the error amplifier as desired. Also the large gain offered by it improves regulation characteristic. In addition, it also yields better stability relative to multistage (multipole) amplifier. Stabilization is further improved by the usage of the technique [2]. The corresponding architecture is shown in Figure 3.

3.1. Error amplifier design

The proposed architecture employs an optimally designed gain boosting topology for the error amplifier as shown in Figure 4. Requisite gain is deduced from steady state specifications which is evaluated be 70 dB for a line regulation of 0.01%. The transconductance of the driving ransistor g_{m1} is calculated from the gain bandwidth specification which is chosen to be 200 KHz for satisfactory transient response using GBW $= g_{m1}/C_L$, where $C_L = 40$ pF (pass transistor gate capacitance). The output resistance R_{out} is calculated from gain. Bias current for this stage is chosen to be 20 μA. Divide the current in the ratio $I_{DM1} : I_{DM6} = 3 : 1$. Sizes of M_6 and M_7 are calculated from R_{out} and I_{D6}. Sizes of the remaining

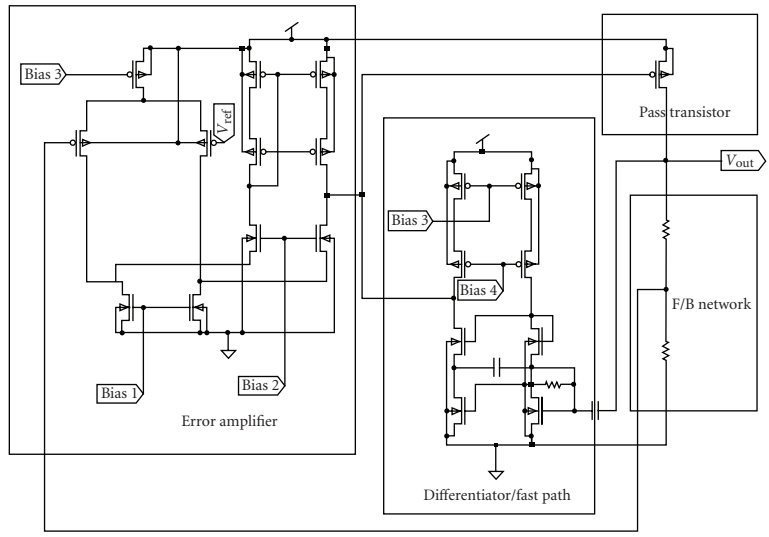


Figure 3: The architecture of the proposed LDO.

Table 1: Salient design parameters.

Design parameters	Error amplifier		Bias circuit	
Transistor sizing (units in microns unless otherwise specified)	M_1: 25/.5	M_7: 4/1	MN1 1/2	MP1 20/1
	M_2: 25/.5	M_8: 15/1	MN2 1/2	MP2 20/1
	M_3: 3.7/1	M_9: 15/1	MN3 1/2	MP3 20/1
	M_4: 3.7/1	M_{10}: 15/1	MN4 2/1	MP4 20/1
	M_5: 100/.5	M_{11}: 15/1	MN5 1/2	MP5 20/1
	M_6: 4/1		MN6 1/2	MP6 20/1
			MN7 1/8.75	MP7 3.1/1
Amplifier gain	70 dB			
GBW	200 KHz			

transistors are calculated to maintain the appropriate biasing currents.

3.2. Pass transistor design

The size of the pass transistor is decided from the dropout voltage by making use of the relation

$$V_{\text{dropout}} = \text{V}_{\text{DSAT}} = \sqrt{\frac{2 \cdot I_{\text{MAX}}}{\mu_p \cdot C_{ox} \cdot (W/L)}}. \quad (2)$$

The dropout voltage is chosen as 200 mV and maximum load current is 50 mA. Substitution of UMC180 nm model parameters yields $W/L = 65,000$.

3.3. Fast path design

A differentiator serving as a fast path [1] is employed (last section of Figure 3) that charges or discharges the gate capacitor of pass transistor along with the error amplifier. This decreases the response time for the pas transistor of LDO to react with load current changes, which in turn reduces the undershoot and overshoot. The capacitor C_F connected between output of LDO and gate of pass transistor serves as a differentiator. The value of C_F can be calculated using

$$C_F = \frac{\Delta I_{\text{load}}}{\Delta V_{\text{out}}} \frac{C_{GS}}{g_{m,\text{pass}}}, \quad (3)$$

with $C_{GS} = 15$ pF, $G_{MP} = 300\,\mu$A/V, $\Delta V_{\text{OUT}} = 100$ mV, $I_{\text{Load}} = 50$ mA, and $C_F = 25$ nF.

The required C_F is apparently large and it moves the RHP zero to lower frequencies which effects stability, since new RHP zero $= G_{MP}/(C_{GD} + C_F)$. This capacitor value is further reduced by making use of a simple auxiliary circuit that consists of simple resistor and an amplifier (G_{mf}). The resistor R_z converts the capacitive current to voltage and the G_{mf} converts this current back to current. It is assumed that the parasitic pole $1/R_Z C_f$ is located at a very high frequency. Thus, this arrangement increases the effect of C_f since the effective C_f is equal to $G_{mf} R_z C_f$. Thus, the required value of C_f can be reduced by the factor of $G_{mf} R_z$ and the feed forward path created by the C_f is eliminated.

3.4. Bandgap reference and biasing circuits

The LDO requires a voltage reference as shock voltage is compared and correction is made accordingly. Hence the

Table 2: Performance measures of the proposed simulated LDO at various process corners.

Process corner	Overshoot mV	Undershoot mV	Settling time (μs)	Line regulation %	Load regulation Ppm/mA
TT	93	86	13.1	.08	32
FF	111	83	12.4	.08	48
SS	80	85	13	.56	32
SNFP	86	82	12.2	.16	32
FNSP	102	89	13.2	.08	16

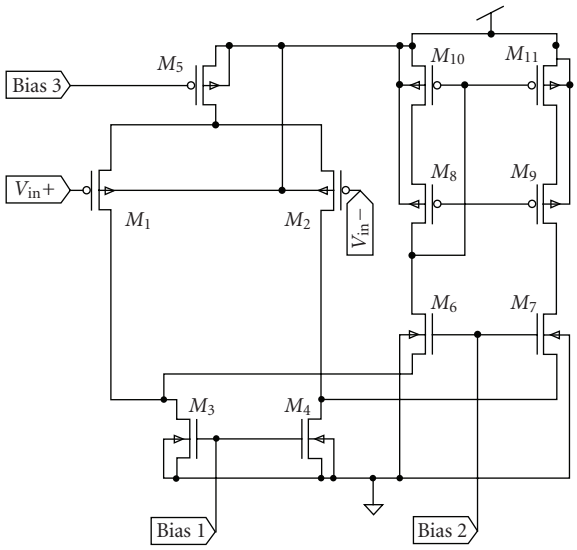


Figure 4: Schematic of error amplifier.

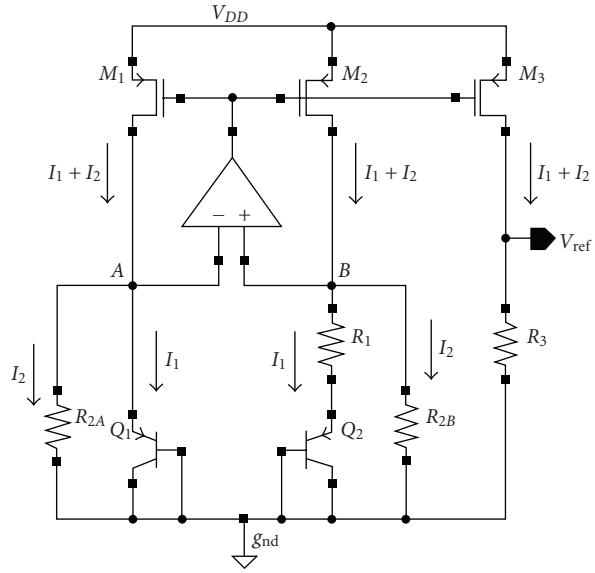


Figure 5: Low-voltage bandgap reference circuit.

voltage reference should be carefully designed to provide a 600 mV constant voltage against process and temperature variations. So a low-voltage BGR is designed with the architecture shown in Figure 5. In this architecture, an op-amp [1] is designed with input common mode range 650 mV which is generated using voltage V_{BE} across diode connected BJTs. The gain bandwidth GBW is chosen to be greater than 1 MHz for this op-amp that keeps the settling time on the order of microsecond(s). The corresponding circuit is shown in Figure 6. In this circuit, $R_{2a} = R_{2a}$ is calculated taking quiescent current into consideration, and then R_{2a}/R_1 ratio is adjusted for making reference voltage less dependent on temperature. The resistor R_3 is scaled to get the required reference voltage. The different bias voltages required for the entire system are obtained from the bias circuit [3] shown in Figure 7 which provides constant required voltages against temperature variations.

The temperature and supply independent constant g_m biasing circuit [3] is designed by taking V_{DSAT} drawn from the dropout voltage specification which is 200 mV and bias current for this section is allocated to be 2.5 μA from power considerations. The various transistor dimensions that yield the requisite bias voltages are chosen as follows.

For PMOS, $(W/L)_{P,i}$ with $i = 1, 2, 3, 4, 5, 6$ are chosen to have identical values while $(W/L)_{P7} < 0.25*(W/L)_{P1}$. Similarly for NMOS, $(W/L)_{N,i}$ with $i = 1, 2, 3, 5, 6$ are chosen

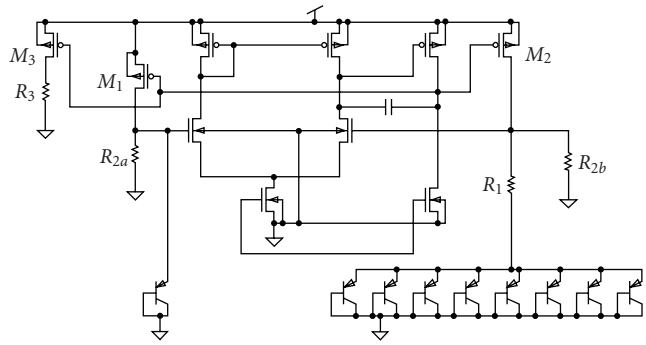


Figure 6: Low-voltage BGR internal op-amp.

to be identical whereas $(W/L)_{N4} = 4*(W/L)_{N1}$, $R_{BIAS} = 1/G_{M1}$, and $(W/L)_{N7} < 0.25*(W/L)_{N1}$. Various salient design parameters are listed in Table 1.

3.5. Layout issues

The proposed LDO is designed using UMC 180 nm twin well process. But it is found that layout versus schematic (LVS) mismatch occurs when both NMOS and PMOS transistors are drawn with the above technology and substrate

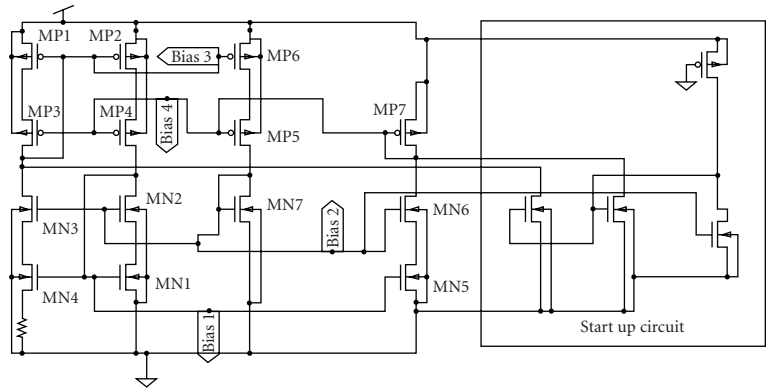


Figure 7: Circuit that generates requisite bias voltages constant against temperature and process variations.

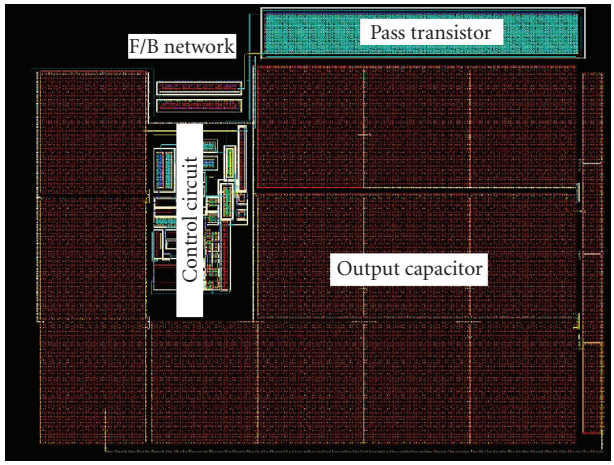


Figure 8: Layout of the proposed LDO.

connection of NMOS is connected to source in order to avoid body bias. Hence triple-well NMOS from the same technology is chosen for NMOS transistors which are sensitive to body bias. The corresponding layout is shown in Figure 8. The triple-well process allows a P-well to be placed inside an N-well, resulting in three types of well structures. This third type of well is useful for isolating circuitry within it from other sections on the chip by the reverse bias between the N-well and the P-substrate. For mixed-signal designs, where noise injection can be a problem, the analog sections can be completely isolated from the digital section by using this third type of well structure. There is no resistive path between the analog and digital circuit, since the P-well connected to the analog VSS is isolated fromthe digital VSS/ground by a reverse biased N-well. The triple-well also significantly reduces the capacitive coupling between the analog VSS and digital VSS/ground. Consequently, a high degree of isolation is achieved for sensitiveanalog circuits from detrimental digital noise sources.

It can be observed that most of the chip area is occupied by the capacitor and pass transistor. The total chip area is $544\,\mu\text{m} \times 377\,\mu\text{m}$ while area of the control circuitry is only $181\,\mu\text{m} \times 94\,\mu\text{m}$.

4. TESTING AND RESULTS

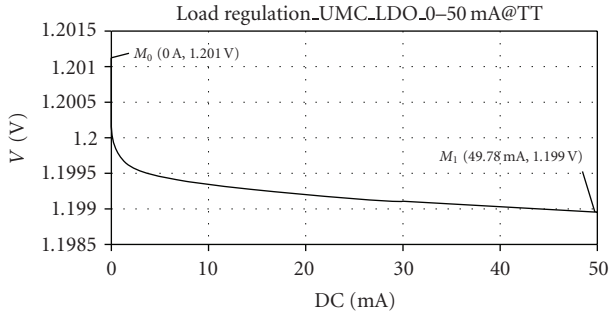
The proposed LDO is simulated on Spectre targeted to be fabricated in UMC 180 nm. Results are tested at five different process corners. Line regulation, load regulation, transient response is evaluated at slow-slow (SS), typical-typical (TT), fast-fast (FF), slow N-fast P(SNFP), fast N-slow P(FNSP).

The transient response is obtained by applying load current pulse of 0–50 mA with 1 microsecond rise and fall times. The corresponding results are tabulated in Table 2. The table clearly shows that the proposed capacitor-less LDO with folded cascode error amplifier exhibits better line and load regulations relative to the reported architecture [1]. A worst-case settling time of 13.1 microseconds is observed against 15 microseconds [1]. Corresponding plots for the process corner TT are shown in Figures 9(a)–9(d). The AC response for different load currents is shown in Figure 10. It can be observed that deviation in phase margin is negligible for all load currents from 50 mA to 1 mA. Also the gain is found to be in the vicinity of 75 dB for all load currents.

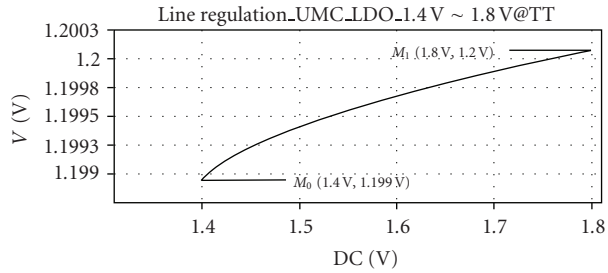
Power supply ripple rejection ratio (PSRR) is a measure of how well a circuit rejects ripple coming from the input power supply at various frequencies. One of the dominant internal sources of PSRR in an LDO is the bandgap reference. Any ripple that makes its way onto the reference will be amplified and sent to the output. The power supply rejection ratio is defined as

$$\text{PSRR} = 20\log\frac{\text{ripple}_{\text{input}}}{\text{ripple}_{\text{output}}}.$$

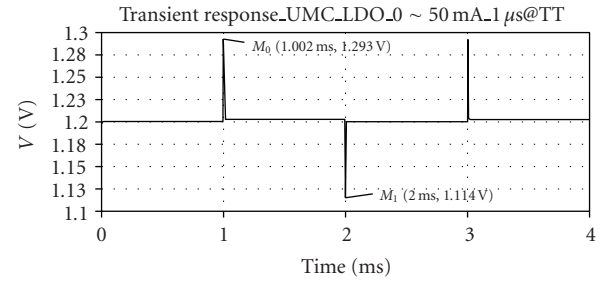
The PSRR is measured by super imposing a sine wave on V_{DD} or by simply setting AC = 1 for V_{DD} settings. The larger the open loop gain, the better the PSRR is. Enough care is taken while designing the error amplifier so that any external circuitry for improving PSRR is avoided. Thus quiescent current budget is minimized. The PSRR is depicted in Figure 11. It can be observed that PSRR of 45.5 dB is



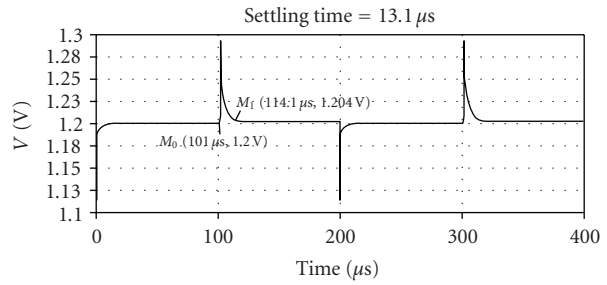
(a) Load regulation (zoomed) of LDO for a variation of load current from 0 mA to 50 mA for TT process corner



(b) Line regulation (zoomed) of LDO for a variation supply voltage from 1.4 V to 1.8 V for TT process corner



(c) Transient response of LDO for a variation of load current from 0 mA to 50 mA for TT process corner. Maximum overshoot is 1293 − 1.2 = 93 mV, while maximum undershoot is 1.2 − 1.114 = 86 mV



(d) Settling time demonstration of the proposed LDO for variation of load current from 0 mA to 50 mA at 1 microsecond rise and fall times

Figure 9

achieved till 10 KHz which is apt for digital baseband section of the receiver. It can also be noticed that the PSRR begins to worsen beyond 0.1 MHz as the operating frequency drift beyond the unity gain frequency, where feedback has little control.

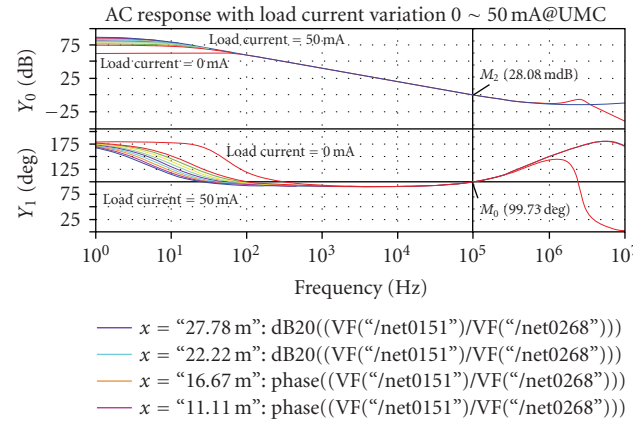
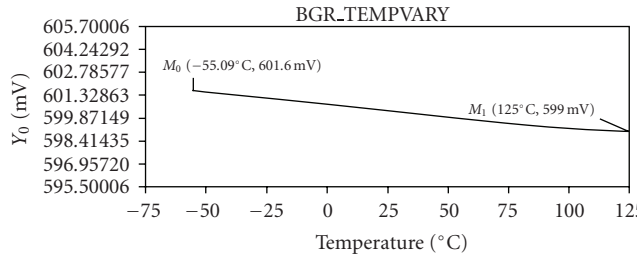
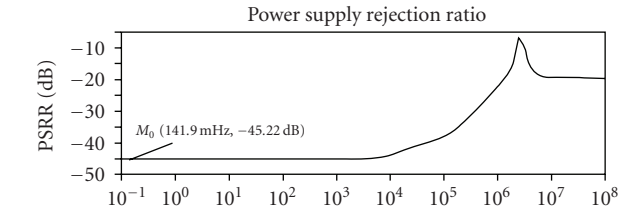


Figure 10: Open loop frequency response of LDO for varying load current.



(a) Band gap reference output voltage variation with temperature



(b) PSRR of the LDO regulator proposed

Figure 11

5. CONCLUSIONS

The proposed LDO which is simulated using 180 nm, 1.8 V supply voltage exhibits better line and load regulations against different process corners, while consuming a quiescent current of 100 μA. It is found to exhibit load regulation (even under worst case) of 48 ppm/mA and transient response reveals that when the load current is varied from 0 mA to 50 mA, then the undershoot is limited to a maximum value of 1.05 V and overshoot is observed to a maximum value of 1.3 V and the settling time is found to be 13.1 microseconds. These above results along with the fact that it is designed to operate with a dropout voltage of 200 mV on 180 nm will make the design a robust deep submicron on-chip LDO voltage regulator.

REFERENCES

[1] R. J. Milliken, J. Silva-Martínez, and E. Sánchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Transactions on Circuits and Systems I*, vol. 54, no. 9, pp. 1879–1890, 2007.

[2] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 629–633, 1983.

[3] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, NY, USA, 1996.