A Hybrid Seven-level Inverter for IM Drive

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***Abstract*-- A new seven-level inverter topology for IM drive is proposed in this paper. This topology consists of two three-phase two-level inverters fed by isolated DC voltage sources and six H-bridges fed by capacitors. An important advantage of this topology is the reduction in DC link voltage magnitude by half when compared with the requirement of DC link voltage in conventional NPC or flying capacitor topologies. The switching state redundancies that exist in generating the middle voltage levels are effectively utilized in balancing the H-bridge capacitor voltages. The proposed topology is inherently capable of preventing the circulation of triplen harmonic current caused by the common mode voltage appearing on the motor winding. Another feature that enhances the reliability of the proposed drive system is its ability to function in three-level mode in case of any switch failure in H-bridges. Extensive simulation study and experimental verification of the proposed topology are carried out for the entire modulation range.**

***Index Terms*-- Multilevel inverters, H-bridge, Induction Motor drive**.

I INTRODUCTION

Multilevel Power Converters have emerged as an attractive choice for medium and high voltage applications due to their ability to generate voltage waveform with less harmonic distortion at reduced switching frequency. These converters can use switching devices of low voltage ratings to generate a step approximation of a high voltage sinusoidal waveform [1, 2]. Multilevel inverters are being increasingly used in the control of medium and high voltage AC drives in the industry due their advantages cited above [3, 4]. However, the multilevel inverters suffer from certain disadvantages that large number of switching devices and their control circuit make the system more complex and less reliable. Hence, the research in this field is mainly driven by the need to develop less complex, more reliable and efficient multilevel inverter topologies.

Different multilevel inverter topologies and their control schemes have been briefly presented in [5]. The Neutral Point Clamped (NPC) inverter is a prominent topology in the group of conventional multilevel inverters [6]. One of the major issues with this topology is the fluctuations in voltages across the series connected capacitors used for splitting the DC link voltage into smaller voltage levels. Hence, special switching strategy is required for balancing the capacitor voltages. Various techniques for capacitor voltage balancing have been reported in the literature [7, 8]. Large number of clamping diodes is required in the NPC circuit especially when the number of levels is high.

The Flying capacitor inverter, which uses series connection of capacitor clamped switching cells to generate multilevel voltage profile is another well known conventional multilevel topology introduced by T.A.Meynard and H.Foch in the year 1992 [9]. The voltages across the flying capacitors have to be maintained at the required level under all conditions of operation. A method to achieve balancing of the capacitor voltages is presented in [10]. The flying capacitor topology does not require any clamping diodes. However, this topology requires large number of capacitors to achieve higher number of voltage levels.

The cascaded H-bridge multilevel inverter is another well-known topology belonging to the category of conventional multilevel inverters. In this topology, multilevel structure is realized by series connection of H-bridge cells fed from isolated DC voltage sources [11, 12]. This topology has gained much attention in high power applications because of its modular structure and simple control circuitry. The main disadvantage of this topology is the requirement of substantial number of isolated DC voltage sources when the number of levels increases. There are several other multilevel converters, which can be considered as variants of the conventional topologies or their hybrid versions [13].

The concept of dual inverter configuration of multilevel inverter for induction motor with open-end windings is introduced by H. Stemmler and P. Guggenbach in the year 1993 [14]. In this topology, each end of the motor phase winding is connected to an inverter for achieving multilevel voltage profile in the winding. Generation of three-level voltage profile in the motor winding using two conventional two-level inverters is presented in [15]. The number of voltage levels in the motor winding can be increased further by cascading two and three level inverters. A scheme for common mode voltage elimination in an induction motor, fed from both the ends of the windings with three-level inverters, is presented in [16]. In the topology proposed in [17] a seven-level inverter topology is realized by cascading four two-level and two three-level inverters.

A new hybrid seven level inverter topology comprising of two two-level inverters and six H-bridges, for Induction motor with open-end winding structure, is proposed in this paper. The two-level inverters feed the coils from both the ends through two capacitor-fed H-bridge cells connected in series with each phase of the motor winding. The redundant switching states available for generating the middle voltage levels are utilized in balancing the capacitor voltages in the entire modulation range.

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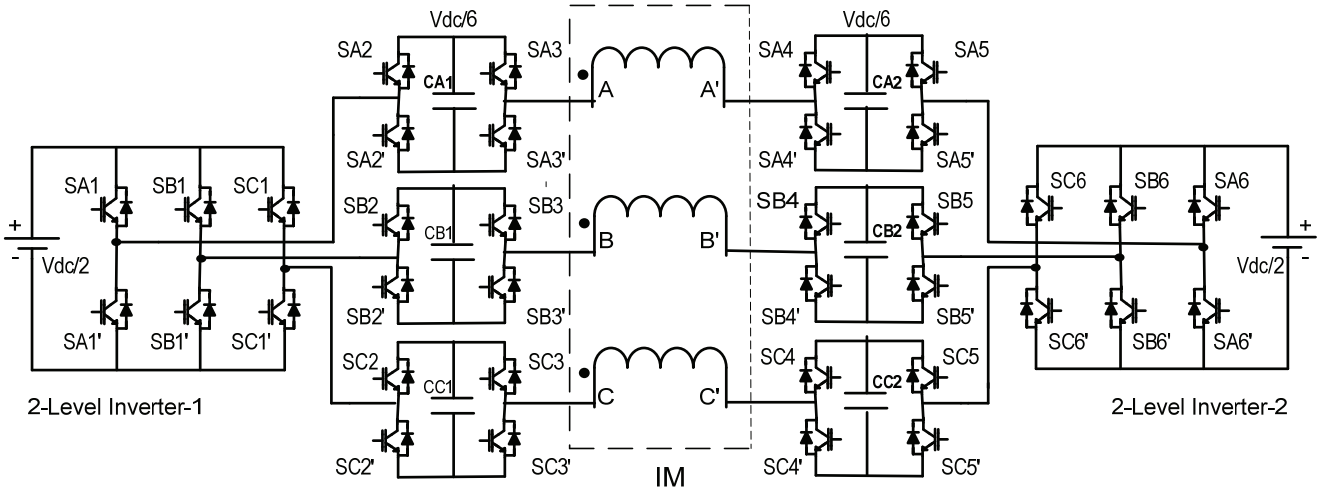

Fig. 1. Power Circuit Diagram of the proposed seven-level inverter drive topology

II PROPOSED HYBRID SEVEN-LEVEL INVERTER

The power circuit diagram of the proposed seven-level inverter is given in Fig.1. In this topology, the induction motor with open-end stator windings is fed from both the sides of the windings by two three-phase two-level inverters cascaded with two H-bridges per phase to realize the seven-level structure. Isolated DC voltage sources of magnitude Vdc/2, feed each two level inverter, where Vdc is the dc-link voltage required by the conventional NPC seven-level inverter. The H-bridges, connected in series with each phase of the motor windings, are fed by capacitors whose voltages are maintained at a level of Vdc/6, as explained later in this paper. This circuit is capable of generating the seven voltage levels of +Vdc/2, +2Vdc/6, +Vdc/6, 0, -Vdc/6, -2Vdc/6 and -Vdc/2. The switch states for generating these voltage levels in A-phase are given in table-I. If the H-bridge cells are clamped to zero voltage, the two two-level inverters can generate voltage levels of +Vdc/2, 0 and –Vdc/2. The other voltage levels can be generated by connecting the two-level inverters in series with the H-bridges or by clamping the two-level inverters to zero voltage and using only the H-bridge voltages. For example the voltage level of +2Vdc/6 can be generated by either subtracting any one of the capacitor voltages (Vdc/6) from the supply source (Vdc/2) or adding the two capacitor voltages and clamping the two-level inverters to zero voltage.

A crucial factor in ensuring proper functioning of the proposed topology is the balancing of the H-bridge capacitors CA1, CA2, CB1, CB2, CC1 and CC2. These capacitors can be charged or discharged by changing the direction of the load current flowing through them. As the capacitors are bypassed while generating voltage levels of +Vdc/2, 0 and –Vdc/2 their voltages are not affected. Since any one or both capacitors are used for generating all the other voltage levels in a phase, balancing of the capacitor voltages has to be ensured. This can be achieved by effectively making use of the switching state redundancies. The switching logic to ensure capacitor voltage balancing in phase-A is illustrated in table-I. Similar switching logics are followed in phase-B and phase-C. It can be seen from this table that there are multiple ways of generating the middle voltage levels of +2Vdc/6, -2Vdc/6, +Vdc/6 and -Vdc/6. The H-bridge capacitors can be charged or discharged in any direction of the phase current for these voltage levels by selecting appropriate switching combinations. This switching logic is implemented by comparing the capacitor voltages with the desired voltage (Vdc/6 $\pm$ allowed ripple) in every switching cycle. Hence, the capacitor voltage correction is almost instantaneous relative to the fundamental period.

III PWM CONTROL AND SWITCHING LOGIC

The Space Vector Pulse Width Modulation (SVPWM) technique for multilevel inverters, proposed in [18], is used for generating the switching signals of the inverter. The induction motor is operated in constant V/f control mode. The three reference phase voltages (va*, vb*and vc* for phases A, B and C respectively) are generated from the reference voltage space vector magnitude ($\underline{V}$r*) which is determined from the constant V/f ratio and the speed requirement of the motor. As in the case of carrier based SVPWM for two-level inverters, an offset voltage is added to the three reference voltages va*, vb* and vc* to generate a new set of reference voltages va1*, vb1*and vc1*. The offset voltage is determined as follows.

$v_{offset} = -(v_{max} + v_{min})/2$

where $v_{max} = \max(v$a*, vb*, vc*) and $v_{min} = \min(v$a*, vb*, vc*)

va1* = va* + v_{offset}

vb1* = vb* + v_{offset}

vc1* = vc* + v_{offset}

The new reference voltages (va1*, vb1*, vc1*) are compared with six level shifted triangular carrier waveforms for generating the PWM signals. The addition of offset voltage increases the utilization of DC bus voltage by extending the range of linear modulation. With constant V/f ratio, the magnitude of the reference voltage space vector ($\underline{V}$r*) changes linearly with the motor speed requirement, within

TABLE-1
SWITCHING LOGIC FOR THE SEVEN VOLTAGE LEVELS OF A-PHASE

Phase Voltage Levels	CONDITIONS FOR SELECTION OF SWITCH STATES					SWITCH STATES TO BE SELECTED					
	CAPACITOR - CA1		CAPACITOR - CA2		Current Direction	SA1	SA2	SA3	SA4	SA5	SA6
	Vca1	Required Action	Vca2	Required Action							
+2Vdc/6	< Vdc/6	charging	<or >Vdc/6	status quo	*i*a >0	1	1	0	0	0	0
	> Vdc/6	discharging	<or >Vdc/6	status quo	*i*a <0	1	1	0	0	0	0
	> Vdc/6	status quo	< Vdc/6	charging	*i*a >0	1	0	0	1	0	0
	< Vdc/6	status quo	> Vdc/6	discharging	*i*a <0	1	0	0	1	0	0
	> Vdc/6	discharging	> Vdc/6	discharging	*i*a >0	0	0	1	0	1	0
	< Vdc/6	charging	< Vdc/6	charging	*i*a <0	0	0	1	0	1	0
+Vdc/6	< Vdc/6	charging	< Vdc/6	charging	*i*a >0	1	1	0	1	0	0
	> Vdc/6	discharging	> Vdc/6	discharging	*i*a <0	1	1	0	1	0	0
	> Vdc/6	discharging	<or >Vdc/6	status quo	*i*a >0	0	0	1	0	0	0
	< Vdc/6	charging	<or >Vdc/6	status quo	*i*a <0	0	0	1	0	0	0
	< Vdc/6	status quo	> Vdc/6	discharging	*i*a >0	0	0	0	0	1	0
	> Vdc/6	status quo	< Vdc/6	charging	*i*a <0	0	0	0	0	1	0
-Vdc/6	< Vdc/6	charging	< Vdc/6	charging	*i*a <0	0	0	1	0	1	1
	> Vdc/6	discharging	> Vdc/6	discharging	*i*a >0	0	0	1	0	1	1
	> Vdc/6	discharging	<or >Vdc/6	status quo	*i*a <0	0	1	0	0	0	0
	< Vdc/6	charging	<or >Vdc/6	status quo	*i*a >0	0	1	0	0	0	0
	<or >Vdc/6	status quo	> Vdc/6	discharging	*i*a <0	0	0	0	1	0	0
	<or >Vdc/6	status quo	< Vdc/6	charging	*i*a >0	0	0	0	1	0	0
-2Vdc/6	<or >Vdc/6	status quo	< Vdc/6	charging	*i*a <0	0	0	0	0	1	1
	<or >Vdc/6	status quo	> Vdc/6	discharging	*i*a >0	0	0	0	0	1	1
	< Vdc/6	charging	<or >Vdc/6	status quo	*i*a <0	0	0	1	0	0	1
	> Vdc/6	discharging	<or >Vdc/6	status quo	*i*a >0	0	0	1	0	0	1
	> Vdc/6	discharging	> Vdc/6	discharging	*i*a <0	0	1	0	1	0	0
	< Vdc/6	charging	< Vdc/6	charging	*i*a >0	0	1	0	1	0	0
+Vdc/2	Unaffected					1	0	0	0	0	0
0	Unaffected					0	0	0	0	0	0
-Vdc/2	Unaffected					0	0	0	0	0	1

Note: '1' denotes ON position of the switch, '0' denotes OFF position of the switch. The switch SAx is ON automatically implies that the switch SA'x is OFF and vice- versa, where x=1, 2,3,4,5, 6. The current from the terminal A to A' of the motor winding is assumed to be the positive direction of current. Vca1 and Vca2 are the voltages across the capacitors CA1 and CA2respectively. *i*a is the current in A-phase winding. Similar switching logic is followed in B-phase and C-phase.

the linear modulation range. The modulation index (M) is defined as the ratio of the magnitude of the reference voltage space vector ($\underline{V}r^*$), generated by the three phase voltages, to the maximum magnitude of the voltage space vector (Vdc). The limit of M for linear modulation is given by:

$$M = |\underline{V}r^*| / Vdc = \cos(30) = 0.866$$

The new A-phase reference voltage (va1*) along with the six level shifted triangular carrier waveforms is shown in Fig.2 for a modulation index of 0.8. It can be seen that the reference voltage for M=0.8 spans all the six level shifted triangular carriers. This reference voltage waveform is compared with the triangular carrier waveforms to generate the PWM signals. When the magnitude of reference voltage waveform is greater than the triangular carrier PWM logic level is high ('1') otherwise it is low ('0'). However, in actual implementation it is difficult to realize such level shifted triangular carriers in DSP. Hence, only one triangular carrier waveform is used for comparison. Whenever the reference voltage waveform traverses from one carrier region to the next carrier region, it is shifted and scaled to reside within one triangle as shown in Fig.3. This is done using the information of carrier level in which the voltage reference waveform actually resides at a particular instant.

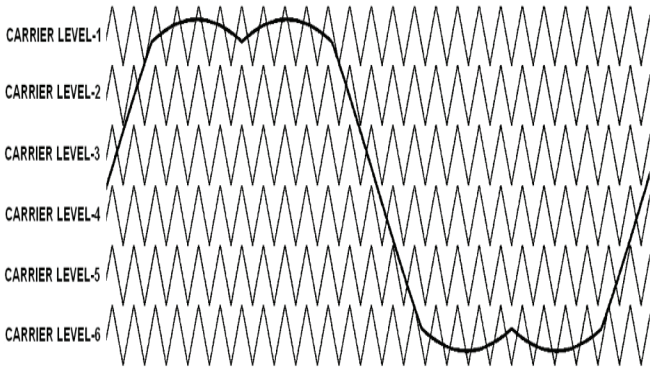

Fig. 2. Reference voltage waveform (after addition of v_{offset}) and the six level shifted triangular carriers

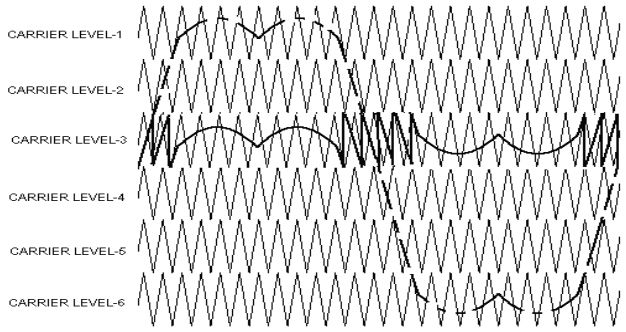

Fig.3. Reference voltage waveform shifted and scaled to reside within one triangle.

The voltage level that has to be applied to the Induction motor is determined from the carrier level information and the PWM signals, following the logic given in table -II. The gating signals for the switches are generated based on the switch states to be selected to realize a particular voltage level in a given condition, as shown in table-I.

IV SALIENT FEATURES

The proposed topology requires two DC voltage sources of voltage rating only Vdc/2 to generate voltage space vector of maximum magnitude Vdc. Thus, the magnitude of the DC link voltage required in this topology is only half of the DC link voltage magnitude required in the conventional NPC or flying capacitor topologies. The switches in the two-level inverters are rated for a voltage blocking capability of Vdc/2 where as the switches in H-bridges are rated for a voltage blocking capability of Vdc/6. Table-I clearly shows that the two-level inverters switch only during a half cycle of the reference voltage waveform. Even in a half cycle, the two-level inverters do not switch for generating the middle voltage levels under certain conditions. Hence, the switchings in the two-level inverters, which operate at a higher voltage level of Vdc/2, are much less compared to the switchings in the H-bridge cells, which operate at a lower voltage level of Vdc/6. This results in switching loss reduction and improvement in overall drive system efficiency.

The common mode (triplen) voltage appearing on motor winding is an inherent feature of the SVPWM technique. This triplen harmonic voltage can cause high triplen harmonic current flow through the motor windings. In the proposed topology, the two 2-level inverters are fed from two isolated voltage sources, thereby preventing the circulation of triplen harmonic current through the motor windings. Another attractive feature of the proposed topology is that if the switches in the H-bridges fail, the system can be operated as a three level inverter, in the entire modulation range, by bypassing the H-bridges.

V SIMULATION RESULTS

Simulations have been carried out in MATLAB-Simulink platform to study the performance of the proposed seven-level inverter feeding an Induction motor rated 5 HP, 415V, 4-pole, 50 Hz, for the entire modulation range. The constant V/f control scheme is used for running the motor at different

TABLE-II
DETERMINATION OF VOLTAGE LEVEL FROM CARRIER LEVEL AND PWM SIGNAL

Carrier Level	PWM Signal	Voltage Level
1	1	+Vdc/2
	0	+2*Vdc/6
2	1	+2*Vdc/6
	0	+Vdc/6
3	1	+Vdc/6
	0	0
4	1	0
	0	-Vdc/6
5	1	-Vdc/6
	0	-2*Vdc/6
6	1	-2*Vdc/6
	0	-Vdc/2

modulation indices spanning from two levels to seven level operation of the inverter. The H- bridge capacitors have to be selected properly to restrict the ripple voltage within acceptable limits. The capacitance of H-bridge capacitor can be determined by using the formula given below.

$$C = I_P * \frac{\Delta T}{\Delta V}$$

where C is the capacitance of the H-bridge capacitors (CA1, CA2, CB1, CB2 CC1 and CC2), Ip is the peak phase current, ΔT is the inverter switching time (Ts) and ΔV is the peak-to-peak voltage ripple allowed in the H-bridge capacitor. If the peak-to-peak ripple voltage allowed in the capacitor is 5V, for a switching frequency of 2 KHz the Capacitance required is 1150 μF.

Simulation waveforms when the motor is running on load are given in figures 4, 5 and 6. Fig.4 shows the simulation waveforms of motor phase voltage, phase current and H-bridge capacitor voltages pertaining to three-level operation of the inverter corresponding to a modulation index of 0.2. The motor operates at a frequency of 10Hz at this modulation index. It can be seen that the capacitor voltages are well balanced. Fig.5 shows the simulation waveforms when the inverter operates in five-level mode corresponding to a modulation index of 0.5. The motor operates at a frequency of 25Hz at this modulation index.

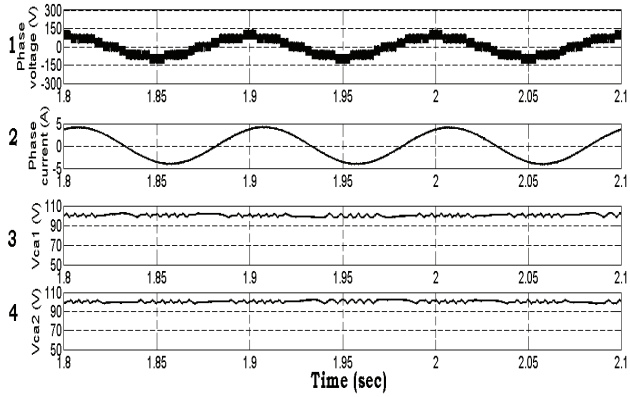

Fig.4. Voltage and Current wave forms when inverter operates at modulation index M=0.2. X-axis : 50ms/div. (1) A-phase voltage (Y axis :150V/div)., (2) A-phase current (Y axis :5A/div), (3) Ripple in H-bridge capacitor voltage V_{CA1} (Y axis :20V/div)., (4) Ripple in H-bridge capacitor voltage V_{CA2} (Y axis :20V/div).

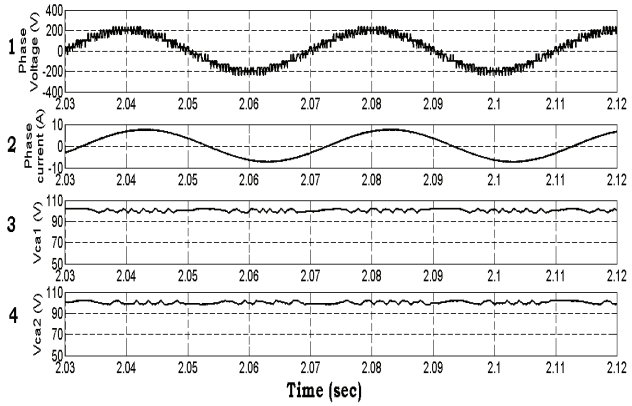

Fig.5. Voltage and Current wave forms when inverter operates at modulation index M=0.5. X-axis : 10ms/div. (1) A-phase voltage (Y axis :200V/div)., (2) A-phase current (Y axis :10A/div), (3) Ripple in H-bridge capacitor voltage V_{CA1} (Y axis :20V/div)., (4) Ripple in H-bridge capacitor voltage V_{CA2} (Y axis :20V/div).

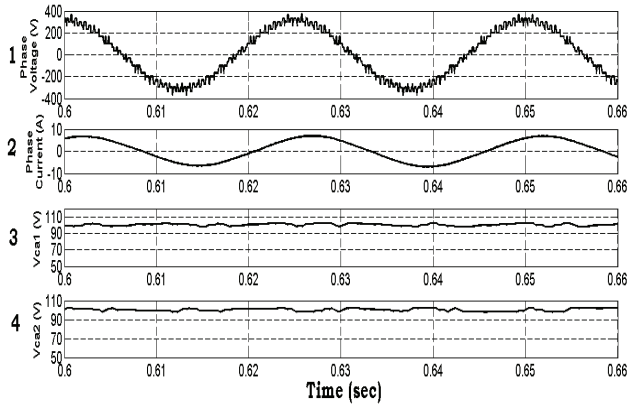

Fig.6. Voltage and Current wave forms when inverter operates at modulation index M=0.8. X-axis : 10ms/div. (1) A-phase voltage (Y axis :200V/div)., (2) A-phase current (Y axis :10A/div), (3) Ripple in H-bridge capacitor voltage V_{CA1} (Y axis :20V/div)., (4) Ripple in H-bridge capacitor voltage V_{CA2} (Y axis :20V/div).

Simulation waveforms when the motor runs at a frequency of 40 Hz (modulation index of 0.8) corresponding to seven-level operation of the inverter are given in Fig.6. The waveforms of V_{CA1} and V_{CA2} in Fig.4, Fig.5 and Fig.6 show that the capacitor voltages are well balanced.

VI EXPERIMENTAL RESULTS

Experimental verification of the proposed topology is carried out on an Induction motor rated 5 HP, 415V, 4-pole, 50 Hz, in constant V/f control mode, under no load condition. IGBTs are used as switching devices. Hall Effect sensors are used for sensing H-bridge capacitor voltages, DC link voltage and motor currents. The controller is implemented in TMS320F2812 DSP platform. The switching logic is implemented in SPARTAN-3 XC3S200 FPGA. The switching frequency is kept constant at 2 KHz. The FPGA receives PWM signals and information on carrier levels, capacitor voltage levels and current directions from the DSP for generating gating signals for IGBTs.

The waveforms pertaining to seven level operation of the inverter (modulation index of 0.8) are shown in Fig.7 and Fig.8. The motor operates at a frequency of 40 Hz under this condition. It can be seen from these waveforms that the H-

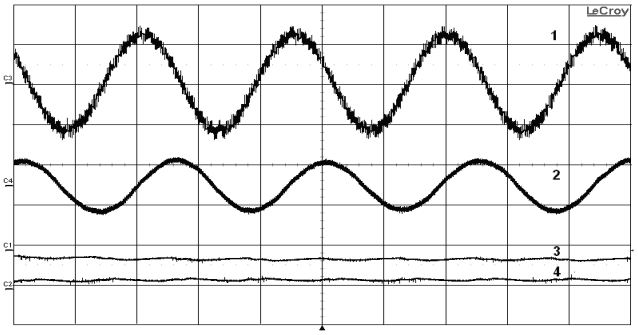

Fig.7. Voltage and Current wave forms when inverter operates at modulation index M=0.8. X-axis : 10ms/div. (1) A-phase voltage (Y axis :200V/div), (2) A-phase current (Y axis :2A/div), (3) Ripple in H-bridge capacitor voltage V_{CA1} (Y axis :5V/div), (4) Ripple of H-bridge capacitor voltage V_{CA2} (Y axis :5V/div).

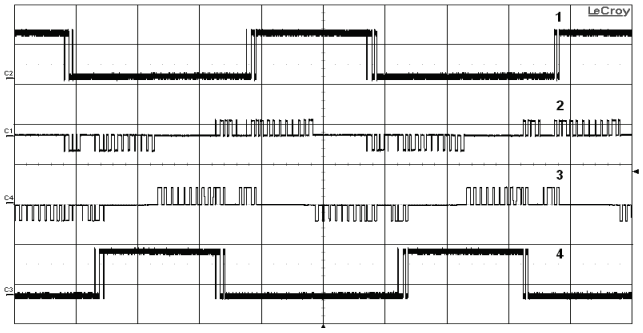

Fig.8. Pole voltage wave forms when inverter operates at modulation index M=0.8. X-axis : 5ms/div., Y axis :200V/div. (1) 2-level inverter-1, (2) H-bridge cell-CA1, (3) H-bridge cell-CA2, (4) 2_level inverter-2.

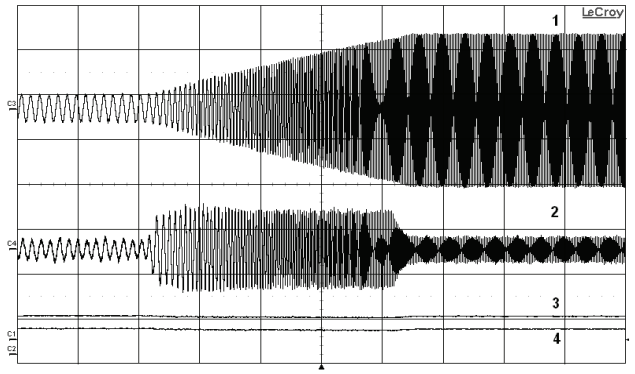

Fig.9. Voltage and Current wave forms under transient condition of acceleration of the motor from 6.5Hz to 40 Hz. (1) A-phase voltage (Y axis :100V/div), (2) A-phase current (Y axis :2A/div), (3) H-bridge capacitor voltage V_{CA1} (Y axis :100V/div). (4) H-bridge capacitor voltage V_{CA2} (Y axis :100V/div).

bridge capacitor voltages are well balanced and the peak to peak ripple voltage is only around 2V. Fig.9 depicts the transient performance of the drive during sudden acceleration from 6 Hz to 40 Hz, corresponding to the transition from two-level to seven-level operation of the inverter. It is evident that the capacitor voltages remain balanced even during transient condition.

The simulation and experimental results establish the fact that in the proposed topology of seven-level inverter, it is possible to achieve balancing of capacitor voltages in the entire modulation range. From the pole voltage waveforms

(Fig.8) of two-level inverter-1, H-bridge cell-CA1, H-bridge cell-CA2 and two-level inverter-2, it can be seen that the two-level inverters switch only during a half cycle of the waveform. As has been explained above, this results in switching loss reduction.

VII CONCLUSION

In this paper a new hybrid seven-level inverter topology for Induction motor drive, using two two-level inverters and six capacitor-fed H-bridge cells, is presented. The DC link voltage magnitude required by this topology is only half of the magnitude of DC link voltage required in the conventional NPC or flying capacitor topologies. The H-bridge capacitor voltages are balanced by utilizing the switching state redundancies. In the event of any switch failure in H-bridges, this inverter can operate in three-level mode, in the entire modulation range, by bypassing the H-bridges. This feature enhances the reliability of the proposed inverter. It has been shown that the high voltage two-level inverters switch much less compared to the switching of low voltage H-bridge cells, thereby reducing the switching loss and improving the efficiency of the drive system. As the two-level inverters are fed from two isolated DC voltage sources, this topology is inherently capable of preventing the circulation of triplen harmonic current in the motor winding. The results of the simulation study and experiment show that the proposed topology is suitable for drive applications.

REFERENCES

[1] . Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel Converters: An Enabling Technology for High-power Applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-source-converter Topologies for Industrial Medium-voltage Drives," *IEEE Transactions on Industrial Electronics.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[4] Mohan M. Renge and Hiralal M. Suryawanshi, "Five-Level Diode clamped Inverter to eliminate Common Mode Voltage and Reduced dv/dt in Medium voltage rating Induction Motor Drives, *IEEE Transactions on Power Electronics,* vol. 23, no.4, pp. 1598–1607 July 2008.

[5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial. Electronics.*, vol. 49, no. 4, pp.724-738,Aug.2002.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-point Clamped PWM Inverter," *IEEE Transactions on Industry Applications*, pp. 518–523, 1981.

[7] S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau, "Pulsewidth Modulations for the Comprehensive Capacitor Voltage Balance of *n*-level Three-leg Diode-clamped Converters," *IEEE Trans. on Power Electronics*, vol.24, no.5,pp.1364–1375,May 2009.

[8] Hirofumi Akagi and Takaaki Hatada, Voltage Balancing Control for a Three-Level Diode-Clamped Converter in a Medium Voltage Transformerless Hybrid Active Filter, *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 571-579, March 2009.

[9] T.A Meynard and H.Foch, "Multilevel choppers for high voltage applications" in Proce. Europian Conference on Power Electronics and applications, 1992, pp. 45-50.

[10] Brendan Peter McGrathand Donald Grahame Holmes, Natural Capacitor Voltage Balancing for a Flying Capacitor Converter Induction Motor Drive, *IEEE Transactions on Power Electronics,* vol. 24, no. 6, pp. 1554-1561, June 2009.

[11] N. P. Schibli, T. Nguyen, and A. C. Rufer, "A three-phase multilevel converter for high-power induction motors," *IEEE Trans. Power Electron.*, vol. 13, no. 5, Sept. 1998, pp. 978-986.

[12] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static Var generation, *IEEE Trans. Ind. Applicat.*, vol. 32, no. 5, Sept./Oct. 1996, pp. 1130-1138.

[13] M. Veenstra, and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Transactions on Industry Applications*, vol. 41, no. 2, no.3, March/April 2005, pp. 655-664.

[14] H. Stemmler, and P. Guggenbach, "Configurations of high-power voltage source inverter drives", in *Proc. EPE-1993*, Brighton, U.K., 1993, vol. 5, pp. 7-14.

[15] V. T. Somasekhar, K. Gopakumar, M. R. Baiju, K. K. Mohapatra, and L. Umanand, "A multilevel inverter system for an induction motor with open-end windings," *IEEE Transactions on Industrial Electronics*,Vol.52, no. 3, pp 824–836, Jun. 2005.

[16] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "A Dual Five level Inverter-fed Induction Motor Drive With Common mode Voltage Elimination and DC-link Capacitor Voltage balancing Using Only the Switching-state Redundancy–part I," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, pp. 2600-2608, Oct. 2007.

[17] G. Mondal, K. Sivakumar, R. Ramchand, K. Gopakumar, and E. Levi, "A Dual Seven-level Inverter Supply for an Open-end Winding Induction Motor Drive," *IEEE Transactions on IndustrialElectronics*, vol. 56, no. 5, pp. 1665–1673, May 2009.

[18] R.S. Kanchan, M.R. Baiju, K.K. Mohapatra, P.P. Ouseph and K.Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *IEE Proceedings - Electric Power Applications*, volume 152, no.2, pp: 3297-309, April 2005.