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REVIEW PAPER

MICROPROCESSORS IN PROCESS CONTROL

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Improvements in LSI technology have resulted in the development of the Microprocessor. The evolution of microprocessor architecture during the past decade has progressed at an incredible pace. From the primitive 4004 in 1971 to the present spectrum of sophisticated microprocessors, the growth has been swift, dramatic and revolutionary. Today's products possess astonishing computational capabilities. In this article, the architectural features of a few commercially available 16-bit microprocessors are discussed. Trends in VLSI technology are also indicated.

The idea of computer control of processes is not new; but, the availability of the microprocessor made the embedded systems flexible, reliable and economically viable. The use of the microprocessor in programmable logic controllers, data acquisition and alarm annunciators, direct digital control, supervisory control and on-line estimation are discussed.

The trends in control algorithm development to suit the microprocessor, distributed control, and the issues in software for real-time applications are also presented.

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SOARING COSTS OF energy and shortage of raw materials are putting stringent demands on control systems in process industries. In view of these demands, computers have assumed significance in process control. Computer process control has seen an upsurge with the advent of LSI technology. A large number of such applications have appeared in recent literature. Algorithms have been designed to suit microprocessors. One of the aims of modern digital control algorithms is that the on-line control computations must be simple and fast. Standard estimation algorithms are reformulated and solved leading to algorithms which are easy to implement on microprocessors.

The ubiquitous microprocessor is finding its way into an amazing array of application as the control component replacing high cost and less flexible mechanical and random logic technologies. In the next section, the 8-bit microprocessors are briefly discussed. The architectural features of the commercially available Intel 8086, Zilog Z8000, Texas Instruments TI9900 and Motorola 68000 are outlined next. Then, the functions of a computer process control are discussed. Also the objectives, various strategies and levels of computer control are described. Finally, the trends in digital control and issues in software are outlined.

8-BIT MICROPROCESSORS

In 1971, the first commercially available microprocessor, the Intel 4004 was released by Intel Corporation. The 8008 was introduced in April 1972 as an eight-bit parallel CPU with 45 instructions oriented towards character-string handling. It had a 30-μs average instruction execution time and offered six eight-bit general purpose registers. It was packaged in an 18-pin DIP and was executed in silicon gate PMOS technology requiring a minimum of 20 TTL packages for memory and I/O interface. The 8008 could address 16 k bytes of memory. With the introduction of the Intel 8080 in April 1974, microprocessors took a major step forward. It quickly became accepted as the standard eight-bit machine and was widely second sourced. With a two-μs instruction cycle and 30 more instructions, the 8080 offered a ten fold increase in throughput over 8008. It could directly address 64 k bytes of memory versus the 8008's 16 k bytes. Package size moved upto a 40-pin DIP from the 18-pin 8008.

The rapid acceptance of and high demand for the 8080 spawned two eight-bit competitors, the Motorola 6800 and the Zilog Z80. The 6800, introduced in mid-1974, was the first +5 V single-power-supply microprocessor. Elimination of the need for multiple power supplies lowered product cost and made the 6800 a popular processor. Motorola also introduced a development system and four peripheral chips mated to the 6800. Peripheral processors replaced the significant amount of TTL necessary with first generation microprocessors and gave designers useful building blocks to execute functions such as CRT and floppy disk control. Over the years, Intel and other manufacturers have introduced a broad range of peripherals to support CPUs.

Zilog's Z80, introduced in 1976, reflected improvements in architecture made since the 8080's introduction. One of its important features was that it incorporated the 8080's instruction set and opcodes within its 158 instructions. Thus the Z80 was entirely compatible with the numerous programmes that had been written by that time for the 8080. The Zilog Z80 offered definite performance enhancements over early eight-bit processors.

The Intel 8085, introduced in 1976 was a single power supply +5 V device that required fewer peripherals than the 8080 and offered features such as vectored interrupts and a serial I/O port.

Another eight-bit advance was, the arrival late in the decade, of processors such as Texas Instrument's 9980,

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Intel's 8088 (iAPX 88), and Motorola's 6809. These devices offered eight-bit external buses but processed data internally in 16-bit words. This approach permits full compatibility with eight-bit hardware, while also providing faster processors if programme complexity warrants it.

The first eight-bit single-chip microcomputer was Intel's 8048, introduced in 1976. Progress in device density made it possible to put a CPU, I/O, RAM and ROM on one die. Motorola, Rockwell, and other firms followed with their own devices and many manufacturers second-sourced the 8048.

With the emergence of the 8080, 6800 and Z80, N-channel MOS became the dominant mode for general purpose microprocessors. Bipolar offered speed, CMOS offered low power, but NMOS offered density and enough speed to make it the preferred technology for general-purpose applications.

16-BIT MICROPROCESSORS

Microprocessor technology has entered a new and especially challenging era with the introduction of the 16-bit microprocessor. Previous generations of microprocessors were limited by the available technology. Microprocessors were limited in number of registers, data path width, and instruction-set power primarily because technology could not support more features on a single chip. Other limitations were too small an address space and awkwardness of address computation which could also be attributed to the technology constraint.

The basic microprocessor technology has steadily advanced in the last few years. The most noticeable improvement has been circuit density, which translates directly into the amount of capability that can be put on a single-chip microprocessor. Whereas the earlier (8-bit) microprocessors contained from 5000 to 10,000 transistors per chip, current 16-bit processors have from 25,000 to 70,000 transistors. Circuit density is not the only technology advance that has been made; corresponding improvements have been achieved in circuit speed and power dissipation. The major advance, increased circuit density, is the result of gradual improvements in processing techniques that permit smaller circuit dimensions.

The available 16-bit microprocessors possess astonishing computational capabilities and support primary memories upto 64 M bytes. They incorporate high-level languages and technical innovations only recently introduced on larger main-frames. Microprocessor-based systems now offer facilities for direct support of multiuser/multitask environments and sophisticated operating system implementations. The current single-chip, 16-bit microprocessors are the following:

* the 8086 (iPAX 86) : designed by Intel;
* the Z8000 : designed by Zilog;
* the MC68000 : designed by Motorola;
* the TMS9900 : designed by Texas Instruments;
* the NS16000 : designed by National Semiconductors.

Intel 8086

The Intel 8086 is implemented in *n*-channel depletion load silicon gate technology (HMOS) and packaged in a 40-pin cer DIP. It is designed to be upward compatible with 8080. The internal functions of the processor are partitioned into two processing units: Bus Interface Unit (BIU) and Execution Unit (EU). These units can interact directly but for the most part perform as separate asynchronous operational processors. The overlap of instruction prefetch provided by the BIU serves to increase processor performance. Upto 6 bytes of instruction stream can be queued while waiting for decoding and execution. The execution unit receives prefetched instructions from the BIU queue.

The Intel 8086 execution unit contains four 16-bit general data registers that are also addressable as eight 8-bit registers. In addition, it has two 16-bit memory base pointer registers and two 16-bit index registers. These eight registers are used implicitly by the instruction set, providing compact encoding at the cost of reduced flexibility. The BIU contains one 16-bit instruction pointer, which contains the offset of the next instruction to be fetched. The BIU also contains four 16-bit dedicated segment registers for segment base addressing, which enables programmes to access upto four 64 k byte segments at a time. Finally, the EU contains six one-bit status flags and three one-bit control flags.

The 8086 processor provides a 20-bit address to memory which is logically organized as a linear array of 1 M bytes. The one megabyte of real addressing space in the 8086 is treated as a group of segments, each segment 64 k bytes in size. Four segments are addressable at one time, providing upto 64 k bytes of code, 64 k bytes for stack and 128 k bytes for data. Physical addresses are generated by shifting the segment base-value four bits to the left and adding the offset.

The Intel 8086 has 64 k byte (32 k words) separate I/O space. A memory-mapped I/O capability that can respond like a memory device is available for linking I/O devices. Intel also offers the 8089 IOP, an independent processor with two DMA channels and an instruction set tailored for I/O operations.

As already mentioned, the 8086 is an improved and expanded version of the 8080. The 8080's basic eight-bit instructions have been retained, and expanded with extended instruction lengths when necessary. For efficient code, the instructions most often executed are only one byte long. Implied register addressing also reduces code size. To allow for expansion of the instruction set, an "escape" facility is available for transferring control to a coprocessor. The addressing highlights of the 8086 include the ability to finely segment memory, and the

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facilities for indexing with displacement and without displacement.

The Multibus is the structure for interfacing Intel's 8080/85/86 products. It supports 1 M byte address space. The 8289 bus arbiter controls multibus access by multiple masters. The control lines are designed according to a master-slave concept. Co-ordination features of the 8086 multiprocessor include:

* the bus lock signal, activated on execution of lock prefix instructions, blocking interrupts and requests by other processors until the lock sequence is completed;
* the semaphore using the lock prefix in conjunction with the XCHG instruction;
* synchronization to an external event using a WAIT instruction and the test input signal.

Zilog Z8000

A register-rich 16-bit processor, the Z8000 is not an enhancement of Zilog's Z80 family and has a different internal structure. The Z8000 is fabricated with high density, high performance scaled *n*-channel silicon gate depletion load technology. The Z8000 is available in two versions: the Z8001 48-pin segmented and Z8002 40-pin nonsegmented. The main difference between the two is in the addressing range. The non-segmented Z8002 has an address space of 64 k bytes. The segmented Z8001 address consists of a 7-bit segment number and 16-bit offset and so the direct addressing range of 8 M bytes. The 16-bit ALU manipulates data and generates logical offset addresses in the general-purpose register block in accordance with the instruction executed. The CPU status and control flags are maintained in the programme status registers, and the CPU, which can operate in a system mode or normal mode, can execute privileged instructions only in the system mode. A refresh counter provides the refresh control logic with timing information for CPU-driven memory refresh operation.

The Z8000 is characterized by sixteen 16-bit registers. The first eight of the 16-bit registers can be used as sixteen 8-bit general purpose registers. All the registers may be used as accumulators and all but one as index registers or memory pointers. The general register architecture avoids bottlenecks inherent in dedicated or implied registers. Two registers are used as implied stack pointers for system mode and normal mode. All Z8000 family chips contain one 16-bit segment offset register, and the Z8001 also contains one 16-bit segment number register. The Z8001 also cont is a 16-bit register, two 16-bit registers as programme status area pointer, one 16-bit flag and control register, and one 16-bit refresh counter.

The eight megabytes of directly addressable memory is split up as 128 segments, each of 64 k bytes. The 23 address lines (on the Z8001) provide a seven-bit segment number and a 16-bit segment offset pointer. The two address parts can be manipulated separately or together by all the available word and long word operations. The CPU generates processor status information, which enables the address range to be increased beyond its nominal limits by physically separating code, data and stack spaces in system and normal modes (6×8 M bytes=48 M bytes). External logic is needed for this memory extension. The Z8010 memory management unit, or MMU, can be used with the Z8001 microprocessor to improve and expand memory addressing capabilities, randomly relocating all 128 segments in the six address spaces with translation tables for each space.

The Z8000 family CPUs support two different I/O address spaces of 64 k bytes through special I/O instructions, which can be executed only in the system mode. Standard I/O instructions transfer data between the CPU and peripherals, and special I/O instructions transfer data to and from external CPU support chips. Processor status information enables separation of address space.

Code is space-efficient because the instructions most often executed are shortest in lengths and because it distinguishes between long branches and short branches. Unlike the 8086, it does not use implied registers. The instruction set facilitates multiprogramming through context switching facility. Other instruction highlights include signed 32-bit multiply and divide, decimal operations, multiple load, string manipulation instruction and the test and set instruction, which is especially valuable in multiprocessor applications. Addressing schemes include indexing with and without displacement, and multiple increment indexing. Multiple stacks, segmented memory and the very large space (48 M bytes) ease programming effort. The user/supervisor stacks are hardwired.

The following are some of the features which facilitate the multimicroprocessor-operation:

* four special, privileged "multimicro" instructions-MBIT, MREQ, MRES and MSET;
* pins for the bus request, bus acknowledge, multimicro-in multimicro-out, and segment trap;
* test and set instructions.

Motorola MC68000

The MC68000 is a 64-pin new generation VLSI microprocessor implemented in high-density *n*-channel silicon gate MOS technology. The control of the MC68000 is implemented by two-level microcode. The CPU may run in either a supervisor mode with privileged instructions or in a user mode. Although internal data paths are all 32-bit wide, the packaging limitation on the number of pins constraints data paths to and from memory to be only 16-bit wide. Of the 64-pins, 23-pins are for address bus and 16 for data bus. The chip specifications provide

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Table 1. *SPECIFICATIONS OF 16-BIT MICROPROCESSORS*

Feature	8086	Z8000	68000	9900	16008/16016	16032
Year of commercial introduction	1978	1979	1980	1975	1981	1981
No. of Basic Instructions	95	110	61	69	100	100
No. of General-purpose Registers	14	16	16	16	8	8
Pin count	40	48/40	64	64	40	48
Direct Address Range (Bytes)	1 M	64K/48M	16M/64M	64K	64K/16M	16M
No. of Addressing Modes	8	8	14	8	9	9
Basic clock Frequency	5 MHz (4-8 MHz)	2.5-3.9 MHz	5-8 MHz	3.3 MHz	10 MHz	10 MHz
Microprogrammed	Yes	No	Yes (two level)	No	Yes	Yes (two level)
Bus structure	Multiplexed data/ address bus	Multiplex data/ address bus	Separate address (24) and data (16) buses	Separate address (15) and data (16) buses	?	Multiplexed address/data bus (24)

for floating-point and string operations, but the current versions do not have these features because of technological limitations on circuit density and size.

The MC68000 has eight 32-bit data registers, seven 32-bit address registers, and two implied 32-bit stack pointers. The data registers can be addressed as byte registers, word registers, or double word registers. The address registers are used for 32-bit base addressing, 32-bit software stack operations, and word and long word address operations. The MC68000 also contains a 32-bit programme counter and 16-bit status register. The programme counter addresses one large linear address space from a full 32-bit address, but only 24 bits are available in the present version.

The MC68000 has 23 address lines, providing a 16 M byte address capability. The address is linear with no internal segmentation. Similar to that of the Z8000, the processor status information separates address space into four areas: the supervisor programme, the supervisor data, the user programme, and the user data. The proposed memory management unit, MC68451, would support sophisticated management and protection of 32 variable sized segments, ranging from 256 bytes to 16 M bytes in increments of 256 bytes and would allow trapping of unauthorized accesses.

The MC68000 possesses no separate I/O space. All I/O is memory-mapped and all I/O protection must occur at the memory protection level. The CPU has been designed to operate in conjunction with the MC68450, which will allow block transfer rates upto four megabytes per second.

The MC68000 has a regular instruction set and provides multiuser support. It emphasizes space efficient code through 'thick' instructions and short jump on loops. Context switching facilitates multiprogramming, and the test and set instructions aids in multiprocessor and database applications.

MC68000 multimicroprocessor operation is facilitated by

* bus arbitration modules (BAMs), which provide support in global multiprocessor design;
* the TAS (Test and Set) instruction.

TI9900

The TMS9900 is a single chip 16-bit processor using silicon gate MOS technology and it is an implementation of the TM 990 series minicomputer CPUs. The TMS9900 is packaged in a 64-pin DIP. It has a separate 15-bit address bus and 16-bit data bus. There are three registers on the 9900 chip, they are the work-space pointer (WP), the programme counter (PC) and the status register (SR).

The 9900 utilizes a memory to memory architecture that provides workspaces of sixteen 16-bit registers in the memory for each level of interrupt or subroutines. This workspace concept is valuable for applications requiring frequent servicing of interrupt and context switching. In the conventional register-to-register architecture, a context switch requires storing and reloading of contents of registers, whereas the workspace register systems exchange the contents of PC, WP, and SR so that the 9900 can accomplish a complete switch in one instruction. Similar time saving occurs on return to the original routine. However, this time saving is accompanied by slower register access times because the registers are in the main memory as opposed to residing on the processor chip.

The address space of TI 9900 is 64 k bytes. The 9900 is not intrinsically a stack-oriented machine. Handling of stacks and stack pointers requires one extra instruction for one of the complementary stack operations because there is no autodecrement addressing mode.

A unique capability of the 9900 is the direct command driven communication register unit (CRU). It supplies upto 4096 directly addressable bits each of input and output. I/O bits can be addressed individually or in fields of 1 to 16 bits.

This processor has only unsigned multiply and divide instructions. In addition to memory mapped I/O, it

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has separate I/O instructions for the CRU which makes interfacing slow devices quite convenient. The TMS 9900 was the first 16-bit microprocessor and therefore, the facilities provided are less compared of the other 16-bit microprocessors.

National 16000

The NS16000 family of processors are developed by National Semiconductor implemented with 3.5 micron gate technology. The 16000 series consists of the NS16008, NS16016, and NS16032 processors. Of these, the NS 16008 and the NS16016 are very similar, each offering an internal data ALU bus 16 bits wide and a direct addressing range of 64 k bytes. Further, either of these two chips can operate in two distinct modes:

(*i*) native mode, in which the two processors have 100 basic instructions and are directly compatible with the NS16032;

(*ii*) 8080 compatibility mode, which permits direct emulation of the 8080, with a speed four times that of the 8080.

The NS16008 and NS16016 processors are designed to bridge the gap between the 8080 and the high-end members of the NS16000 family. NS16008 and 16016 have 16-bit address pointers that are upward compatible through software to the 16032 address space. The primary difference between them is that the NS16016 has a 16-bit data bus, whereas the NS16008 has only an eight-bit data bus.

The architecture of NS16000 family supports 16 registers forming two register files: eight 24-bit dedicated registers and eight 32-bit general-purpose registers. The NS16081 floating point unit, or FPU, has an additional set of eight general purpose registers, supplementing the GPRs on the master processor.

The NS16032 achieves an address range of 32 M bytes by means of a memory management unit (16082) or MMU. It has a direct address range of 16 M bytes using 24-bit address pointers.

The NS16000 family offers several symmetric addressing modes, including top of the stack addressing, memory relative addressing, external addressing and scaled addressing. In addition to conventional CPU instructions, the architecture includes advanced instructions that are useful in an HLL environment. The CHECK, INDEX, STRING, CXP, ENTER and EXIT are some of the instructions for this purpose.

The IN 'ERLOCKED instructions (test and set/clear) provide interlocked semaphore primitives for multitasking and multiprocessing co-ordination.

PERFORMANCE ISSUES

The operational speeds of all the 16-bit microprocessors have improved over the previous generation 8080, Z80 and MC6800 processors. In the 16-bit microprocessors, extended address ranges allow large memory sizes directly to be accessed. Large memory space requires some form of management. The internal segments of the 8086 provide internally-controlled memory management via relocation. The other processors Z8000, MC68000, NS16032 are designed to be used with an external memory management chip. The Z8000 is best suited for word processing and text editing applications because of its sophisticated string instruction repertoire. The MC68000 design supports high-level languages at both compilation time and execution time with a set of special-purpose instructions designed to manipulate run time environment of a high-level-language programme. The NS16000 architecture is designed to support high-level languages, such as Pascal, Ada, and Fortran. Its architectural features increase the efficiency of HLL compilers to generate compact code, and special emphasis has been put on modular programming. Since the TMS9900 was more or less the first 16-bit microprocessor, its architecture does not support the features provided by the other processors. However, TMS99000 microprocessor announced by the Texas Instruments is a 24 MHz version and is microprogrammed. The microcode, with 152-bit-wide words, can increase the overall processing throughput by 9 to 12 times over that of comparable TMS9900 microprocessor. There are also corresponding improvements in clock rates for other processors.

COMPUTER PROCESS CONTROL

An understanding of the role of microprocessors in process control needs an appreciation of the application of digital computers to process control. The usage of digital computers to process control is now well established. Moreover, the rising energy costs and limited availability of raw materials have placed unprecedented demands on the process control systems.

A typical computer process control system can be described by the functional block diagram as shown in Fig. 1 [4]. The three functions required of the control computer are:

(*i*) *Estimation:* The ability to predict, using a mathematical model for the process, some of its dependent variables that cannot be directly measured;

(*ii*) *Optimization:* The ability to determine an optimum operating condition with respect to an economic objective function;

(*iii*) *Control:* The ability to set process variables such that the optimum operating condition, determined in (*ii*), is continuously maintained.

When the above three aspects of a process control problem, *viz.*, estimation, optimization and control, are considered as a whole, the computer becomes attractive. Using a programmable control computer, as opposed to

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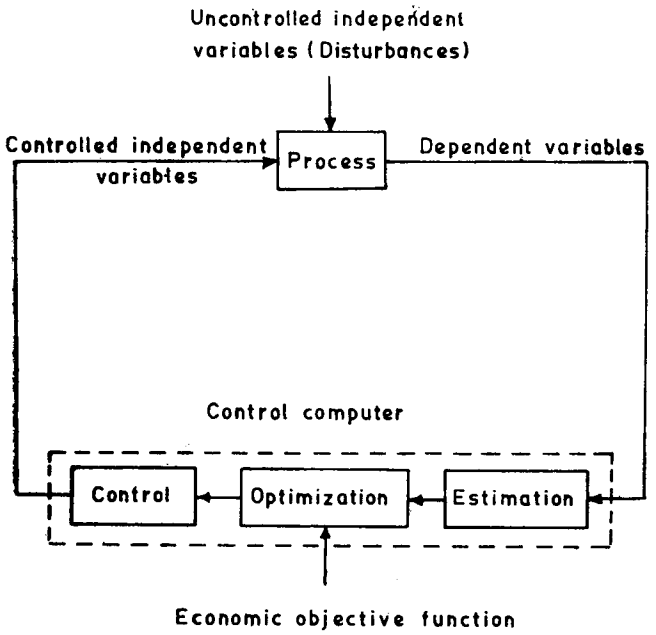

Fig. 1. Functional block diagram of a computer process control system

hard-wired systems, provides for flexibility in design by permitting:

(*a*) the tuning of a system by adjusting model parameters;

(*b*) the changing of the model, the estimation, optimization and control algorithms without drastic alteration to the original system.

Also, with a control computer, improved regulation of key process variables can be achieved. This can generate tangible benefits because [5]:

(*i*) the magnitude of the variation of the key variables is reduced;

(*ii*) the reduced variation permits moving the mean value of the key variable closer to an operating point; or

(*iii*) both of the above.

In computer control systems, we perforce deal with discrete information on a sampled basis. The sampled data control concepts and techniques are well developed and have been used effectively for the analysis of control systems involving digital computers.

Adapting process models to microprocessors

The microprocessor has brought with it many advantages like higher reliability, smaller size and light weight, easy maintenance, cost reduction and low power consumption. Because of these advantages, the microprocessor is replacing and enhancing dedicated analogue units. The full benefits can be realized only after altering the structure of the overall control system. In addition, they bring with them the problems of standardization in hardware, software, interconnection protocol and levels of modularization.

To appreciate the role of microprocessors, one should not only understand the application of a digital computer in process control but also appreciate the process control environment as a whole. The basic control loop in conventional (analogue) systems is the simple feedback loop. The value of the controlled variable is detected by a sensor or transmitter. This value is compared to desired value of set point to generate the error. The control law generates a change in the manipulated variable so as to drive this error to zero. This controller output is imposed on the process by an actuator, which is an automatic positioning valve in many cases (process control). The control law commonly used is the PID relationship or some simplification thereof. Conventional analogue control systems basically suffer from inflexibility [14].

In Direct Digital Control (DDC) the computer calculates the values of the manipulated variable directly from the values of the set points, control variables and other measurements on the process. The decisions of the computer are applied directly to the process and hence the name DDC. A typical microprocessor based DDC system is shown in Fig. 2. As the values of the manipulated variables are calculated by the computer, the conventional three-mode controllers are no longer needed. Their functions are instead performed by the equations, called algorithms by which the computer calculates the manipulated variable from the set point and controlled variable. One of the first incentives suggested for DDC is that the computer can provide the same function as several analogue controllers. Jacobs has given the following advantages of a microprocessor-based process controller [8].

1. Increased flexibility in the design, modification and expansion of the control system.
2. The capability for interactive communication with other controllers or monitors.
3. Automatic logging or display of process status and data.
4. The detection of abnormal condition and execution of discrete emergency shut down procedures.

In a large petroleum refinery or petrochemical complex, it might be required to handle upto 1500 to 1800 analogue inputs and an equal number of digital signals [7]. Sampling of analogue input information from chemical and petroleum type plant is as follows:

60 per cent	once per second
15 ,,	once per five seconds
25 ,,	once per twenty seconds.

It is anticipated that there will be process industry requirements for computers in sizes equivalent to the following number of control loops [7]

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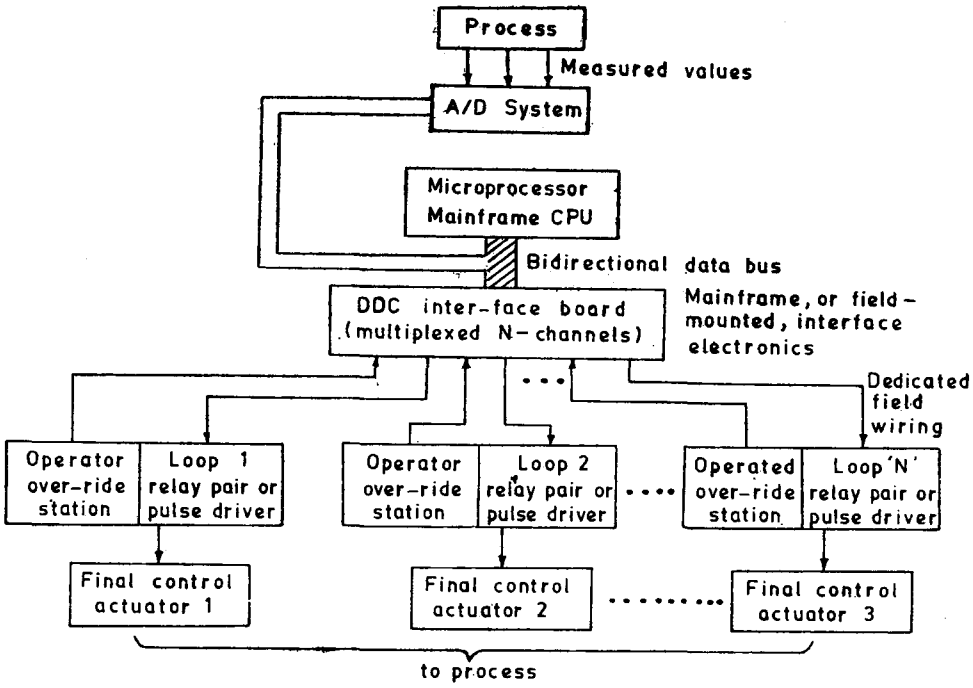

Fig. 2. A microprocessor based direct digital control system

16 loops
32 loops
64 loops
128 loops
256 loops.

Greatest demand should be for the three medium sized machines with somewhat less interest in the very large or very small sizes.

In supervisory control, the computer monitors data and computes the set-points of all the controllers. A microprocessor-based supervisory control system is shown in Fig. 3. For all control interfaces, there should be computer fail-safe system to disconnect all computer outputs in case of a computer malfunction and switch the system to manual control.

Digital control algorithms

Algorithms have been designed to suit microprocessors. One of the aims of modern digital control algorithms is that the on-line control computations must be simple and

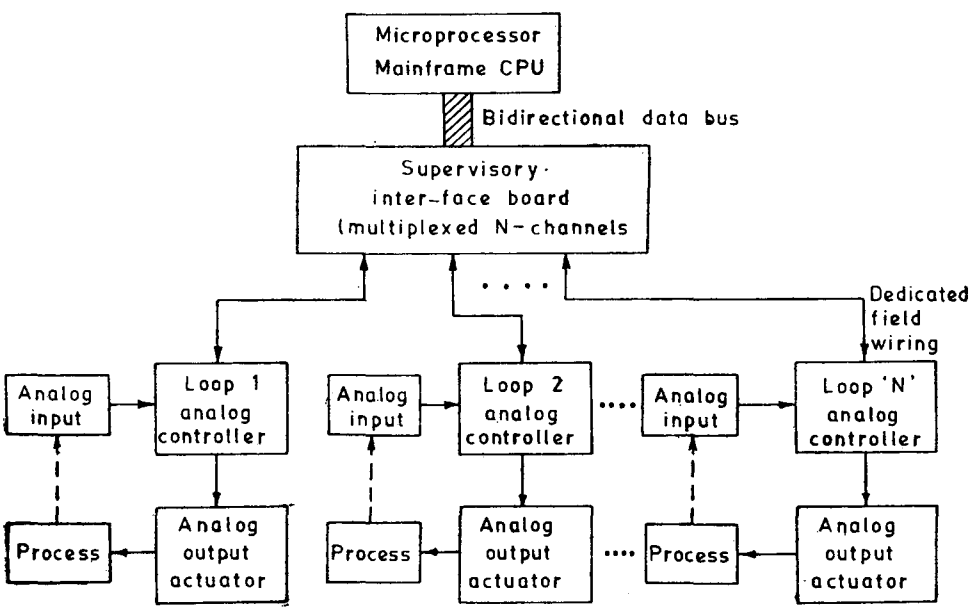

Fig. 3. A supervisory control interface

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fast, preferably involving neither transcendental functions nor iterations. Standard estimation problems are reformulated and solved leading to algorithms which are easy to implement on microprocessors [2].

A digital control algorithm for single loop system was developed by Auslander [1]. The equations for finite time settling observer (FTSO) and for finite time settling controller (FTSC) are given by Auslander. These equations have been developed to make the on-line control computations simple and fast so that they can be implemented on a microprocessor. Digital filter techniques are employed where conventional analogue filters become impractical.

Sinha *et al.* had investigated the application of minicomputer for the on-line estimation of the parameters of a two-stage heat-exchanger from the samples of the input/output data with the system under operation [13]. The objective of the investigation was to consider the application of the on-line identification methods to the estimation of the parameters of the dynamic model of an actual industrial process in real-time employing a minicomputer. Therefore, the 16-bit microprocessors can be considered for implementation of on-line identification of chemical processes.

Kalman filtering is a popular method of estimating states from noisy measurements. Computational time per iteration establishes meaningful data sample rates. Singer [12] had derived an optimal Kalman filter, for tracking of manned manoeuverable vehicles, using a target model that is simple to implement and that represents closely the motion of manoeuvering targets. The Kalman filter equations can be implemented on the 16-bit microprocessors.

Even though effective algorithms have been developed to calculate the optimal control policies, for dynamic systems, the solution of many classes of optimization problems, especially those with non-linear and distributed parameter characteristics still require excessive computation time and when these algorithms are applied. Suboptimal control is an attempt to approximate the solution to these problems with a reduced amount of computer storage and computer time. From a chemical engineering point-of-view, the use of suboptimal control is justified for these problems where the performance index to be optimized is not sensitive to small perturbation in the control policy.

Burrows had investigated the application of a dedicated microprocessor to suboptimal excitation control of an a.c. turbogenerator [3]. Attempts are being made to apply modern control and microprocessors to the power electronics field.

With the prices of microprocessors declining steadily, it is now possible and economical to implement sophisticated control strategies.

PROCESS CONTROL APPLICATIONS

Process control continues to receive attention in view of the more expensive raw materials, increasing costs of energy. With man power availability a critical factor, there will be continuing demand for simple systems that are easy to understand, operate and maintain. Therefore, an over-riding consideration regarding control systems in the chemical process industries has been simplicity.

One major area where the microprocessors have made significant impact is sequential control. Programmable logic controllers (PLC) are designed to perform sequencing operations by first scanning inputs such as relay contacts, limit switches, push buttons, valves, etc. then comparing the inputs to the conditions specified in the programme, and finally by energizing or de-energizing outputs in accordance with the programmed instructions. Microprocessors are used in PLCs. In our country, organizations like ECIL, KELTRON have introduced PLCs into the market.

Data acquisition/Alarm annunciator systems are also developed based on microprocessors. Organizations like KELTRON have developed temperature scanners. As far as digital controllers are concerned, we have yet to make a beginning. Microprocessors have enabled the process control designers to move over from large graphic panels incorporating meter dials and indicators and annunciator dials to the colour graphic displays.

In addition to DDC and supervisory control, a new control technology, distributed digital control (DiDC) has assumed importance. Distributed process control systems are collections of computing or information processing elements connected by communication links. The elements may range from controllers to optimizers or operator interface drivers located in supervisory areas. The primary advantages are the flexibility to configure highly modular systems to changing needs, and the reliability offered by autonomy of processing elements. The main problems of distributed control are the difficulty of interfacing and coordinating separate elements. Effective exploitation of microprocessor technology to distributed control calls for a systems approach to tackle the problems of communication between elements, reliability, flexibility and co-ordination.

As the hardware costs are going down, the software development costs are going up. A major obstacle in using computers in process control has been development and preparation of applications software. For this reason, emphasis was placed on languages like FORTRAN or BASIC, as opposed to assembly languages. Several attempts have been made to develop control-oriented languages through which the control engineer can quickly obtain the desired control functions from the computer system. Many variants of FORTRAN for real-time applications have appeared. The I/O operations in these languages are achieved with facility to link assembly language routines. However, the fill-in-the-forms language had become most practical. The major problem in implementing a real-time language is the overhead involved.

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Real-time languages like MODULA, concurrent PASCAL are developed based on the highly typed and structured language like PASCAL. They have yet to make an impact in process industries. The software for a distributed process control system will be quite different from that for a single processor system. It is to be seen how the language Ada will be received by the process control community.

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