Development of Characterization Circuit for Power Semiconductor Devices

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***Abstract*—Researchers have come to rely heavily on I-V Characterization as a means of evaluating power semiconductor devices' ON - state performance and performing real - time condition monitoring. However, because of their high cost, intricate operation, and possibility for errors at various setup phases, the current SIVC systems can be difficult to deploy in laboratory settings. Even though certain commercial items function exceptionally well, their high cost can often make them difficult to get. In this manuscript, a simple, precise, and economical characterization configuration is presented to deal with these problems. Conventional standards for testing discrete power device parameters may not adequately address the demands of high-power applications. In-circuit or in-situ testing methods are proposed as more suitable, allowing devices to be tested at full power and stress, mimicking real-world operation. Introducing a class of switch-mode power electronics circuit topology called Energy Recirculating and Storage Circuits, this approach enables high-power device testing with a low-power source, eliminating the need for a load. The ERSCs, derived from two-port power converters, demonstrate the ability to recirculate and store energy, simulating a higher power source. The thesis establishes ERSCs as a new switch-mode power electronic circuit classification, providing a method for their construction and synthesizing a family of ERSCs from buck and boost-derived converters. Simulations validate the proof of concept and circuit operation.**

Keywords—I-V Characterization, High-Power Testing, In - Circuit Testing, Energy Recirculating and Storage Circuits (ERSCs)

I. Introduction

Researchers use Static I-V Characterization (SIVC) as a vital method to evaluate power semiconductor devices' ON-state performance. It makes it possible to estimate important factors including these devices' transfer characteristics, threshold voltage, ON-state resistance, and ON-state voltage-current relationship. As seen in Fig., SIVC is essential to many research applications. 1, encompassing.

Derivation of ON-State Loss Model: SIVC is used by researchers to create ON-state loss models for power semiconductor devices, which are essential for figuring out conduction losses. Design and Development of Devices: SIVC assists in the creation of novel devices. For example, SIVC is necessary for the production of high - power SiC diodes.

The manufacturing maturity of SiC-based MOSFET power modules is demonstrated by their near alignment with datasheet values under changing gate voltages and temperatures, as demonstrated by their characterisation.

Evaluation of Device potential: For medium and high voltage applications, SIVC evaluates the potential of a range of SiC-based devices, including SiC supercascode, SiC, SJT, SiC, n-IGBT, and SiC DMOSFET [3-6].

Condition Monitoring: By measuring the ON - state voltage drop of power semiconductor device, researchers frequently use SIVC to monitor their condition [7-9].The precision of SIVC is crucial in each of these applications for dependable outcomes and insightful knowledge about power semiconductor devices."

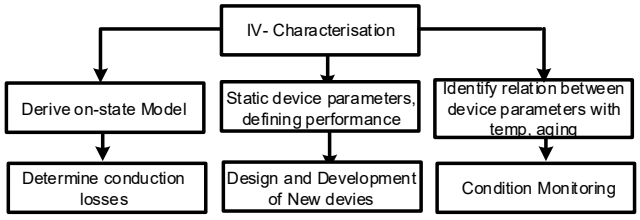

Fig. 1. SIVC Applications.

II. Existing Methods And Challenges

The Single - Pulse Test Circuit (SPTC) and Electrical Measurement Unit (EMU) make up the SIVC setup. This setup includes a pulse generation circuit responsible for producing voltage or current pulses of varied intensities for Device Under Test (DUT). The scaled outputs from these

circuits for measuring are sampled by the Analog-to-Digital Converter (ADC) module in the DAS. The chosen components undergo processing to determine the precise voltage and current across the DUT. The cumulative error in the SIVC setup arises from the aggregation of errors within these three individual components. The ideal SIVC setup should minimize errors to satisfy the application's requirements while still being economically viable.

Commercial curves tracers like the Tektronix TEK371A and Keysight B1505A are available for SIVC and provide an integrated solution for data acquisition across the DUT, pulse generation, and displays static characteristic result [10–12]. Although these curve tracers are highly accurate and quick to perform, their high cost prevents them from being used widely. Moreover, they cannot be used to simultaneously characterize multiple DUT.

There is an increasing need for economic solutions that use discrete and inexpensive components to build SIVC setups. In [13] introduced an isothermal SIVC configuration utilizing a microcontroller, featuring a self-developed I-V measurement unit and a pulse generation unit based on a DC power supply in the laboratory. This manuscript suggests using short-duration voltage pulses for isothermal I-V measurements, but it doesn't go into detail about how to choose the frequency and duration of the pulses, nor does it describe the various units and the associated characterization errors.

To achieve isothermal SIVC of DUT across various temperatures, [8] and [9] present current pulse - based methods for SIVC of semiconductor device, which describe the development, and operation of current pulse generation circuits. These circuits offer simple operation, but they do not include information on the technique for voltage and current measurements or the DAS.

III. Synthesis Of A New Class Of Converter That Utilize Energy Recirculation

A. *Synthesis of ERSCs*

The foundational configurations employed in all Energy Recirculation and Storage Circuit systems are ladder-structured buck-boost derive DC/DC switch-mode power converters with two ports. In order to establish a system that can both store and recirculate energy, particular topologies are generated through the following processes: Reducing the size of two-port power converters to single-port setups, matching port characteristics, and directly connecting the input to the output without any load. By integrating recirculated energy into the input, a more powerful source is emulated. When employing techniques to reduce ports, understanding the characteristics of both input and output ports is crucial. Typically, the input section includes an active switch and a power source. This source can be either real or an equivalent source providing constant current or voltage. For instance, an equivalent current source can be produced by connecting a real current source in series with a large inductor, or by connecting a real voltage source in parallel with a sizable filter capacitor. Most input sources used in practical applications are either equivalent current or real voltage sources. This article explores the precise relationship between equivalent resistor-controlled sources (ERSCs), examining all four common types of input sources found in input sections.

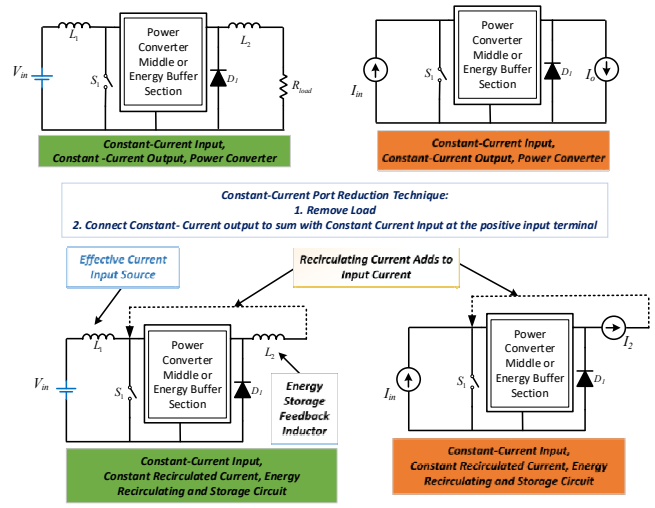

Fig. 2. Constant-Current Port-Reduction.

ERSCs employ a method to overcome the limitations imposed by the constraints of voltage and current in real sources. This involves recirculating and storing energy. The input and output terminals can display either constant current or constant voltage traits. Many converters have constant current output, although this is often concealed by adding a filter capacitor in parallel with the load, causing constant voltage output. To ensure precise duality among ERSCs, capacitors typically used as filter elements for constant current outputs are excluded.

B. *Synthesis of ERSCs*

When there is no demand, an energy recirculation and storage circuit (ERSC) is formed by linking the output back to the input. This particular arrangement permits the converter to function ordinarily when the load is present, while simultaneously recirculating and storing a portion or the entirety of the energy that is customarily supplied to the load. Consequently, the converter's total energy management is enhanced by the recirculated energy, contingent upon the fulfilment of two topological prerequisites.

A usual connection point between the input and output terminals is an absolute necessity. It is essential to remember that connecting the opposite polarity terminals of two ports on ladder-structured, non-transformer isolated converters is not feasible. Alternatively stated, if the input port displays characteristics of constant voltage, then the output port must also display such characteristics.

When both of these topological conditions are met, it becomes feasible to create two separate links between the input and output ports, determined by the electrical characteristics of the matched ports.

Constant Current Characteristics: When matched ports maintain a constant current electrical characteristic, the port-reduction method depicted in Fig. 3 is utilized. This involves

combining the current at the positive input terminal with the output current using Kirchoff's laws. Consequently, the energy that would typically be discharged to the load is retained in the feedback inductor of the ERSC. Due to the current passing through the feedback inductor, the energy that accumulates in the inductor over time increases, thereby augmenting the overall power managed by power circuit and generating impression that the input source is being increased.

Constant Voltage Characteristics: The port-reduction technique depicted in Fig. 4 is utilized when the electrical behavior of the matched port remains consistent. This approach ensures compliance with Kirchoff's laws by connecting the input and output voltages in series. To achieve this, the input source, whether real or simulated, is disconnected from the negative input terminal and linked to the positive output terminal. Consequently, the energy previously directed to the load is now stored in a feedback capacitor. This energy accumulation assumes constant source power and buffer energy. The increase in capacitor voltage enhances the circuit's power capacity, creating the impression of amplified capabilities in the input source.

Cascade Boost/Buck ERSCs: The ERSC configuration with cascaded boost/buck can have fewer ports by using the constant-current port-reduction technique, as depicted in Fig 3. Fig 5 illustrates the synthesis process of the cascade Boost / Buck ERSC. By cascading the boost converter and buck converter, a Cascaded Boost/Buck ERSC is produced.

Cascade Buck / Boost ERSC: The ERSC depicted in Fig 6, which combines a buck converter with a boost converter, can be seen as the dual of the previously mentioned ERSC. This configuration forms a voltage-current-voltage structure where voltage is manipulated using the constant-voltage method, as shown in Fig. 3.

Single-Ended ERSCs: To achieve a port reduction, it's vital to incorporate transformer-isolated single-ended buck/boost and reverse converter designs. These single-ended ERSCs, depicted in Fig. 7, utilize two active switch states, contrasting with the four in two-switch configurations. Fig. 3 illustrates the boost/buck and fundamental single-ended boost/buck converters, displaying a reversal of output polarity concerning the input.

IV. Analysis Of The Cascade Boost/Buck Recirculation

Reference [19] provides a thorough description and analysis and of the four topologies depicted in Fig. 2. Below is a more detailed discussion on the Cascaded Boost/Buck Energy Recovery Switched Capacitor (ERSC) architecture and its utilization in power factor correction.

ERSCs are characterized by their energy-pumping behavior, which results in transients in all operational modes. As a result, the duty cycle is non-constant, which makes the direct application of state-space averaging approaches necessary.

For ERSC topology analysis unfeasible. In order to address this issue, the first generation of ERSCs uses a methodology based on the examination of incremental linear transitions of state variables.

The circuit's operation is simulated numerically under a few assumptions: that all ERSCs function in the continuous conduction mode, which makes the analysis process easier, and that there are small deviations in the voltage and current in the state equations that describe every switch state topology during switching cycles. It is also assumed that switching frequencies constantly exceed the natural frequencies that are inherent in each circuit, which allows the transitions in state variables to appear linear throughout the operation.

A. Cascaded Boost/Buck ERSCOperation

As illustrated in Fig. 3, the ideal Cascaded Boost/Buck Energy Recovery Switched Capacitor (ERSC) is characterized by three primary state variables: Cascaded configurations, as opposed to single-ended setups, involve four active switch states that manage energy storage in feedback and buffer components, along with the filter element connected to an effective input source. The current flow in the inductor functions as the effective current source, while the voltage across the capacitor serves as the energy storage mechanism. The current passing through the feedback inductor is also crucial. Detailed descriptions of all four transition states and their respective equations are provided below..

The functioning of the ERSC is investigated in three distinct modes, each of which is designed to permit regulated energy storage in one of the three primary components. These modes are summarized as follows:

Soft-Start Mode: The circuit commences in state A of Fig. 4, denoted as A, where V_C is exceeds or equal to the input voltage, V_S, and both i_1 and i_2 are set to zero. S_1 modulates the switch to increase the current, i_1, through input filter inductor, L_1, whereas S_2 remains "off," thereby maintaining i_2 at zero. As illustrated in Fig. 3, the modulation of S_1 causes a progressive increase in i_1 until it reaches its maximal average value. The rate at which i1 increases can be regulated, much like the operation of a conventional boost converter. This mode concludes upon reaching I1.

Charge Mode: By transitioning to S_1, the circuit preserves the mean value of i_1, which falls within a specified range of ripples spanning from $I_{1(MAX)}$ to $I_{1(MIN)}$. This procedure is repeated until V_c is equivalent to the specified value, V_c.

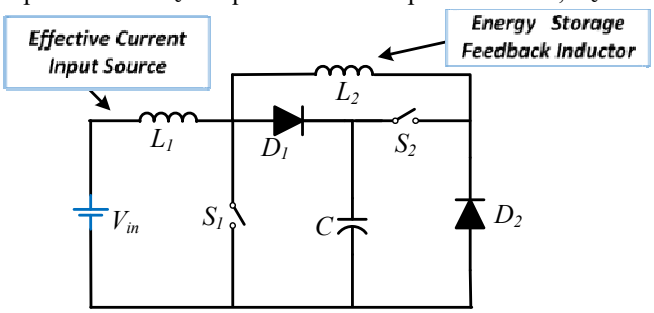

Fig. 3. Ideal Cascaded Boost / Buck ERSC.

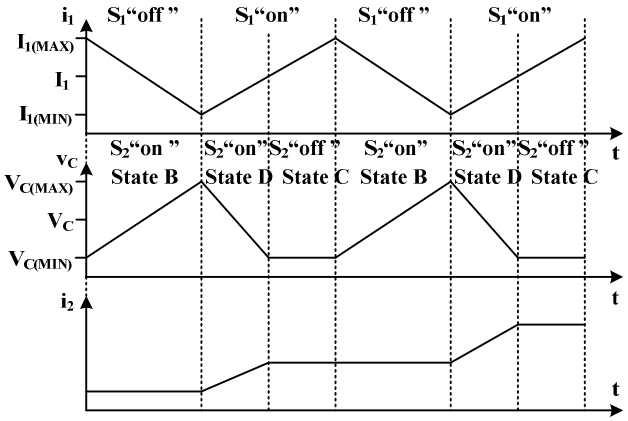

Fig. 4. Cascaded Boost / Buck ERSC Switching during Magnetize Mode.

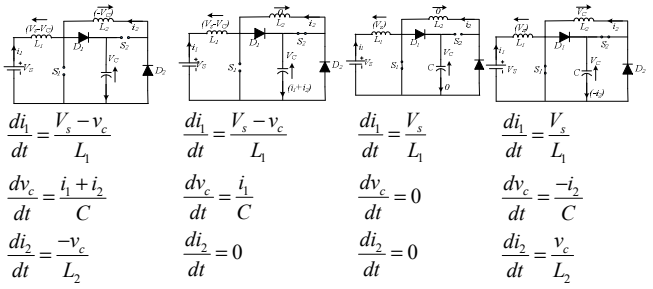

Fig. 5. Cascaded Boost/Buck ERSC Switch - State Topologies.

Charge Mode: The circuit enters charge mode upon attaining I_1. In this stage, the buffer capacitor is charged to a voltage defined by the user, denoted as VC (assuming VC was not reached during the soft-start mode). Charging occurs by regulating S1 through current-injection control, while S2 stays inactive to keep i2 at zero.

Magnetize Mode: The primary operating mode of the magnetize inductor is characterized by an increase in current from 0 to max levels. This is accomplished by adjusting S1 through current injection control and regulating S2 to ensure that the voltage across the buffer capacitor stays within specified upper and lower ripple thresholds., max V_C and min $V_C/2 = V_C$, respectively.

The switching phases of magnetize mode are illustrated in Fig. In order to maintain i_1 within predetermined ripple boundaries, S_1 is modulated independently from S_2 using the same current injection control strategy as the charge mode. The complex adjustment of S_2, which attempts to maintain V_C within predetermined lower and upper ripple boundary, is dependent on the S_1 state and the V_C value.

B. Cascaded Boost / Buck ERSCAnalysis

The design equations are formulated specifically for the magnetized mode. In order to find the duty cycle of S1, DS1, we substitute the constant variation in input current, denoted as, $\Delta I_1 = I_{1(MAX)} - I_{2(MIN)}$, into the equations representing state B and state D (or C) during the S1 switching cycle. This substitution yields the following results

$$t_{ON(S1)} = (\Delta I_1 L_1) / V_S \quad (1)$$

$$t_{OFF(S1)} = (\Delta I_1 L_1) / (V_S - V_S) \quad (2)$$

Combining (1) and (2) and equating L

$$D_{S1} = (V_C - V_S) / V_C \quad (3)$$

Rearranging equation (3) yields a formula to ascertain the voltage at which the buffer capacitor should be charged during the charging phase. The equation for V_C can be expressed as

$$V_C = V_S / (1 - D_{S1}) \quad (4)$$

To find the input filter inductance (L1) required for S1 in magnetize mode when a maximum switching frequency (fS1) is specified, you can calculate it by combining equations (1) and (2) and then solving for L1:

$$L_1 = [T_{S1}\, V_S\, (V_C - V_S)] / (V_C \Delta I_1) \quad (5)$$

The buffer capacitance must be adjusted to enable the voltage V_C to increase from its minimum value, $V_{C(MIN)}$, to its maximum value, $V_{C(MAX)}$, throughout the constant "off" duration of S_1, referred to as $t_{off(S1)}$. This adjustment is necessary to derive an equation representing the state of the buffer capacitance, denoted as B.

$$C = [I_1 \Delta I_1 L_1] / [\Delta V_C (V_C - V_S)] \quad (6)$$

where I_1 represents the mean i_1 value for state B.

As a result, the relationship between the total input energy, the energy in inductor, the maximum current $I_{2(MAX)}$, and the time duration is established by the equation above. During magnetization mode, all energy supplied by the voltage source is solely stored within the feedback inductor. To determine the total input energy, integrate the average input power over the operational period of the magnetization mode. This sum of input energy is equivalent to the energy stored in the feedback inductor at the conclusion of the magnetization mode when i2 has escalated from zero to a predefined maximum value,

$$I_{2(MAX)}.L_2 = (2 V I_1 t_m) / (I_{2(MAX)})^2 \quad (7)$$

It is crucial to acknowledge that the duty cycle, D_{S2}, of S_2 is in a dynamic state when in the magnetize phase. Initially, D_{S2} equals when i_2 is conducting lower current levels; consequently, the circuit never enters state C. As the value of i_2 progressively rises, S2 approaches 0.5, causing S_2 and S_1 to become out of phase, thereby reducing the duration of time spent in state D. As a consequence, the time allotted to state C is extended. When a circuit includes parasitic losses, the rise in i_2 stops once the average input power equals the losses of the circuit. This condition occurs during the magnetize mode, where all state variables remain unchanged. while defined boundaries for AC ripple occur, is commonly known as the "recirculate mode."

C. Applications of ERSC

This progress showcases the ability to assess power devices effectively at exceptionally high levels of power conversion, replicating the configuration of their final deployment, even when the circuit's input is supplied by a low-power source.

ERSCs have been utilized across various scenarios since their introduction as tools for on-the-spot evaluation of power.

VII. Simulations And Results

A. Simulation Results

The simulation waveform analysis of the energy recirculation and storage circuit yields compelling results, showcasing a remarkable performance characterized by high voltage and current levels the DUT. This outcome underscores the circuit's ability to harness and store energy beyond conventional input voltage constraints, indicating its potential for applications demanding elevated power levels.

The observed phenomenon in the simulation waveform signifies a successful energy recirculation process within the circuit. The efficient modulation of switches and controlled charging mechanisms contribute to the circuit's capacity to achieve and sustain high voltage and current levels. This result is indicative of the circuit's robust design, demonstrating its suitability for scenarios where augmented power capabilities are essential. The simulation outcomes not only validate the effectiveness of the energy recirculation and storage circuit but also suggest its potential in diverse applications requiring superior energy utilization and storage capabilities.

B. Soft-Start/Magnetize Mode

Soft Start Mode starts with state A, where both switches, S_1 and S_2, are turned off, and capacitor is pre-charged to a voltage (V_C) equal to or exceeding the input voltage Vs. The pre-charge can be achieved through an auxiliary charge circuit or by allowing a half-cycle of current to flow through L_1 and D_1 from V_S to charge capacitor C. In this initial state, the values of the three variables remain the same. During the soft start process, S1 is adjusted to gradually raise the current flowing through the input filter inductor, L1, while S2 remains inactive, thus maintaining i2 at a zero. Switching S_1 gradually raises the input filter inductor current, i_1, to its maximum value, $I_{1(MAX)}$. This incremental increase per switching cycle is achieved by keeping S_1 "on" longer than "off". The rate at which i_1 reaches $I_{1(MAX)}$ can be adjusted by controlling the difference between the on and off times of S_1, $t_{on(S1)}$, and $t_{off(S1)}$. The larger $t_{on(S1)}$ is compared to $t_{off(S1)}$, the faster i_1 reaches $I_{1(MAX)}$.

C. Charge Mode

When i1 reaches its maximum value, $I_{1(MAX)}$, the circuit enters a charging phase to charge the energy buffer capacitor. The duty cycle of S_1 in the subsequent operational mode is contingent upon the charge level of the capacitor, provided that the capacitor voltage, V_C, has not attained its intended level during the soft start process.

The process of charging the capacitor involves regulating the current injection to adjust S_1. By toggling S_1, the aim is to maintain a consistent average value, I, for i_1, with a ripple between $I_{1(MAX)}$ and $I_{1(MIN)}$. This relationship is expressed as

$$I_1 = [I_{1(MAX)} + I_{1(MIN)}]/2$$

Throughout this process, S_2 remains off to keep i_2 at zero. This switching cycle continues until the capacitor voltage, V_C, reaches the desired level, V_C.

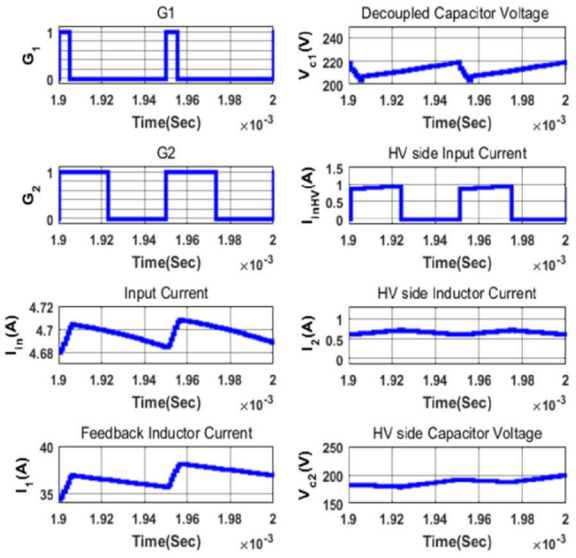

Fig. 6. Output waveforms in Soft-Start/Magnetize Mode.

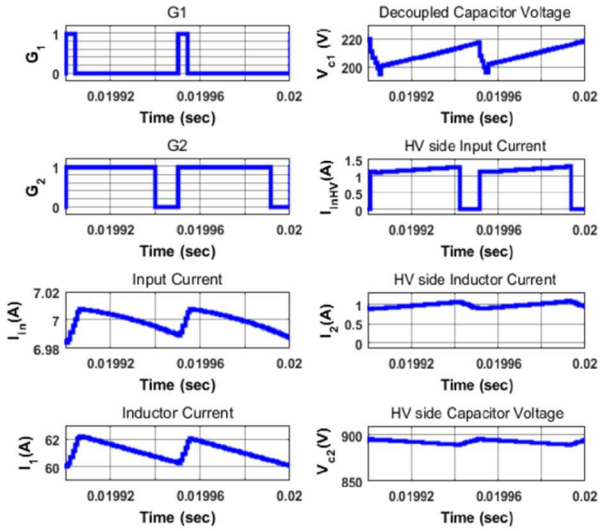

Fig. 7. Output waveforms in Charge Mode.

The process of charging the capacitor involves regulating the current injection to adjust S_1. By toggling S_1, the aim is to maintain a consistent average value, I, for i_1, with a ripple between $I_{1(MAX)}$ and $I_{1(MIN)}$. This relationship is expressed as

$$I_1 = [I_{1(MAX)} + I_{1(MIN)}]/2$$

Throughout this process, S_2 remains off to keep i_2 at zero. This switching cycle continues until the capacitor voltage, V_C, reaches the desired level, V_C.

After completion of the charge mode, the circuit moves into the "main" or magnetize mode. In this operating mode, the aim is to raise the current flowing through the feedback inductor gradually from zero to high levels. This is accomplished by employing current-injection control to modulate S_1, and S_2 is modulated to maintain the voltage across the energy buffer capacitor operating within specified

upper and lower ripple thresholds, $V_{C(MAX)}$ and $V_{C(MIN)}$, where $(V_{C(MAX)} + V_{C(MIN)}) / 2$ equals V_C.

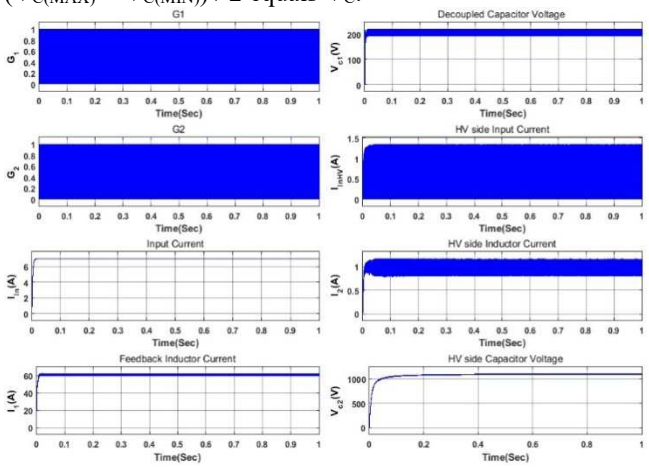

Fig. 8. Output Output waveforms.contingent upon the charge level of the capacitor, provided that the capacitor voltage, V_C, has not attained its intended level during the soft start process.

D. Energy Recirculation Mode

V_C represents an estimated value of the typical voltage across the energy buffer capacitor while in magnetize mode. It represents the maximum voltage that the capacitor reached during the charge mode. The modulation of S_1 and S_2 ensures a controlled increase in feedback inductor current and maintains the voltage across the capacitor within specified limits.

VIII. CONCLUSION

This manuscript presents a methodology for building and running a modular SIVC (Switching Interval Voltage Characteristic) setup that allows low-cost, precise testing of power semiconductor devices. This paper presents Energy Recirculation and Storage Circuits (ERSCs), an innovative category of power circuit topologies. Port reductions of DC/DC switch-mode power converters, in which the load is disconnected and the output is connected to the input in order to create pathway for recirculation, are the source material for ERSC. For ladder-structured constant – current - port and constant – voltage - port when connecting terminals of similar polarity between input and output, standard rules for port reduction are established. The manuscript addresses applications of ERSCs and analyzes ERSC to illustrate the idea and functionality of ERSCs for the characterization of devices.

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