AC-DC PFC-BOOST CONVERTER WITH RIPPLE REDUCTION TECHNIQUE FOR E-BIKE BATTERY CHARGING SYSTEM

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Abstract— E-bikes are fetching immense admiration in current market, because of miniature size, simplicity of charging at home and cost-effectiveness substitute in the segment of electric vehicles (EV). For charging the batteries of e-bikes, an ameliorate converter is suggested and is presented in this paper. Proposed converter has two stages. Each stage has a separate boost converter for achieving near UPF, low THD and low ripple in output voltage. First stage boost converter is to provide continuous power to e-bike battery and thereby maintaining near UPF and second stage boost converter is meant for ripple reduction in output voltage. To meet this standard criterion, only a minimal capacitance is required. First stage boost converter steers maximum amount of power through e-bike battery, whereas the second stage boost converter just steers a fraction of power through e-bike battery. In comparison to conventional converters, this proposed parallel architecture of boost converters ensures higher efficiency. A lithium-ion battery pack with 4500 mAh capacity, 100V fully charged voltage of battery pack, 86.12V nominal voltage of battery pack and 66V cut-off voltage of battery pack is utilized.

Keywords—Unity power factor (UPF); Total harmonic distortion (THD), Electric vehicle (EV), Electric bike (Ebike), Internal combustion engine (ICE), Discontinuous conduction mode (DCM), Ripple reduction (RR).

I. INTRODUCTION

Long-drawn-out, the vehicle industry has been using desegregated chip engines to power private and public conveyance systems. As a result of the extensive use of the crude oil sub product like petrol/gasoline, harmful emanations have caused major health risks as well as environmental damage [1]. Electric vehicles are majorly categorised in three categories, (1.) Fully electric vehicles, (2.) Hybrid electric vehicles and (3.) Fuel cell electric vehicles. Electric power is utilized to power the battery of fully EV and fuel-cell EV, however hybrid electric vehicles now on the market contain an additional ICE along with battery. Since in EV's, huge electric load charging & high-capacity batteries are required,

omnipresent acquisition of this concept will have noteworthy connotations on electric power system working & structure. However, EV's will have positive impact on environment as it will only utilize non-polluting energy resources [2], [3]. [4] & [5] indicate how electric vehicles are anticipated to modify energy requirement. [6] represents the economic implications for electric utilities. Conventionally, one-stage driver is employed to serve as both a PFC stage and continuous output current origin. It is seen that for low power applications as well as for medium power applications, flyback converter and buck converter demonstrate precise current regulation and admissible power condition data, like better PF & reduced THD. The loss-less resistance feature of boost converter running in DCM is employed to assure high power factor. The operation in DCM, on the other hand, enhances the electrical pressure on the converter elements. As a result, using a onestage driver, a trade-off must be created between achieving improved power quality & good efficiency. The dual-stage driver arrangement has been presented to meet the norms and mandates. A PFC level & a power control level in cascade make-up dual-stage drivers [7]. Despite the fact that dualstage converters have a lot of advantages, they also have certain disadvantages. For example, accommodating minimum 2 active switches, that entails 2 gate drivers & accompanying set-up, results in a larger size & greater cost [8]-[11]. Dual-stage converters which are basically the integrated converters are built using only one-active switch, provide a viable way to alleviate the above-mentioned limitations by requiring just single gate dive circuitry & offering reduced switching losses. As a result, they maintain the efficiency of dual-stage converters while keeping some of the benefits of one-stage converters [12]-[16]. Power quality requirements and mandates like PF, THD are resolved by the traditional integrated converters. They do, however, need the existence of huge ripple filter capacitance to meet flicker regulations. Therefore, parallel dual-stage converters are presented as a unique form to meet both improved quality of power and flicker regulations & mandates. It is made up of two stages: a PC stage that functions as a PFC stage & a RR stage. Going through various literatures, it was found that there is a lot of combinations of converters acting as PFC converter & ripple reduction stage converter. Flyback working as PFC with buck /boost as opposite stage converter. Buckboost working as PFC & buck converter working in parallel

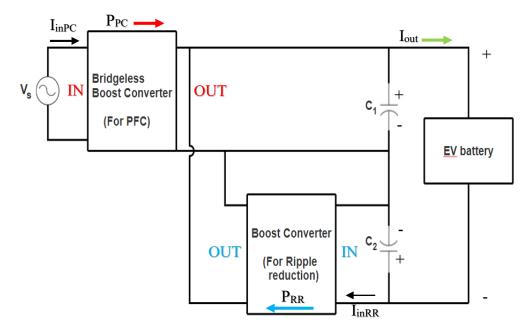


Fig. 1. Proposed converter block diagram

stage converter. The suggested converter is a unique amalgamation of boost converter for power factor correction stage & separate boost converter for ripple reduction stage. Initially the power is manipulated by the 1st stage, subsequently by the 2nd stage & then ultimately it is fed to the battery in case of standard dual-stage driver working in cascade mode. The suggested converter, on the other hand, includes PC stage, which is responsible for delivering the required power to the load. It also employs a RR stage, whose primary function is to eradicate output voltage ripple & this stage only handles a portion of output power. As a result, no girthy capacitor is required only the electrolytic capacitor -less driver will serve the purpose. The suggested converter is depicted in Fig. 1 as a block diagram, with boost converter in power control stage and another boost converter in ripple reduction stage. To eliminate output ripple, output voltage is calculated by knocking-off the ripple reduction stage input voltage from power control stage output voltage. Input voltage of ripple reduction stage will be polarised in the opposite direction of the power control stage. As a result, the low frequency ripple will be eliminated from the output, leaving only mean value.

II. PROPOSED CONVERTER WORKING PRINCIPLE

The two converters can be unified in order to maintain the same operational conduct and functionality. PC step boost converter is formed by L_1 , D_1 , D_2 , S_{1a} , S_{1b} , while the RR step boost converter is made by L_2 , C_2 , D_3 , S_2 .

A. Working of the first stage (PC-stage) converter

Operation of PC-stage boost converter is briefly discussed below-

Mode-I: Switch S_{1a} & switch S_{1b} are activated during this mode. Inductor L_1 gets energized during this mode. Therefore, to excite the boost converter inductance in PC-step, a current comes from AC grid & glides in boost input mesh. In inductor, current grows in a linear manner.

Mode-II: The switch-off of the main switches $S_{1a} \& S_{1b}$ initiates this mode. Inductor L_1 de-energize throughout this time frame.

B. Working of the second stage (RR-stage) converter

The suggested converter model is shown in Fig. 2. Operation of RR-stage boost converter is briefly discussed below-

Mode-I: Switch S_2 gets activated during this mode. Inductor L_2 gets energized during this mode. Therefore, to excite the boost converter inductance in RR-stage, a current comes from capacitor C_2 which is initially already energized & flows in boost input loop. In the inductor, current grows in a linear manner.

Mode-II: The switch-off of the main switch S_2 initiates this mode. Inductor L_2 de-energised throughout this time frame.

III. RESULTS AND DISCUSSION

Suggested converter with 100 W output is simulated on MATLAB. TABLE I lists the components specification. Source voltage & source current waveform is shown in Fig. 3. We can see near UPF was achieved at source side.

TABLE I. SPECIFICATION A	AND DESIGN PARAMETERS
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S.No	Parameters	Values
1	V _s (RMS)	230 V
2	f _{supply}	50 Hz
3	Vo	100 V
4	Io	1 A
5	Po	100W
6	PC-stage switching frequency	48 kHz
7	RR-stage switching frequency	48 kHz
8		365 µH
9	L_2	1 mH
10	C1	160 µF
`11	C ₂	20 µF

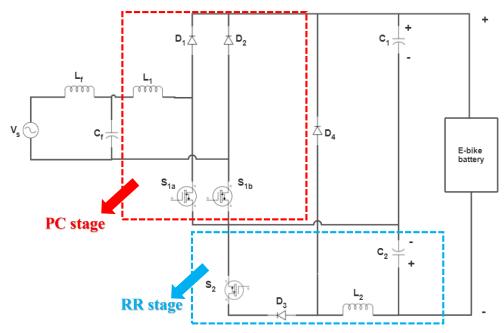


Fig. 2. Proposed converter model

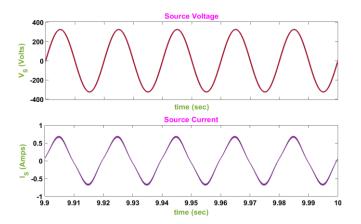


Fig. 3. Source voltage & source current waveform

Output voltage & output current waveforms are reflected in Fig. 4. We can see that 100 V voltage & 1 A current is maintained at the output making output power equal to 100 W.

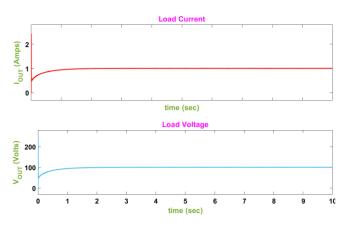
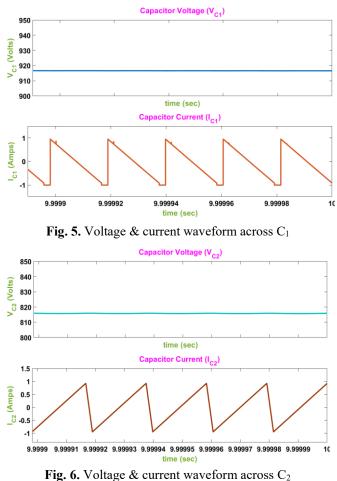


Fig. 4. Output voltage & output current waveform

Fig. 5 & Fig. 6 represents the voltage & current waveforms across capacitor $C_1 \& C_2$ respectively. With the help of C_2 , we were able to manage 0.5% ripple in the output voltage & 0.45% ripple in the output current which is well within the threshold limits.



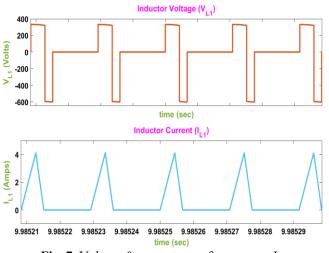


Fig. 7. Voltage & current waveform across L₁

Fig. 7 illustrates the waveforms for voltage & current across inductor L_1 & Fig. 8 represents the waveforms for voltage & current across inductor L_2 . The inductor (L_1) current is discontinuous as evident from Fig. 7.

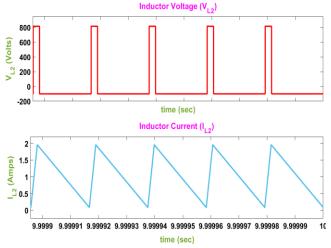


Fig. 8. Voltage & current waveform across L₂

S.No	Parameters	Converter [15]	Converter [16]	Proposed Converter
1	Switch count	1	4	3
2	Diode count	7	6	4
3	Filter inductance count	1	1	1
4	Filter capacitance count	2	2	1
5	PC stage inductance value	500 µH	1.3 mH	365 µH
6	Topology type	Conventional bridge topology	Conventional bridge topology	Bridgeless topology
7	Efficiency	92.4%	96.11%	98%

TABLE II. PERFORMANCE COMPARISON OF PRO	POSED CONVERTER
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IV. CONCLUSION

The proposal is for an improved power quality charger for e-bikes with minimum ripple in output voltage & output current which is 0.5% in output voltage & 0.45% in output current with the help of utilizing modest capacitances allowing for an electrolytic-capacitor-less driver for E-bike charging. The efficiency of 98%, 8% THD of source current and near UPF is achieved with proposed topology. It is accomplished by combining boost converter employed as power control step & power factor correction stage concurrently. Moreover, the suggested topology doesn't rely on transformers or integrated inductors, ensuring that the system operates without spikes & losses in windings shall be reduced. Furthermore, the suggested method does not necessitate any sophisticated control. Finally, parallel combination allows the percentage of circulating power in ripple reduction stage to remain under limits.

ACKNOWLEDGEMENT

The proposed research work is supported by IMPRINT-IIC.1 SERB research funded project IMP/2019/000295, IMPRINT-India, Govt. of India.

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