Nonisolated Switched Inductor – Capacitor based High Gain DC-DC Converter

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***Abstract*— This paper presents a nonisolated switched inductor-capacitor based DC-DC converter (NSLCDC) which combines switched inductor and capacitor technologies to accomplish high stepped-up voltage at the output terminals. The NSLCDC converter operates on the fundamental principle of parallel charge and series discharge of interleaved inductors with low component count. The steady state continuous conduction mode (CCM) of operation and a suitable comparison with the similar topologies are discussed in detail. The proposed NSLCDC converter of 100 W output power rating is simulated on PSIM platform and results are presented.**

Keywords*— *Nonisolated DC-DC converter, Switched Inductor-Capacitor, Continuous Conduction Mode (CCM).

I. INTRODUCTION

Recent trends signify the importance of renewable energy sources like solar, fuel cells, etc in the energy sector. These sources provide low and variable output DC voltages like 12 to 128 volts. These low voltage levels must be raised to a standard high voltage level to suit the applications like EV charging, satellite and DC home applications.

The conventional boost converter contains one inductor and one active switch so that to raise the voltages to higher levels the switch is stressed to longer time intervals and further the voltage gain provided is also not adequate for certain applications. The main demerit of the boost converter is the blocking capability of switch, which is at output voltage and thereby increased switching losses leading to poor efficiency. One of the classic solutions to attain high step-up gain is to cascade numerous boosting stages but the problem with this approach is the overall efficiency is greatly reduced.

Majority of voltage amplification techniques involve either isolated or nonisolated DC-DC converters. The isolated topologies in addition with flyback, push-pull, forward converter and half/full bridge converters are having a problem of voltage spikes across the switch. The main reason behind this voltage spikes is the leakage inductance of transformers or coupled inductors. These voltage spikes can be reduced by providing additional clamping circuits or snubber circuits for the switches. In either way additional components are added to the existing topology there by making the converter bulky, non-economical, increased losses and reduced efficiency.

The nonisolated DC-DC converters (without coupled inductor) are free from above stated problems. Numerous voltages raising techniques like active switched inductor/capacitor [1], voltage lift, voltage multiplier cells, quadratic boost [2] etc are available to raise the voltage levels. These nonisolated converters are compact in size, component count is less, more economical and power density is high. The nonisolated step-up converters are suited to those utilities where galvanic isolation is not necessary.

II. PROPOSED NSLCDC CONVERTER

The NSLCDC converter power circuit consists of a pair of identical inductors (L_1, L_2) for which the duration of energization is controlled by switches (S_1, S_2). The diode D_0 is to aid the for charging of capacitor C_0 and diodes D_1, D_2 to aid for charging/discharging of capacitors C_1, C_2 as shown in Fig. 1. The following steady state analysis is carried out on the assumption that all the elements in power circuit are ideal.

A. Operating Principle of NSLCDC Converter

The NSLCDC converter ccm operation is in two modes CCM_1 and CCM_2. The detail operation of the NSLCDC converter in these two modes is as follows

CCM_1 Mode of Operation:

In CCM_1 mode the switch S_1 and S_2 are turned ON i.e., shunting inductor pair (L_1, L_2) across the source and the ideal operating waveforms are as shown in fig. 2(a). The forward biased diode D_2 lead to the charging of capacitor c_2 from capacitor C_1 via switch S_1. The output capacitor C_0 energizes the load as shown in Fig. 3(a).

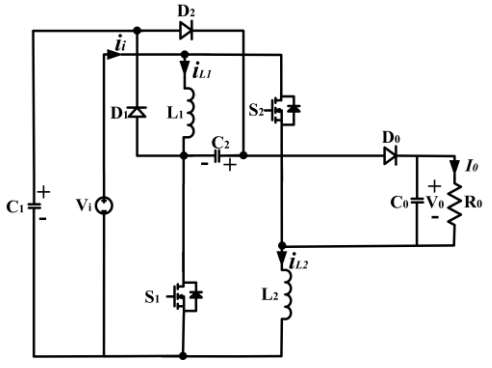

Fig. 1. The NSLCDC converter

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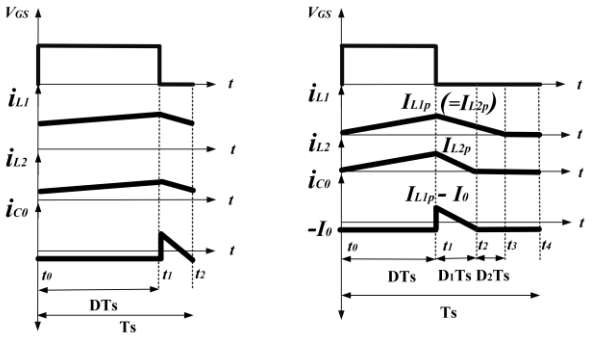
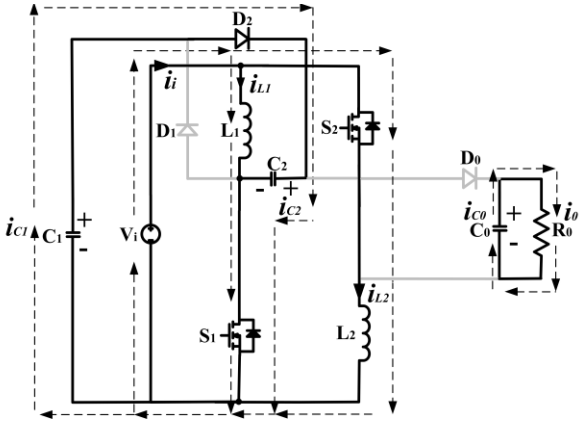
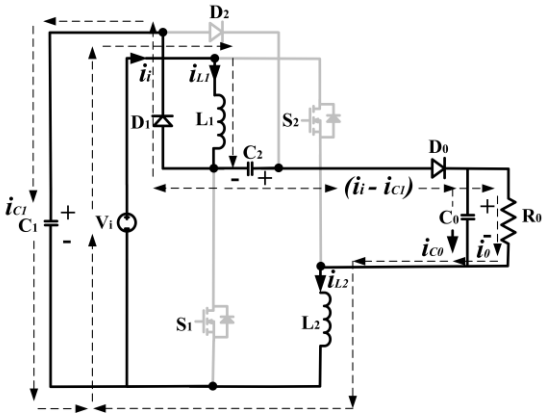


(a) (b)

Fig. 2 Operating Waveforms (a) CCM (b) DCM



(a)



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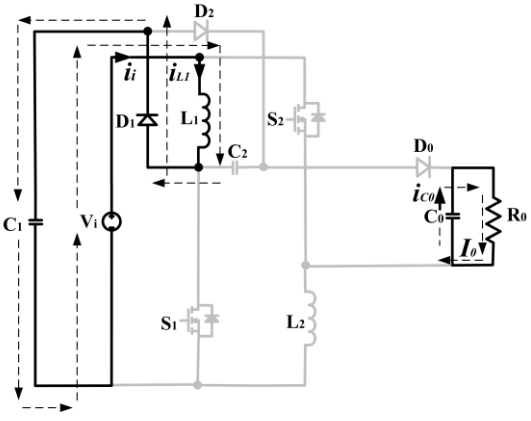

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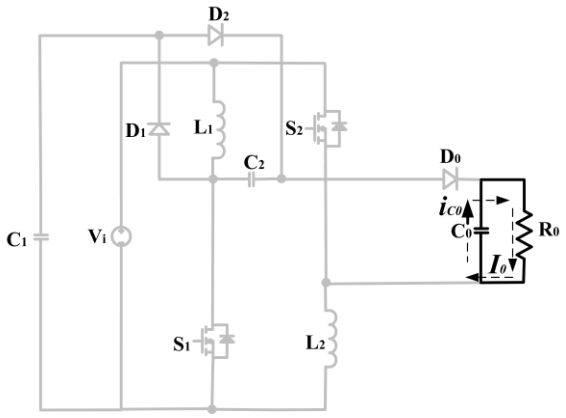


(d)

Fig. 3. Operating modes of NSLCDC converter (a) CCM_1 (b) CCM_2 (c), (d) DCM

The CCM_1 operating mode constitutes of the following element voltages

$$L_1 = L_2 = L \tag{1}$$

$$V_{L1} = V_{L2} = V_i \tag{2}$$

$$V_{C1} = V_{C2} \tag{3}$$

CCM_2 Mode of Operation:

In CCM_2 mode two switches are turned OFF. The two identical inductors (L_1, L_2) along with capacitor C_2 and DC source (V_i) discharges through the output capacitor (C_0) and load resistor (R_0) as shown in Fig. 3(b). The diode D_1 drives the capacitor C_1 charge from the combination of DC source V_i and inductor L_1.

The CCM_2 operating mode constitutes of the following element voltages

$$V_{L1} + V_{L2} = V_i + V_{C2} - V_0$$

$$V_L = \frac{V_i + V_{C2} - V_0}{2} \tag{4}$$

$$V_i = V_{C1} + V_{L1}$$

$$V_L = V_i - V_{C1} \tag{5}$$

Writing the volt-sec balance for inductor L_1

$$V_i D T_S + (V_i - V_{C1})(1 - D)T_S = 0$$

$$V_{C1} = \frac{V_i}{1 - D} \tag{6}$$

Similarly, volt-sec balance for inductor L_2 is as follows

$$V_i D T_S + \left(\frac{V_i + V_{C1} - V_0}{2}\right)(1 - D)T_S = 0$$

$$V_i\left(D + \frac{1 - D}{2}\right) + \left(\frac{1 - D}{2}\right)V_{C1} = \left(\frac{V_0}{2}\right)(1 - D) \tag{7}$$

Using (6) in (7), the voltage gain can be written as

$$V_0(1 - D) = V_i(2 + D)$$

$$G_{CCM}\left(\frac{V_0}{V_i}\right) = \left(\frac{2 + D}{1 - D}\right) \tag{8}$$

The step-up voltage gain variations with respect to the variation in the conducting duration of switches (D) is plotted as shown in Fig.6. Initial raise of the gain is very low and hence it is better practice to operate this converter more than 0.6 duty ratio for better step-up gains. The converter can attain a maximum step-up conversion ratio of

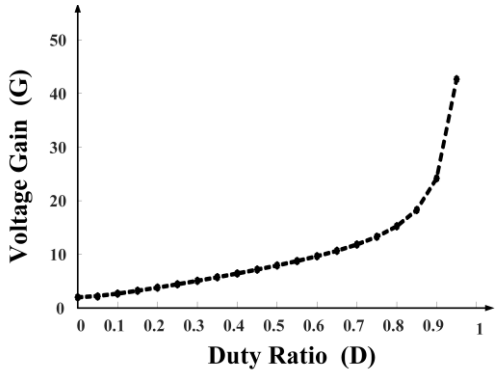


Fig. 4. DCM gain vs duty ratio

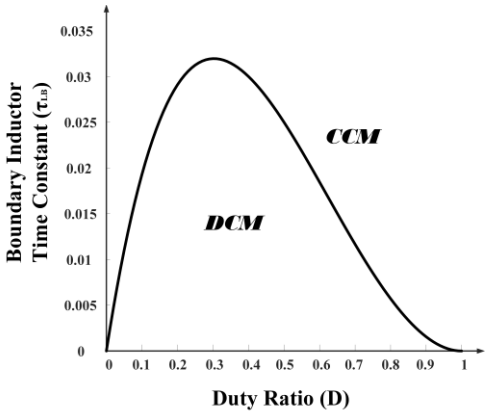


Fig. 5. Normalized boundary inductor time constant vs duty ratio

29 for a switch duty of 0.9. Increasing the duty ratio beyond 0.9 is not suggestable because the converter may enter into unstable region of operation.

The NSLDC converter dcm operation consists of three modes dcm_1, dcm_2 and dcm_3. The analysis and performance of proposed converter under dcm mode is as follows

DCM_1 Mode of Operation:

The operating principle is same for DCM_1 mode of operation as that of CCM_1 mode. The inductor L_2 peak currents are written as

$$I_{L2p} = \frac{V_i}{L} DT_S \tag{9}$$

DCM_2 Mode of Operation:

The operating principle is same for DCM_2 mode of operation as that of CCM_2 mode. The inductor L_2 peak currents are written as

$$I_{L2p} = \frac{V_0 - V_i\left(\frac{2}{1-D}\right)}{L} D_1 T_S \tag{10}$$

DCM_3 Mode of Operation:

This mode consists of two sub intervals D_1T_S, D_2T_S as shown in Fig. 2(b). At the end of period D_1T_S the inductor L_2 is completely demagnetized which makes the output capacitor (C_0) power the load and DC source along with inductor L_1 charges the capacitor (C_1) as shown in Fig 3(c). Similarly, at the end of period D_2T_S inductor L_1 also demagnetizes and capacitor C_0 continue powering the load as shown in Fig 3(d).

Equating (9) and (10), the duty ratio D_1 can be evaluated by the following equation

$$D_1 = \frac{V_i D}{V_0 - V_i\left(\frac{2}{1-D}\right)} \tag{11}$$

From Fig. 2(b) the average value of output capacitor current is written as

$$I_{C0} = \frac{\frac{1}{2} D_1 T_S I_{L2p} - I_0 T_S}{T_S} \tag{12}$$

Using (9), (11) in (12) and by making it equal to zero

$$\frac{(V_i D)^2}{\left(V_0 - V_i\left(\frac{2}{1-D}\right)\right)} = \frac{2 V_0}{R_0}(Lf_S) \tag{13}$$

Then, the normalized inductor time constant

$$\tau_L = \frac{Lf_S}{R_0} \tag{14}$$

Using (14) in (13) the DCM voltage gain is written as

$$G_{DCM} = \frac{1}{1-D} + \sqrt{\left(\frac{1}{1-D}\right)^2 + \frac{D^2}{2\,\tau_L}} \tag{15}$$

The step-up DCM voltage gain variations with respect to the variation in the conducting duration of switches (D) is (at, τ_L=0.004) plotted as shown in Fig.4.

At the boundary the CCM and DCM voltage gains are equal. Hence, from (8) and (15) the normalized boundary inductor time constant is written as

$$\tau_{LB} = \frac{D\,(1-D)^2}{2\,(D+2)} \tag{16}$$

The plot of normalized boundary inductor time constant against duty ratio is shown in Fig. 5, by locating CCM and DCM regions.

By considering an inductor L_2 current at the end of D_1T_S or at the beginning of D_2T_s like in (9) and (10), the duty ratio D_2 is derived as

$$D_2 = D_1 \tag{17}$$

B. Component Design

Inductor Design:

The two identical inductors are designed depending on the parameters of ripple current (Δi_L), duty ratio (D), applied voltage across the inductors and switching frequency (f_s).

$$L_1 = L_2 = \frac{V_i D}{\Delta i_L f_s} \tag{18}$$

By considering a suitable value for the ripple current inductor L_1 and L_2 values can be determined.

Capacitor Design:

The capacitance value of three capacitors (C_1, C_2, C_3) can be determined by voltage ripple (ΔV_C), duty ratio (D), switching frequency (f_s) and the current flowing through the capacitor.

By knowing proper charging and discharging patterns of the capacitors, the capacitances are determined as follows

$$C_1 = C_2 \geq \left(\frac{(i_i - i_L(1-D))}{\Delta V_{C1} f_s}\right) \tag{19}$$

$$C_0 \geq \left(\frac{i_0(1-D)}{\Delta V_{C0} f_s}\right) \tag{20}$$

TABLE I. COMPARISION OF NSLCDC CONVERTER WITH SIMLAR TOPOLOGIES

Converter	Voltage Gain	Nominal Switch Voltage Stress	Component Count				Total Component Count
			Inductors	*Capacitors*	*Diodes*	*Switches*	
A	$1/(1-D)$	1	1	1	1	1	4
B [3]	$2/(1-D)$	1/2	1	3	3	1	8
C [4]	$(1+D)/(1-D)$	$1/((1-D)\,G)$	2	2	4	2	10
D [5]	$(1+D)/(1-D)$	$(1+G)/G$	2	1	1	2	6
NSLCDC	$(2+D)/(1-D)$	$\frac{1}{2}-\frac{1}{2G}\left(\frac{D}{1-D}\right)$	2	3	3	2	10

A = Classic Boost Converter

III. COMPARATIVE ANALYSIS

The NSLCDC converter component count, switch voltage stress and voltage conversion ratio are compared with that of the converters specified in A, B, C and D as shown in Table I. It is clear from the Fig.6 that for the same operating constraints of duty ratio 0.85 the step-up gains provided by converters A, B and C/D are 6.66, 13.33 and 12.33 respectively, whereas the NSLCDC converter provides a step-up voltage gain of 29 which is far superior than all the stated converters. The component count compared with A, B and C converters is slightly higher but this is the optimized component count for the proposed topology to attain high voltage gain. The major advantage of the NSLCDC converter is drain to source voltage of switches is less than voltage V_0, thereby reducing the switching losses and increasing life span of the switches.

Where ΔV_{C1}, ΔV_{C2} and ΔV_{C3} are the ripple voltages of three capacitors respectively.

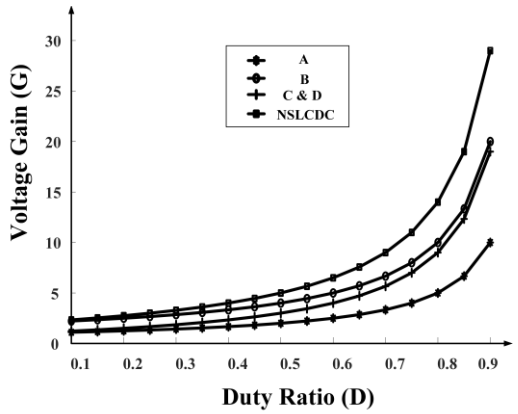


Fig. 6. Similar topologies voltage gain comparison with NSLCDC

IV. SIMULATON RESULTS

TABLE II. POWER CIRCUIT DESIGN SPECIFICATIONS

Parameter	Value
Power	100 W
Output voltage	380 V
Input voltage	20 V
Switching frequency	50 kHz
Voltage Gain	19
Duty Ratio	0.85
Inductors (L_1/L_2)	400 µH
Capacitors (C_0)	50 µF

The NSLCDC converter simulated with a load power rating of 100 W i.e a load resistor of 1444 Ω is used. The ideal switches are switched at a frequency (f_s) of 50 kHz at 85% duty. The inductors are identical with an inductance value of 400 µH. The capacitors values are chosen according to (19) and (20). The input voltage applied to the converter is 20 V and the output voltage attained with the above parametric values is 380 V i.e., a voltage gain of 19 is achieved as stated in Table II.

In this section the simulated results of NSLCDC converter are discussed. The proposed converter has been simulated with an output power rating of 100 W and key results are shown in Fig 7. The NSLCDC converter attains 380 V at the output with an applied voltage of 20 V and output voltage fluctuations ranging from 379.22 to 379.3 V as shown in Fig 7(a). The NSLCDC converter rated at 100 W delivers an output current of 263 mA to the load and draws an average current of 5.12 A at the input terminals, which fluctuates from 3.13 A to 6.12 A as shown in Fig 7(b).

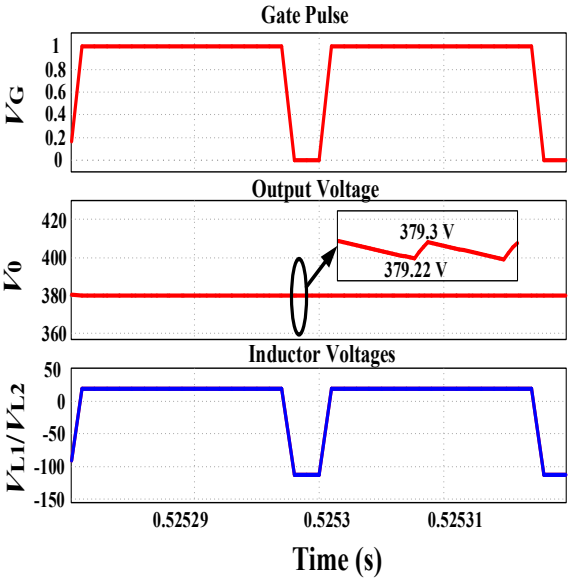
The voltage profile for the two identical inductors L_1 and L_2 is similar but the current profile will differ. The average current of inductor L_1 is 3.57 A fluctuating from 3.13 A to 3.98 A and that of inductor L_2 is 1.8 A ranging from 1.38 A to 2.23 A as shown in Fig 7(c).

The voltage across various elements is shown in Fig. 7 (d), (e) and (f). The average voltage of the capacitors C_1, C_2 is 133 V and that of the output capacitor C_0 is 380 V. The switches S_1 and S_2 are subjected to a voltage stress of 133 V, which is much less that the output voltage of 380 V. The output diode D_0 is subjected highest voltage stress of 380 V. The diodes D_1 and D_2 has a voltage stress of 133 V across them.

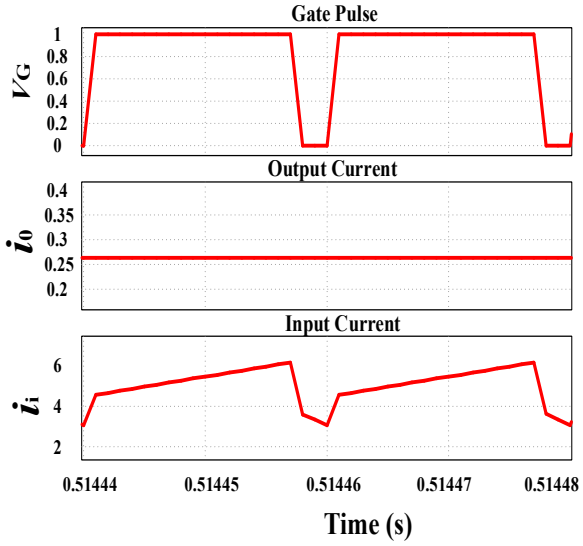
Effect of Nonidentical Inductors:

The effect of non-identical inductors in [2] (inductor L_1 > inductor L_2) caused a small interval between ON and OFF periods of the two switches but the overall step-up gain of the converter remains similar to that of identical inductors case.

The NSLCDC converter is simulated for inductor L_1 which is twice that of inductor L_2 and the results are presented in Fig. 8. It is clear from the current pattern of the two non-identical inductors that there is no such interval as in [2] between the intervals DT_S and (1-D) T_S. Moreover, output voltage and step-up conversion ratio of NSLCDC converter remains same to that of identical inductors case.



(a)



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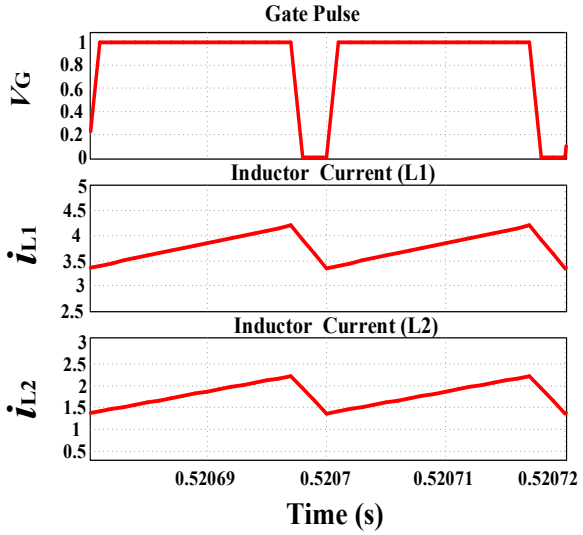

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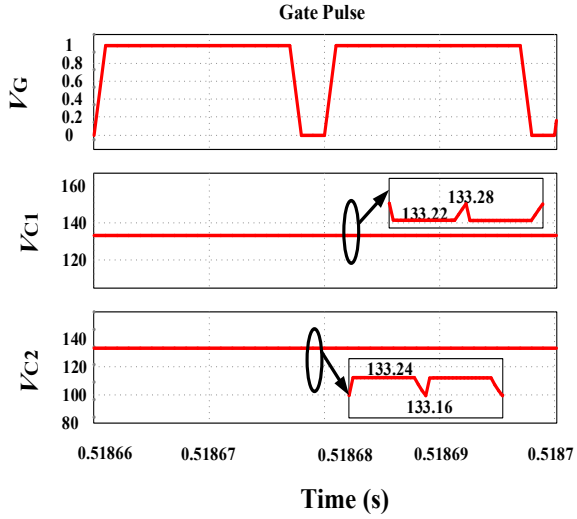
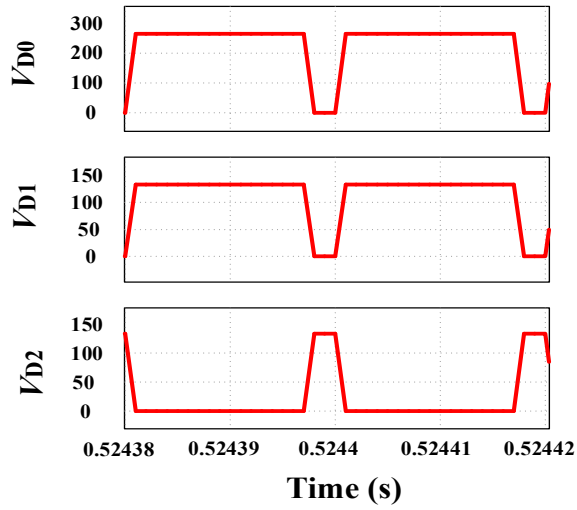


(d)



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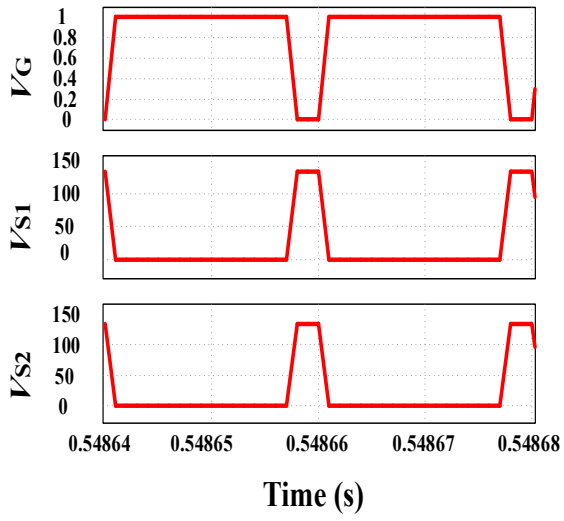

(f)

Fig.7. Simulated results of NSLCDC converter

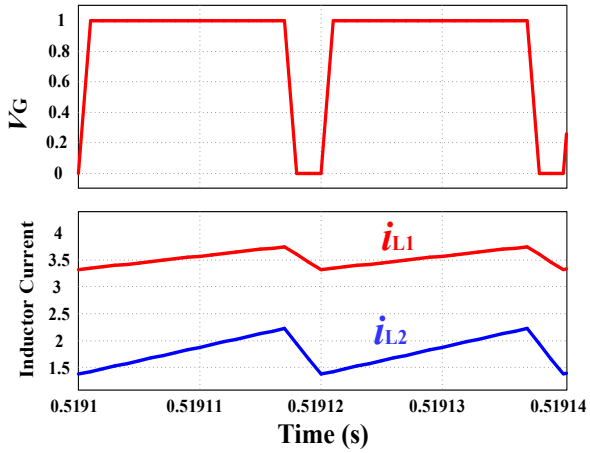

Fig. 8 Effect of nonideality in inductors

V. Conclusion

This paper presented a nonisolated DC-DC converter with the integration of switched inductor–capacitor techniques. High voltage gain achieved with the basic interleaved inductor boosting principle of parallel charge and series discharge. The voltage stress across the switches is less than output voltage which causes reduced switching losses and also the element count is optimized with the NSLCDC converter. The proposed converter rated at 100 W functionality is validated with the simulation results.

Acknowledgment

This research work is supported in part by Scheme for Promotion of Academic and Research Collaboration (SPARC), Government of India, through its research grant number: SPARC/2018-2019/P1392/SL

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