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A Front End Interleaved Split Duty Switched Inductor-Capacitor Based High Boost DC-DC Converter

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***Abstract*—DC microgrids have surged in popularity owing to the seamless integration of sustainable energy such as fuel cells, solar photovoltaic, wind and hydro power. Because of the comparatively modest output voltage of these energy sources, there is a need for highly efficient DC-to-DC converters to facilitate the integration with DC microgrids. This paper introduces a Front End Interleaved Split Duty Switched Inductor-Capacitor (SDSLC) based High Boost DC-DC Converter. SDSLC Converter achieves voltage gain amplification without the need for voltage multipliers, transformers, and voltage lifting methods. This design choice simplifies both the construction and operation. The primary advantage of this converter resides in its ability to operate switches with two distinct duty ratios, enabling ultra voltage gain is achieved without necessitating high duty ratios. SDSLC converter is theoretically deduced in continuous conduction mode. Detailed analysis at steady state of SDSLC Converter by these two distinct duty ratios is provided. The development of the SDSLC Converter is implemented in PSIM with 20V to 300V, 100W, and its accuracy is confirmed through theoretical validation.**

***Index Terms*—DC DC Converter, Switched Inductor, Switched Capacitor, High gain**

I. Introduction

The concept of microgrids continues to evolve with the aim of maximizing the contributions of sustainable energy resources [1], [2]. Sustainable energy sources necessitate a power electronic interface to effectively transmit power to the DC grid while maintaining satisfactory performance indices regarding power quality. Management of storing and releasing energy within the microgrid should also be taken into consideration [3], [4]. DC power sources typically yield low output voltage, necessitating the utilization of highly efficient, high-gain converters to fulfill the demands of DC loads.

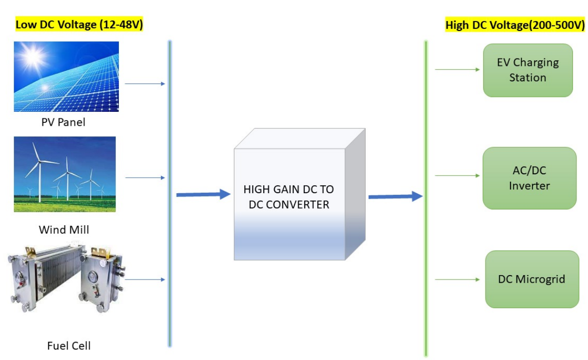

Fig. 1. Layout of a high gain DC-DC converter.

Historically, conventional DC-DC boost converters have been used to increase voltage levels as depicted in Fig.1. However, this approach presents challenges such as switch having a higher voltage stress, necessitates careful selection of high-rated switches to manage the stress [5]. Moreover, the use of larger duty ratios for attaining higher voltage gain causes to conduction losses, while also introducing significant diode issues. As a solution, utilizing non-isolated converters can achieve higher voltage gains with a concurrent reduction in size and cost. This approach addresses the aforementioned challenges while offering efficiency improvements and cost savings. Several non isolated high-gain converters include the cascaded boost, voltage lift, quadratic boost, voltage multiplier, and various topologies are evolved in the literature based on the boost converter [6]-[10].

This paper introduces a SDSLC Converter addressing previous issues. It achieves high voltage gain through inductor, capacitor, and with split duty ratio, offering several advantages:

- Three switches having two distinct duty ratios to achieve higher voltage gains.
- Greater voltage gain than conventional converters .
- Reduction of voltage stress on switches and diodes.
- Without using clamping circuit efficient energy is transferred.

II. Topology Description

Fig.2 depicts proposed SDSLC Converter which comprises of three switches (S_1, S_2, S_3), three diodes $(D1, D2, D3)$, two capacitors (C_1, C_2), and three inductors (L_1, L_2, L_3). Switches S_1, S_2, and S_3 operating at frequency f_s, with duty ratios D_1 for switches S_1, S_2 and D_2 for switch S_3.

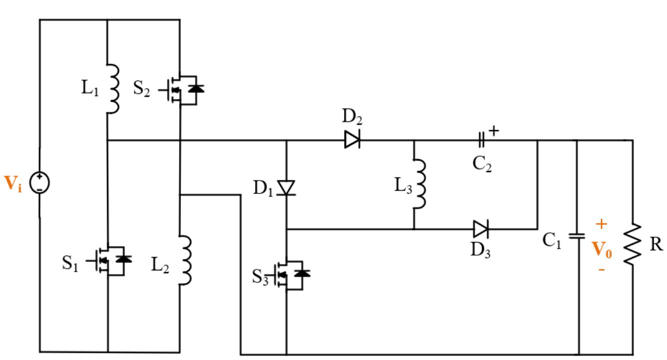

Fig. 2. The design of SDSLC Converter

To elucidate steady state operation of the SDSLC Converter, following assumptions have been taken into account:

- Consider the components as Ideal .
- Neglect the effects of equivalent series resistance of capacitors and inductors, switches resistance at ON state, and also the forward voltage drop of diodes.

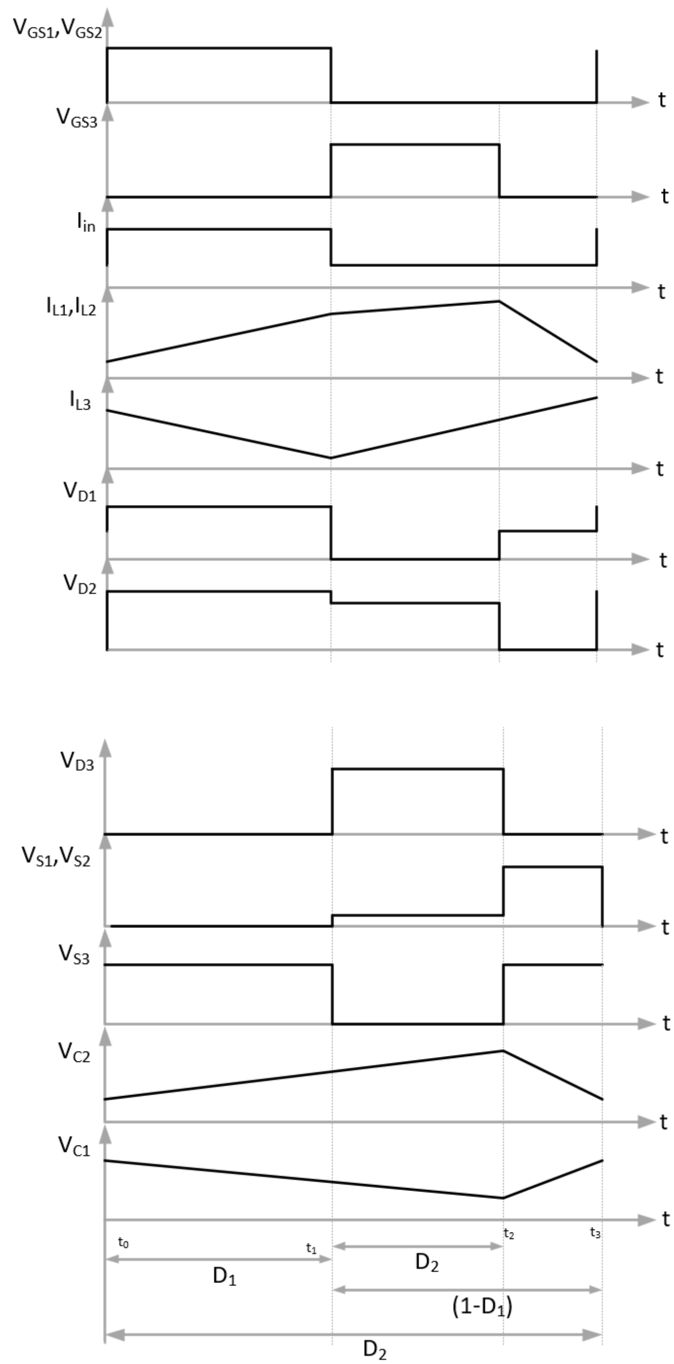

Fig. 3. CCM Operation of SDSLC Converter

III. Operation Theory of SDSLC Converter

Here we discuss about the operating modes of the SDSLC Converter during continuous conduction mode. SDSLC Converter operates in three distinct modes. Also voltage stress across diodes, and switches. Design equations of three inductors and two capacitors is mentioned. Fig.3 depicts the key waveforms of SDSLC Converter in CCM.

A. Operating Modes

Mode I: Fig.4 depicts the mode of operation, this mode takes place in the interval of time $[t_0, t_1]$. The DC source charges inductor L_1 through the switch S_1 and also charges inductor L_2 through the switch S_2 simultaneously. The switches S_1, S_2 to be switched ON while switch S_3 is to be switched OFF. Here capacitor C_2 discharges and also inductor L_3 discharges through diode $D3$. The capacitor C_1 discharges to resistive load R here.The equations that derived from KVL are:

$$V_{\text{L3}} = -V_{\text{C2}} \tag{1}$$

$$V_{\text{in}} = V_{\text{L1}} = V_{\text{L2}} \tag{2}$$

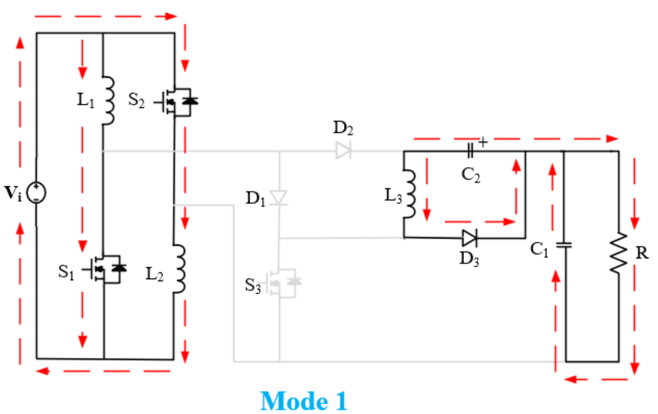

Fig. 4. SDSLC Converter operation in Mode I

Mode II: Fig.5 depicts the mode of operation, this mode takes place in the interval of time $[t_1, t_2]$, the switches S_1, S_2 to be switched OFF while switch S_3 to be switched ON. The DC source charges inductor L_1, L_2 through diode $D1$ simultaneously. Here capacitor C_1 discharges which charges the capacitor C_2, and also the inductor L_3. The equations that derived from KVL are:

$$V_{\text{L3}} = V_{\text{C1}} - V_{\text{C2}} \tag{3}$$

$$V_{\text{in}} = V_{\text{L1}} + V_{\text{L2}} \tag{4}$$

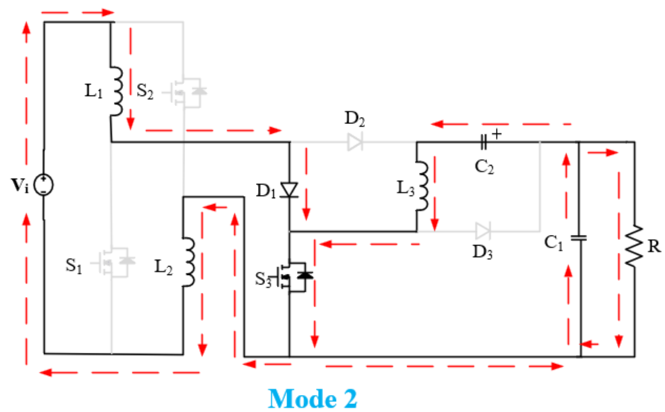

Fig. 5. SDSLC Converter operation in Mode II

Mode III: Fig.6 depicts the mode of operation, this mode takes place in the interval of time $[t_2, t_3]$, all the switches S_3, S_2, S_1 are switched OFF. And also all the inductors L_3, L_2, and L_1 discharges in this mode. Here capacitor C_2 discharges and also inductor L_3 discharges through diode $D3$. The capacitor C_1 discharges to resistive load R here. The equations that derived from KVL are:

$$V_{\text{L3}} = -V_{\text{C2}} \tag{5}$$

$$V_{\text{L1}} + V_{\text{L2}} = V_{\text{in}} - V_{\text{L3}} - V_{\text{C1}} \tag{6}$$

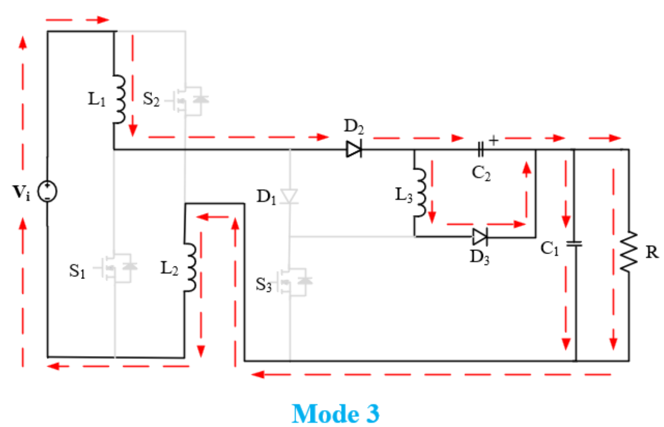

Fig. 6. SDSLC Converter operation in Mode III

The voltage-second balance method is employed to determine the average value of inductors L_1, L_2, and inductor L_3 seperately:

$$< v_{\text{L1}} + v_{\text{L2}} >= 2D_1V_{\text{in}} + D_2V_{\text{in}} + (1 - D_1 - D_2)(V_{\text{in}} - V_{\text{C1}} + V_{\text{C2}}) = 0 \tag{7}$$

$$< v_{\text{L3}} >= D_1(-V_{\text{C2}}) + D_2(V_{\text{C1}} - V_{\text{C2}}) + (1 - D_1 - D_2)(-V_{\text{C2}}) = 0 \tag{8}$$

On solving for V_{C1}

$$V_{\mathrm{C1}} = \frac{(1+D_1)V_{\mathrm{in}}}{(1-D_2)(1-D_1-D_2)} \tag{9}$$

The voltage gain obtained is

$$\frac{V_0}{V_{\mathrm{in}}} = \frac{(1+D_1)}{(1-D_2)(1-D_1-D_2)} \tag{10}$$

To attain high voltage gain, consider the following constraints:

- Both D_1 and D_2 must not equal 0.5
- The duty ratios D_1 and D_2 sum should not surpass 1.

B. Voltage Stress

The voltage stress across the switches S_1, S_2 and S_3 are given as

$$V_{\mathrm{S1}} = V_{\mathrm{S2}} = \frac{V_0(1-D_2)}{(1-D_1)} \tag{11}$$

$$V_{\mathrm{S3}} = V_0 \tag{12}$$

The voltage stress on the diodes D_1, D_2 and D_3 are given as

$$V_{\mathrm{D1}} = V_0 + V_{\mathrm{in}} \tag{13}$$

$$V_{\mathrm{D2}} = V_{\mathrm{in}} + \frac{2}{3}V_0 \tag{14}$$

$$V_{\mathrm{D3}} = V_0 \tag{15}$$

C. Design of Inductors

Selecting the inductors depends upon many factors such as the source voltage (V_{in}), switching frequency (f_s), ripple current and duty ratios (D_1, D_2). To ensure the SDSLC Converter operating in the Continuous Conduction Mode, the inductance value can be obtained using the below equations:

$$L_1 = L_2 = \frac{V_{\mathrm{in}}D_1}{\Delta i_{\mathrm{L1}} f_{\mathrm{s}}} \tag{16}$$

$$L_3 = \frac{V_{\mathrm{in}}D_1}{\Delta i_{\mathrm{L3}} f_{\mathrm{s}}(1-D_1-D_2)} \tag{17}$$

D. Design of Capacitors

When capacitors C_1, C_2 are charged we obtain the equations

$$I_{\mathrm{C1}}(1-D_1-D_2)T_{\mathrm{s}} = C_1 \Delta V_{\mathrm{C2}} \tag{18}$$

$$I_{\mathrm{C2}}(D_2)T_{\mathrm{s}} = C_2 \Delta V_{\mathrm{C2}} \tag{19}$$

By solving the above equations for C_1, C_2 we get

$$C_1 = \frac{(I_0)(1-D_1-D_2)}{f_{\mathrm{s}}\Delta V_{\mathrm{C1}}} \tag{20}$$

$$C_2 = \frac{(I_0)(1-D_2))}{f_{\mathrm{s}}\Delta V_{\mathrm{C2}}(1-D_1-D_2)} \tag{21}$$

IV. Analysis of Simulation

The SDSLC Converter has been formulated within the PSIM platform, incorporating meticulously selected parameter values to achieve an exceptionally high voltage gain. The design of the SDSLC Converter is illustrated in Fig.7. To validate its accuracy, both theoretical and simulation values are compared, yielding satisfactory results. Table.1 outlines the design specifications and component ratings.

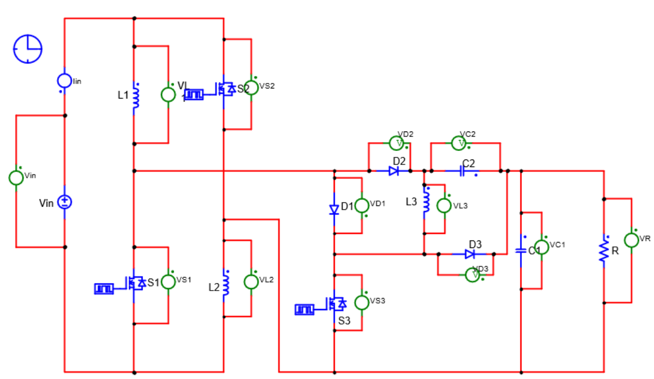

Fig. 7. SDSLC Converter design in PSIM

Fig.8 depicts the current and voltage waveforms of input and output at steady state. We can obtain voltage gain of 15 i.e for a input voltage 20V, output voltage is 300V. Fig.9 depicts the voltage across Inductors L_1, L_2 which are having the same voltage in three modes whereas L_3 having different voltage. Fig.10 depicts current through the Inductors L_1, L_2 having current ripple of 4.81% and for L_3 current ripple is 12.97% and the current is continous throughout the modes. If switches S_1, S_2 are switched ON, then input current (I_{in}) doubles the value of the inductor current L_1 or L_2. Conversely, if switches S_1, S_2 are switched OFF, the input current matches the inductor current L_1 or L_2. Fig.11 shows voltage across the Switches, and also the voltage stress seen here equal to that of theoretical equations. Fig.12 depicts current through the switches. Fig.13 depicts the voltage across the diodes, the diode stress seen here is equal to that of theoretical equations.

TABLE I
DESIGN SPECIFICATIONS

Components	Ratings
Source Voltage(V_{in})	20V
Output Voltage(V_0)	300V
Output Power	100W
Carrier Frequency(f_s)	50kHz
Duty Cycle(D_1)	0.5
Duty Cycle(D_2)	0.35
Inductance(L_1,L_2)	360uH
Inductance(L_3)	1000uH
Capacitance(C_1)	100uF
Capacitance(C_2)	22uF

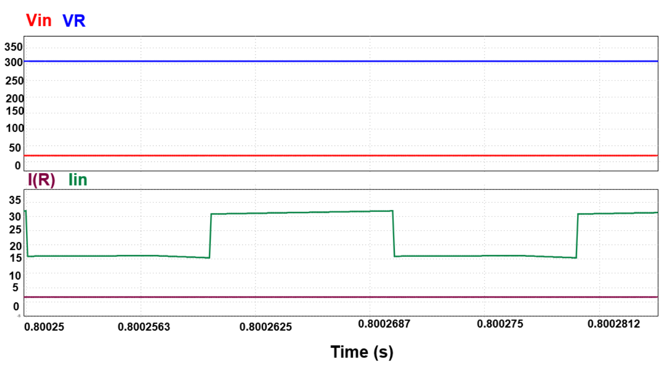

Fig. 8. Input and output waveforms of voltage and current

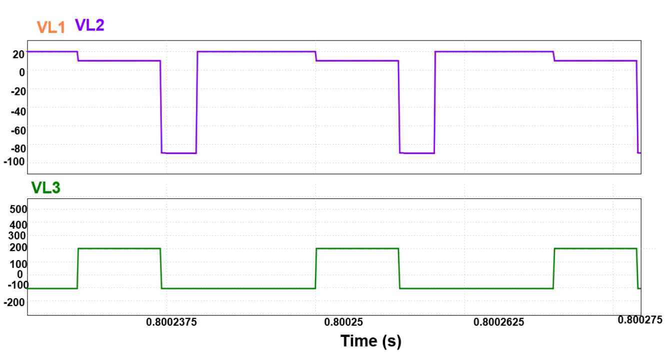

Fig. 9. Voltage across the Inductors

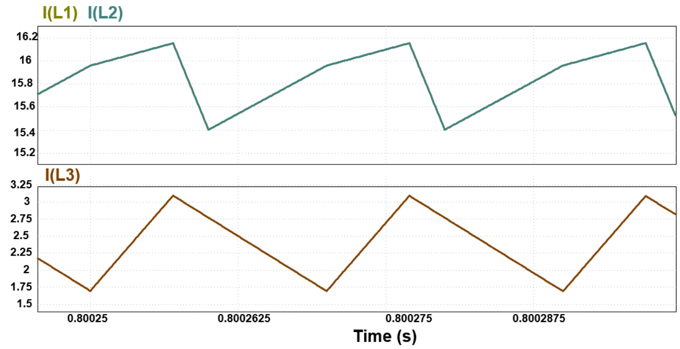

Fig. 10. Current of the Inductors

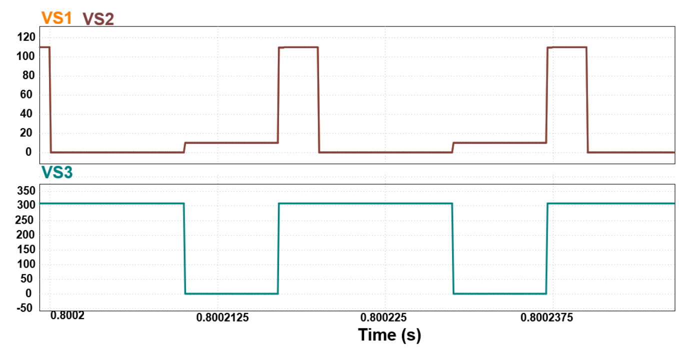

Fig. 11. Voltage across the Switches

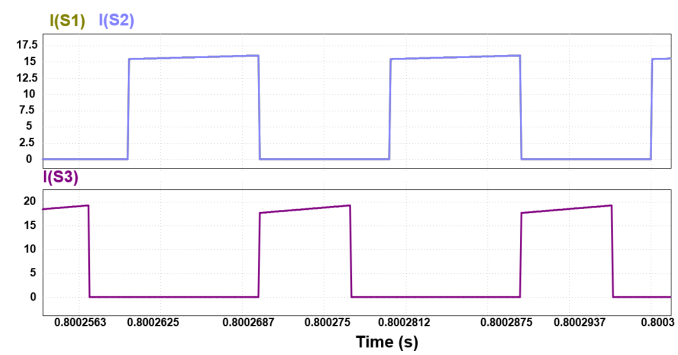

Fig. 12. Current of the Switches

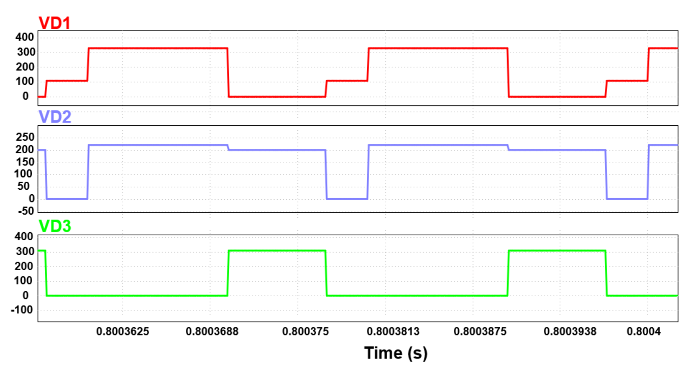

Fig. 13. Voltage across the Diodes

V. Conclusion

In this paper, SDSLC Converter was proposed to attain high voltage gain of 15 i.e for input voltage of 20V output voltage attained is 300V which is greater the converters proposed in [6]-[10]. In open-loop conditions, the output voltage varied by approximately 2.5 percent in response to changes in the load. The proposed SDSLC converter have a power rating of 100W. Percentage of Current ripple on inductors is less compared to others [6], [9]. Theoretical analysis and simulation analysis focused on factors such as voltage gain, parameter design, and switch voltage stress. Proposed converter in this study demonstrates some key advantages for DC microgrids. The proposed SDSLC Converter can be widely used for various voltage inputs.

The selection of the switches duty cycle is critical to meet real-world application demands, typically kept at or below 0.5. The duty ratio values of D_1=0.5 and D_2=0.35 chosen can satisfy many requirements. Voltage stress on switches and diodes is low. Due to a relatively simple structure, the volume and cost of the Converters can be relatively low.

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