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Active switched-capacitor based ultra-voltage gain quadratic boost DC-DC converters

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Abstract

This paper presents active switched capacitor integrated ultra-voltage gain quadratic boost converters (ASC-QBC). The step-up conversion ratio provided by quadratic boost converter is not ample to meet the renewable microsource applications. The active switched capacitor integrated quadratic boost converter is a propitious alternate to acquire high voltage conversion ratios. A simple diode-capacitor voltage lift arrangement is used in one of the introduced converters, thereby further enhancing the voltage gain and also reducing the input current ripple to a greater extent. The voltage stress on semiconductor devices is greatly alleviated with the aid of diode-capacitor voltage lift arrangement. The input current ripple aspects with green energy sources along with control feasibility of the proposed converters against input voltage and load perturbations are experimentally demonstrated for a power rating of 100 W. The theoretical analysis and performance indices of proposed converters are validated with a fabricated laboratory prototype.

KEYWORDS

DC-DC converter, nonisolated converter, quadratic boost converter, active switched capacitor, voltage gain

1 | INTRODUCTION

The conventional fossil fuels are depleting at a faster rate with greater emissions into the atmosphere. The aforementioned cause of depletion of conventional energy resources led to the development and penetration of green energy micro sources into the energy sector. These micro sources are mostly at consumer premises and can be able to form DC micro grid.[1] The aforementioned micro sources also known as green energy sources include photovoltaic cells, a stack of fuel cells, and battery energy management systems, etc. The merits of green energy sources are low emission, highly consistent, low cost, and, on the other hand, the major limitation of these sources is the low voltage at their output terminals. The terminal voltage range of green energy sources is typically 12–48 V; therefore, to be compatible with DC microgrid efficient power electronic interface, i.e., DC-DC voltage step-up converters are needed.[2–5] The general voltage of green energy micro sources is in the aforementioned range (12 to 48 V); in some exceptional cases, it would be 128 V, where it is necessary to form a low voltage DC bus. Later, this low DC bus voltage has to be stepped up in the range of 400 to 800 V by DC-DC converters to comply with the requirements DC microgrid. In addition to the previously mentioned DC microgrid application, DC-DC converters are used in other industries including telecommunication, stand-alone UPS systems, bulk data center power management, on-road lighting in the automotive industry, and power conditioning in medical equipment. Extensive research has been carried out to attain high step-up conversion ratios at low duty cycles.[6–10]

The majority of these DC-DC converters are classified into isolated and non-isolated. In isolated converters, in order to improve the step-up gain turns ratio is increased. This in turn degrades the performance indices like bulky in size, magnetic components caused additional losses, high cost, and leakage inductance. Both isolated and non-isolated converters have their own merits and demerits, but from a micro source point of view, non-isolated converters are preferable because of their compactness, ease of control and improved efficiency.[11]

The switched inductor[12] and switched capacitor[13,14] or integration of both into DC-DC converters is one of the prominent solutions to achieve impeccable voltage gains, but the duty ratios to retain this high voltage gain are extreme. So, in order to further boost the voltage gain to certain higher extents, auxiliary arrangements like diode-capacitor voltage lift,[15] voltage multipliers, and cascade connections[16,17] are used.

The coupled inductors[18,19] arrangement is also one of the solutions for attaining ample amplification of voltage in DC-DC converters. Similar to isolated converters, one of the factors to improve the voltage gain in coupled inductor DC-DC converters is the turns ratio, and another factor is the duty ratio. The coupled inductor converters are compact because all the windings are wound on a common core. The major concern of these coupled inductors is leakage inductance due to which a mismatch in volt-amps between the coupled windings will exist. This leakage inductance of coupled inductors causes voltage spikes across the switches in DC-DC converters.

The switched capacitor arrangement is used for voltage lifting purposes in most of the conventional nonisolated DC-DC converters. The converter in[20] uses switched capacitor arrangement as a voltage lift mechanism added to active switched inductor; however, the voltage gain attained is not quite high. To overcome this short fall of low voltage gain, a multistage switched inductor arrangement integrated with the switched capacitor is proposed in[21] but here, the component count is high. The posture of capacitor-diode (C_2-D_2) arrangement in converter[22] is exclusively used for voltage lifting. However, this posture of the capacitor-diode can be altered as the arrangement (C_2-D_2, C_3-D_3) in the proposed converters to combine the positive features of regenerative energization for one of the inductor and voltage lifting. One of the simple and efficient ways to enhance the voltage step-up conversion ratio with the optimized component count is to use this switched capacitor arrangement as an energizing (regenerative from the front-end inductor) element to the rear-end inductor. Thereby, the voltage gain is improved with simple and efficient converter construction.

The aforementioned discussion on numerous techniques to attain ample amplification of input voltage in DC-DC converters has some constraints like extreme duty ratio, probable failure of switches due to voltage spikes, high voltage–current stress, and bulky in nature etc., except the approach of rear-end inductor energization by the active switched capacitor arrangement. In order to have the merits of low duty ratio, simple construction, ease of operation and low voltage–current stress quadratic boost configuration with an integrated active switched capacitor arrangement would be one of the feasible solutions. So a quadratic boost converter with active switched-capacitor in the first stage (ASC-QBC-I) is proposed, and later, to enhance the voltage gain further, a simple diode-capacitor voltage lift arrangement is integrated into the first stage to form the proposed ASC-QBC-II converter.

2 | THE PROPOSED TOPOLOGIES POWER CIRCUIT DERIVATION

The power circuit of ASC-QBC-I converter is constructed by integrating ASC cell with the quadratic boost configuration as shown in Figure 1. The switch S_1 along with diode D_1 and capacitor C_1 forms ASC cell and the rest of the circuit

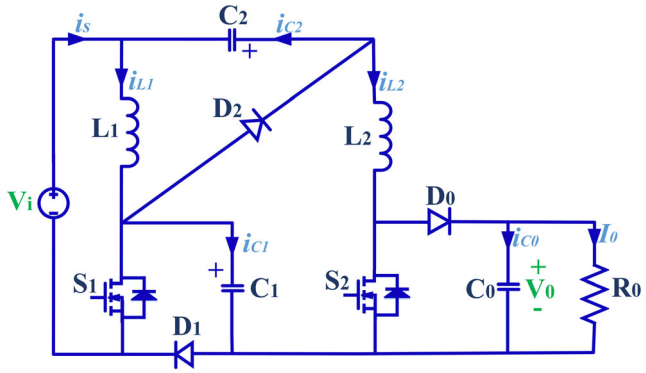


FIGURE 1 ASC-QBC-I converter

resembles the quadratic boost converter. The prime objective of capacitor C_1 of ASC cell in ASC-QBC-I converter is to charge the inductor L_2 along with the DC source (V_i) and capacitor (C_2).

The proposed ASC-QBC-I converter is a basic constructing element for the ASC-QBC-II converter in which switch S_2, diode D_2, and capacitor C_2 form ASC cell-II as shown in Figure 2. The diode-capacitor arrangement (D_4-C_4) is used for voltage lifting. Unlike capacitor C_1, the only purpose of capacitor C_2 in ASC cell II is to provide voltage lift but not to charge any of the two inductors (L_1 and L_2). By integrating ASC cell-II and diode (D4)-capacitor (C_4) arrangement to the ASC-QBC-I, the ASC-QBC-II converter is obtained.

3 | ANALYSIS OF ASC-QBC-I CONVERTER

The following analysis of ASC-QBC-I converter in terms of performance indices like voltage gain, element voltage and current stress, the effect of element parasitics, and converter efficiency is carried out for CCM operation. The theoretical waveforms for the ASC-QBC-I converter are as shown in Figure 3.

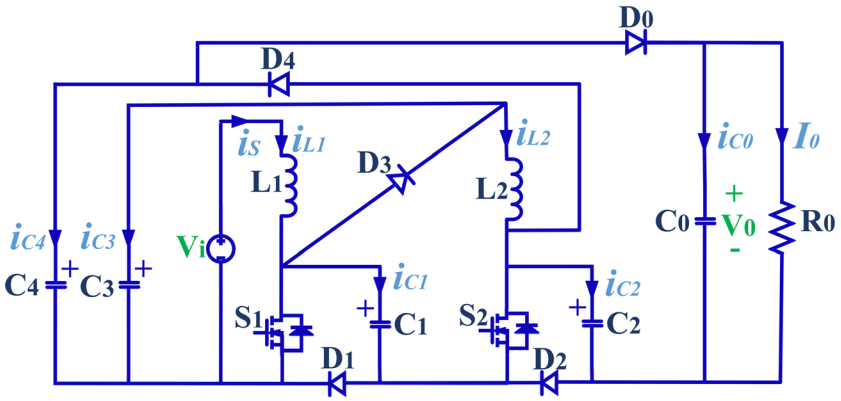


FIGURE 2 ASC-QBC-II converter

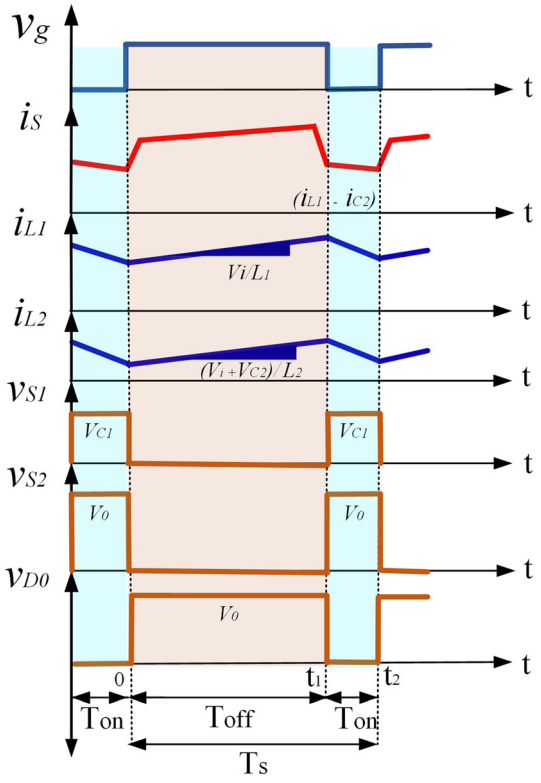


FIGURE 3 Ideal operating waveforms of ASC-QBC-I converter

3.1 | Operating state I ($0 \le t \le t_1$; DT_S)

The operating state I for a duration of DT_s corresponds to the turn ON of the switches (S_1 and S_2) at the instant t_0 as shown in Figure 4A. The input voltage (V_i) is applied across the inductor L_1, whereas the inductor L_2 will have a sum of voltages of V_i, V_{C1} and V_{C2}. Since diode D_0 is reverse biased load (R_0) is powered by capacitor C_0. In this operating state, all the intermediate capacitors are in discharging mode.

The voltage profile of the two inductors is governed by the following equations:

$$V_{L1} = V_i, \tag{1}$$

$$V_{L2} = V_i + V_{C1} + V_{C2} \tag{2}$$

3.2 | Operating state II ($t_1 \le t \le t_2$; $(1\text{-}D)T_S$)

This is the operating state in which both the switches at the instant t_1 are turned OFF as shown in Figure 4B. The source along with inductor L_1 charges the capacitor C_1 and the capacitor C_2 is charged by the inductor L_1. Since the diode D_0 has forward biased, the source along with the two inductors powers the combination of capacitor C_0 and load R_0.

The voltage profile of the two inductors L_1 and L_2 is as follows:

$$V_{L1} = V_i - V_{C1}, \tag{3}$$

$$V_{L2} = V_i + V_{C2} - V_0. \tag{4}$$

For the instants t_0-t_1 and t_1-t_2, the volt-sec balance for the inductor L_1 is as follows:

$$\int_{t_0}^{t_1} (V_i)\,dt + \int_{t_1}^{t_2} (V_i - V_{C1})\,dt = 0. \tag{5}$$

Simplifying the above expression,

$$V_{C1} = \frac{V_i}{1-D}. \tag{6}$$

Similarly, for the aforementioned time instants, the volt-sec balance for inductor L_2 is written as

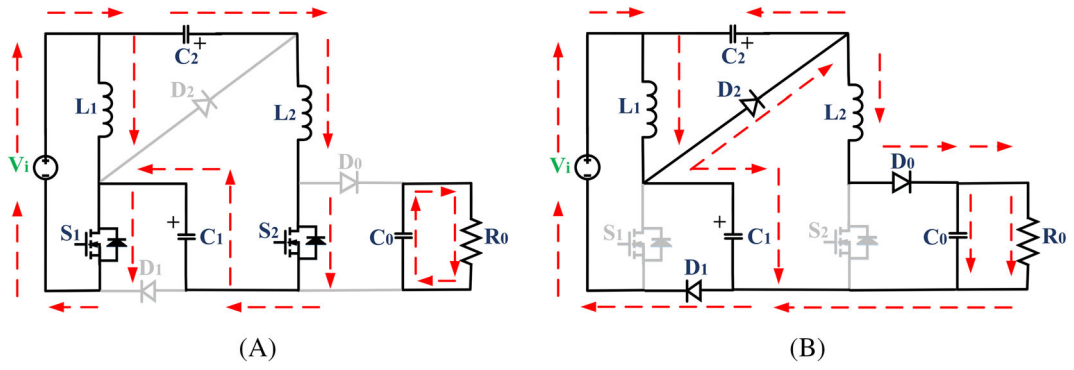


FIGURE 4 Operating states of ASC-QBC-I converter (A) state I and (B) state II

$$\int_{t_0}^{t_1}(V_i+V_{C1}+V_{C2})\,dt+\int_{t_1}^{t_2}(V_i+V_{C2}-V_0)\,dt=0. \tag{7}$$

For the instants t_1-t_2,

$$V_{L1}=-V_{C2}. \tag{8}$$

Using (8) in (3), the capacitor C_2 voltage is obtained as

$$V_{C2}=V_i\left(\frac{D}{1-D}\right). \tag{9}$$

Using (6) and (9) in (7), the CCM voltage gain is written as

$$G_1\left(\frac{V_0}{V_i}\right)=\frac{1+D}{(1-D)^2}. \tag{10}$$

3.3 | Diode-switch voltage stress analysis

The blocking voltages will appear across semiconductor elements when the diodes are reverse biased and the switches are at turn OFF condition. Considering the aforementioned operating conditions and writing appropriate KVL equations for the suitable loops, the blocking voltages are specified as in Table 1.

3.4 | Diode-switch current stress analysis

The following current expressions are produced by using KCL for the two operating states of the ASC-QBC-I converter on individual capacitors.

$$\left.\begin{aligned} I_{C1-ON}&=-I_{L2}\\ I_{C2-ON}&=-I_{L2}\\ I_{C0-ON}&=-I_0 \end{aligned}\right\}\quad\left\{\begin{aligned} I_{C1-OFF}&=\frac{I_{L1}-I_{L2}}{2}\\ I_{C2-OFF}&=\frac{I_{L1}-I_{L2}}{2}\\ I_{C0-OFF}&=I_{L2}-I_0 \end{aligned}\right\} \tag{11}$$

Since the average current through the capacitor C_0 is zero,

$$(-I_0)D+(I_{L2}-I_0)(1-D)=0. \tag{12}$$

Rewriting the above expression, the inductor L_2 current is written as

TABLE 1 Diode-switch voltage stress

Diodes			Switches	
V_{D0}	V_{D1}	V_{D2}	V_{S1}	V_{S2}
V_0	$\frac{V_i}{1-D}$	$\frac{V_i}{1-D}$	$\frac{V_i}{1-D}$	V_0

$$I_{L2} = \frac{I_0}{1-D}. \tag{13}$$

By making the average current of capacitor C_1/C_2 equal to zero,

$$(-I_{L2})D + \left(\frac{I_{L1} - I_{L2}}{2}\right)(1-D) = 0.$$

Rewriting the above expression, the inductor L_1 current is written as

$$I_{L1} = \frac{I_{L2}(1+D)}{1-D}. \tag{14}$$

Using (13) in (14), the current I_{L1} is expressed as

$$I_{L1} = \frac{I_0(1+D)}{(1-D)^2}. \tag{15}$$

The peak current stress on the switch S_1 is obtained as

$$I_{S1} = I_{L1} - I_{C2-ON}.$$

Using (11) and (15) in the above expression,

$$I_{S1} = \frac{2I_0}{(1-D)^2}. \tag{16}$$

Similarly, the current stress on switch S_2 is written as

$$I_{S2} = \frac{I_0}{1-D}. \tag{17}$$

The semiconductor current stress is as shown in Table 2.

3.5 | Parasitic parameters influence on voltage gain and efficiency

Each element in the power circuit of the proposed ASC-QBC-I converter contains some parasitics such as capacitance with series ESR of r_C, inductors with series ESR of r_{LX} (x = 1–2), semiconducting elements, i.e., diodes with respective ESR of r_{DX} (X = 0–2), and forward voltage drop of V_{FDX} (X = 0–2), and for the switches during conducting period, the parasitic element is a resistance r_S. By incorporating the parasitics of the respective elements into the ideal power circuit, then the ASC-QBC-I converter is as shown in Figure 5.

TABLE 2 Diode-switch current stress

Diodes			Switches	
I_{D0}	I_{D1}	I_{D2}	I_{S1}	I_{S2}
$\frac{I_0}{1-D}$	$\frac{I_0}{(1-D)^2}$	$\frac{I_0}{(1-D)^2}$	$\frac{2I_0}{(1-D)^2}$	$\frac{I_0}{1-D}$

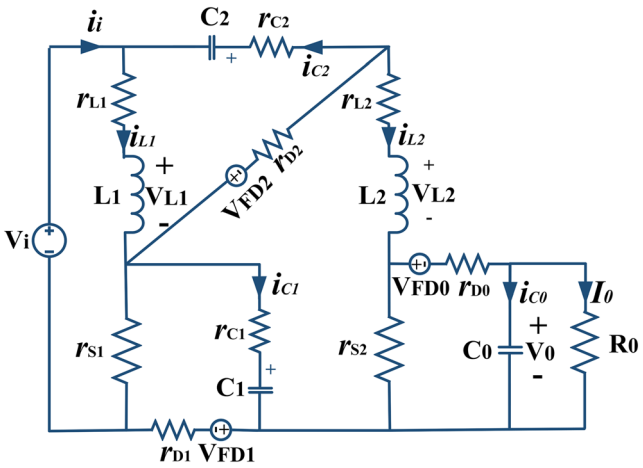


FIGURE 5 Equivalent circuit of ASC-QBC-I converter with element parasitics

For the operating state 1 (with $V_{L1} = -V_{C2}$) and 2, the voltage of inductor L_2 in the presence of element parasitics can be expressed as

$$V_{L2} = V_i + V_{C1} + V_{C2} - I_{L2}r_{L2} - I_C(2r_C) - I_{S1}r_S - I_{S2}r_S, \tag{18}$$

$$V_{L2} = V_i + V_{C2} - I_{L1}r_{L1} - I_{L2}(r_{L2} + r_{D0}) - I_{D2}r_{D2} - (V_0 + V_{FD0} + V_{FD1}). \tag{19}$$

Writing the volt-sec balance for inductor L_2 under the influence of element parasitics, the output voltage is as follows:

$$V_0 = \frac{V_i\left(\frac{1+D}{(1-D)^2}\right) - V_{FD0} - V_{FD1}}{1 + \left(\frac{r_{D0}}{R_0}\right) + a_1\left(\frac{r_C}{R_0}\right) + b_1\left(\frac{r_{L1}}{R_0}\right) + c_1\left(\frac{r_S}{R_0}\right) + d_1\left(\frac{r_{L2}}{R_0}\right) + e_1\left(\frac{r_S}{R_0}\right) + \left(\frac{r_{D2}}{R_0}\right)}, \tag{20}$$

where

$$a_1 = \frac{2D}{1-D}\ b_1 = \frac{1+D}{(1-D)^2}\ c_1 = \frac{D^2(1+D)}{(1-D)^3}\ d_1 = \frac{1}{(1-D)^2}\ e_1 = \frac{D}{(1-D)^2}.$$

The plot of nonideal terminal voltage and voltage gain with the effect of element parasitics is shown in Figure 6. Later in the experimental validation, we can observe that this non-ideal voltage gain is in good accord with the experimental voltage gain.

Using (20), the efficiency of ASC-QBC-I converter can be evaluated as

$$\eta = \frac{1 - (V_{FD0} + V_{FD1})/V_{0-ideal}}{1 + \left(\frac{r_{D0}}{R_0}\right) + a_1\left(\frac{r_C}{R_0}\right) + b_1\left(\frac{r_{L1}}{R_0}\right) + c_1\left(\frac{r_S}{R_0}\right) + d_1\left(\frac{r_{L2}}{R_0}\right) + e_1\left(\frac{r_S}{R_0}\right) + \left(\frac{r_{D2}}{R_0}\right)}. \tag{21}$$

The schematic representation of efficiency versus duty ratio is shown in Figure 7, in which the efficiency for the operating conditions of ASC-QBC-I converter is in good agreement with the experimental validation.

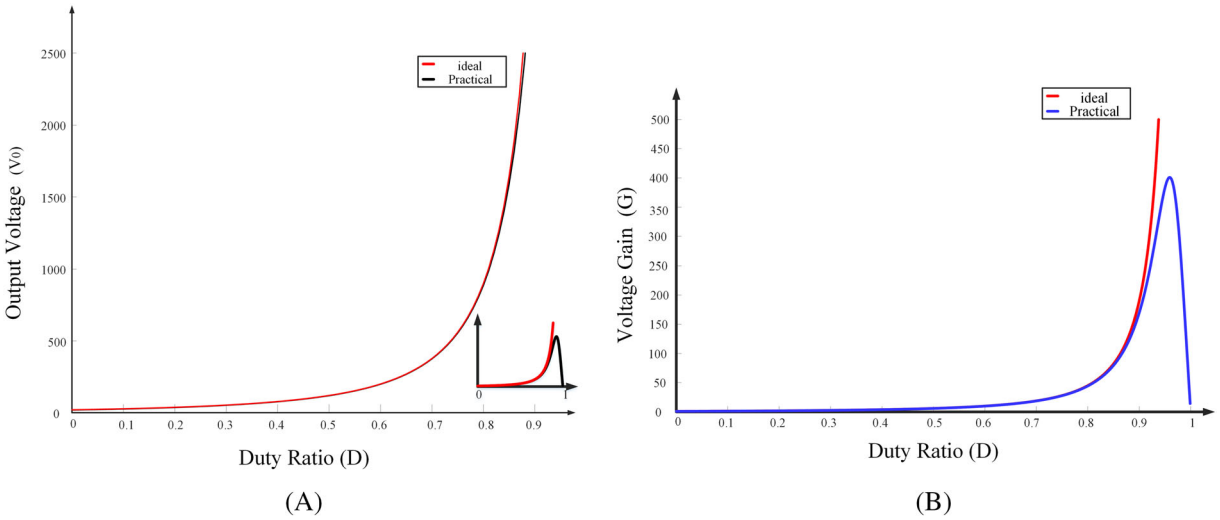


FIGURE 6 ASC-QBC-I converter nonideal (A) terminal voltage (B) voltage gain with element parasitics

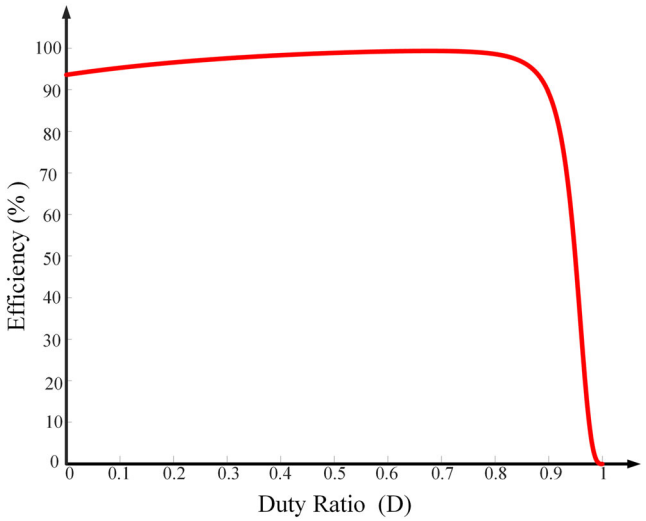


FIGURE 7 Efficiency versus duty ratio with element parasitics of ASC-QBC-I converter

4 | ANALYSIS OF ASC-QBC-II CONVERTER

The following discussion on performance indices of ASC-QBC-II is similar to that of ASC-QBC-I converter, and the posture of capacitor C_3 is altered to reduce the input current ripple. The ideal operating waveforms of ASC-QBC-II converter are as shown in Figure 8.

4.1 | Operating state I ($0 \leq t \leq t_1$; DT_S)

In this duration of time (DT_S), the switches (S_1, S_2) associated with the inductors are conducting as shown in Figure 9A. The inductors magnetization, i.e., the voltage applied across them, is similar to that of ASC-QBC-I converter. All the capacitors (C_1-C_4) are discharging except capacitor C_0, which along with load R_0 powered by the capacitor C_4.

The inductor voltage profile for state I is as follows

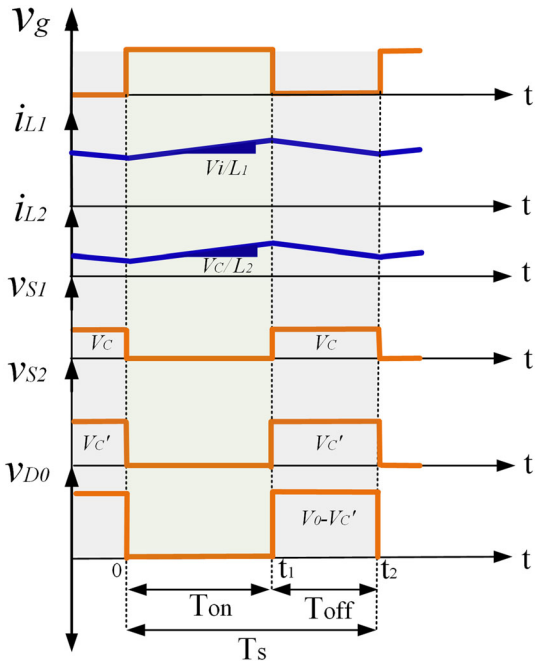


FIGURE 8 Ideal operating waveforms of ASC-QBC-II converter

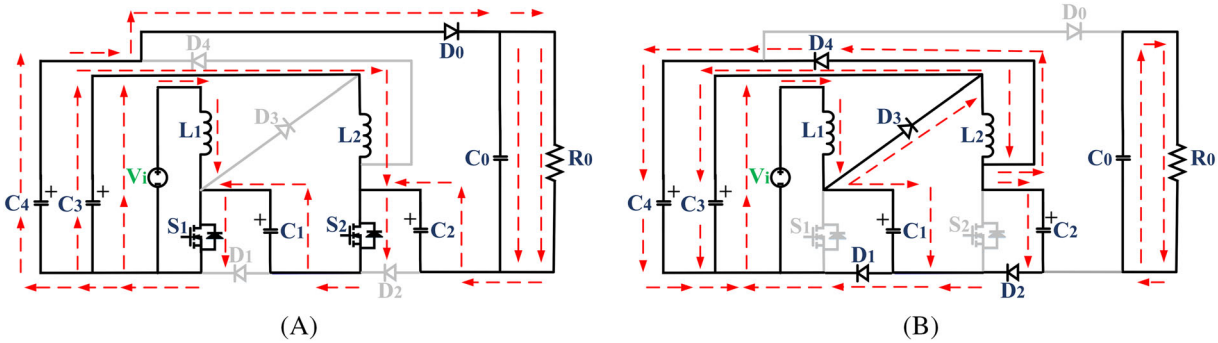


FIGURE 9 Operating states of ASC-QBC-II converter: (A) state I; (B) state II

$$V_{L1} = V_i, \tag{22}$$

$$V_{L2} = V_{C1} + V_{C3}. \tag{23}$$

Since

$$V_{C1} = V_{C3} = V_C,$$

$$V_{L2} = 2V_C. \tag{24}$$

4.2 | Operating state II ($t_1 \le t \le t_2$; (1-D)T_S)

The operating state II corresponds to turn OFF condition of the switches (S_1, S_2) as shown in Figure 9B. The charging pattern of capacitor C_1 is similar to the previous converter, whereas the capacitor C_3 is charged by the combination of

source (V_i) along with inductor L_1. In this stage II, the source (V_i) along with two inductors (L_1, L_2) charges the capacitors C_2 and C_4. Since the load end diode D_0 is reverse biased, capacitor C_0 powers the load (R_0).

The inductor voltages for operating state II are as follows:

$$V_{L1} = V_i - V_{C1}, \tag{25}$$

$$V_{L2} = V_{C3} - V_{C2}. \tag{26}$$

The capacitors C_3 and C_4 voltages can be written as

$$V_{C3} = V_{C4} = V_C{}', \tag{27}$$

applying the volt-sec balance for both the inductors L_1 and L_2 within the duration of t_0-t_2.

For inductor L_1,

$$\int_{t_0}^{t_1} V_i \, dt + \int_{t_1}^{t_2} (V_i - V_C) \, dt = 0.$$

Rewriting the above expression for the voltages of capacitors C_1 and C_3,

$$V_{C1} = V_{C3} = V_C = \frac{V_i}{1-D}. \tag{28}$$

For inductor L_2,

$$\int_{t_0}^{t_1} 2V_C \, dt + \int_{t_1}^{t_2} \left(V_C - V_C{}'\right) dt = 0.$$

By using the above expression, the capacitor C_2 and C_4 voltages are as follows:

$$V_{C2} = V_{C4} = V_C{}' = \frac{V_i(1+D)}{(1-D)^2}. \tag{29}$$

The duration t_0-t_1 in which the diode D_0 is conducting; the output voltage is expressed as

$$\begin{aligned} V_0 &= V_{C1} + V_{C2} + V_{C4}, \\ V_0 &= V_C + 2V_C{}'. \end{aligned} \tag{30}$$

Using (28) and (29) in (30), the output voltage can be evaluated as

$$V_0 = \frac{V_i(3+D)}{(1-D)^2}. \tag{31}$$

The CCM voltage gain of ASC-QBC-II converter is as follows:

$$G_2\left(\frac{V_0}{V_i}\right)=\frac{(3+D)}{(1-D)^2}. \tag{32}$$

4.3 | Diode-switch voltage stress analysis

The voltage stress of different elements in ASC-QBC-II converter can be evaluated by corresponding KVL equations for the suitable loops and as presented in Table 3.

4.4 | Diode-switch current stress analysis

The approach for evaluating different element current stress is similar to that of the previous case and are represented as follows:

$$\left.\begin{aligned} \mathrm{I_{C0-ON}}&=\frac{\mathrm{I_0}(1-\mathrm{D})}{\mathrm{D}}\\ \mathrm{I_{C1-ON}}&=\frac{-\mathrm{I_0}(1+\mathrm{D})}{\mathrm{D}(1-\mathrm{D})}\\ \mathrm{I_{C2-ON}}&=\frac{-\mathrm{I_0}}{\mathrm{D}}\\ \mathrm{I_{C3-ON}}&=\frac{-2\,\mathrm{I_0}}{(1-\mathrm{D})}\\ \mathrm{I_{C4-ON}}&=\frac{-\mathrm{I_0}}{\mathrm{D}} \end{aligned}\right\}\quad\left\{\begin{aligned} \mathrm{I_{C0-OFF}}&=-\mathrm{I_0}\\ \mathrm{I_{C1-OFF}}&=\frac{\mathrm{I_0}(1+\mathrm{D})}{(1-\mathrm{D})^2}\\ \mathrm{I_{C2-OFF}}&=\frac{\mathrm{I_0}}{(1-\mathrm{D})}\\ \mathrm{I_{C3-OFF}}&=\frac{\mathrm{I_0}\,(2\mathrm{D})}{(1-\mathrm{D})^2}\\ \mathrm{I_{C4-OFF}}&=\frac{\mathrm{I_0}}{(1-\mathrm{D})} \end{aligned}\right\}. \tag{33}$$

By using (33), the average inductor currents are written as follows:

$$\mathrm{I_{L1}}=\frac{\mathrm{I_0}\,(3+\mathrm{D})}{(1-\mathrm{D})^2}, \tag{34}$$

$$\mathrm{I_{L2}}=\frac{2\,\mathrm{I_0}}{1-\mathrm{D}}. \tag{35}$$

Similarly, the current stress of semiconductor elements is as presented in Table 4.

TABLE 3 Diode-switch voltage stress

Diodes					Switches	
$\mathbf{V_{D0}}$	$\mathbf{V_{D1}}$	$\mathbf{V_{D2}}$	$\mathbf{V_{D3}}$	$\mathbf{V_{D4}}$	$\mathbf{V_{S1}}$	$\mathbf{V_{S2}}$
$\frac{2V_i}{(1-D)^2}$	$\frac{V_i}{1-D}$	$\frac{V_i(1+D)}{(1-D)^2}$	$\frac{V_i}{1-D}$	$\frac{2V_i}{(1-D)^2}$	$\frac{V_i}{1-D}$	$\frac{V_i(1+D)}{(1-D)^2}$

TABLE 4 Diode-switch current stress

Diodes					Switches	
$\boldsymbol{I_{D0}}$	$\boldsymbol{I_{D1}}$	$\boldsymbol{I_{D2}}$	$\boldsymbol{I_{D3}}$	$\boldsymbol{I_{D4}}$	$\boldsymbol{I_{S1}}$	$\boldsymbol{I_{S2}}$
$\frac{I_0}{D}$	$\frac{2I_0}{(1-D)}$	$\frac{I_0}{(1-D)}$	$\frac{2I_0}{(1-D)^2}$	$\frac{I_0}{(1-D)}$	$\frac{I_0(1+3D)}{D(1-D)^2}$	$\frac{I_0(1+D)}{D(1-D)}$

4.5 | Parasitic parameters influence on voltage gain and efficiency

The power circuit of the proposed ASC-QBC-II converter under the influence of element parasitics is as shown in Figure 10. The inductors L_1 and L_2 voltages for operating state I, i.e., when the switches S_1 and S_2 are turned ON, can be written as

$$V_{L1} = V_i - I_{L1}r_{L1} - I_{S1}r_S, \tag{36}$$

$$V_{L2} = V_{C3} - I_{C3}r_C - I_{L2}r_{L2} - I_{S2}r_S + V_{C1} - I_{C1}r_C - I_{S1}r_S, \tag{37}$$

The operating state II corresponds to the turn OFF switches S_1 and S_2. For this duration, the inductor voltages L_1 and L_2 are written as

$$V_{L1} = V_i - I_{L1}r_{L1} - I_{C1}r_C - V_{C1} - I_{D1}r_{D1} - V_{FD1}, \tag{38}$$

$$V_{L2} = V_{C3} - I_{C3}r_C - I_{L2}r_{L2} - I_{C2}r_C - V_{C2} - I_{D2}r_{D2} - V_{FD2} - I_{D1}r_{D1} - V_{FD1}, \tag{39}$$

Writing the volt-sec balance for inductor L_1, the capacitor C_1 voltage is written as

$$V_{C1} = \frac{V_i}{(1-D)} - \frac{I_0(a')}{(1-D)^3} - V_{FD1}, \tag{40}$$

where

$$a' = \frac{r_{L1}(3+D) + r_S(1+3D) + r_C(1-D^2) + r_{D1}2D(1-D)}{(1-D)^2}.$$

Similarly, writing the volt-sec balance for inductor L_2, the capacitor C_2 voltage is written as

$$V_{C2} = \frac{V_{C1}(1+D)}{(1-D)} - \frac{I_0(b')}{(1-D)^3} - (V_{FD1} + V_{FD2}), \tag{41}$$

where

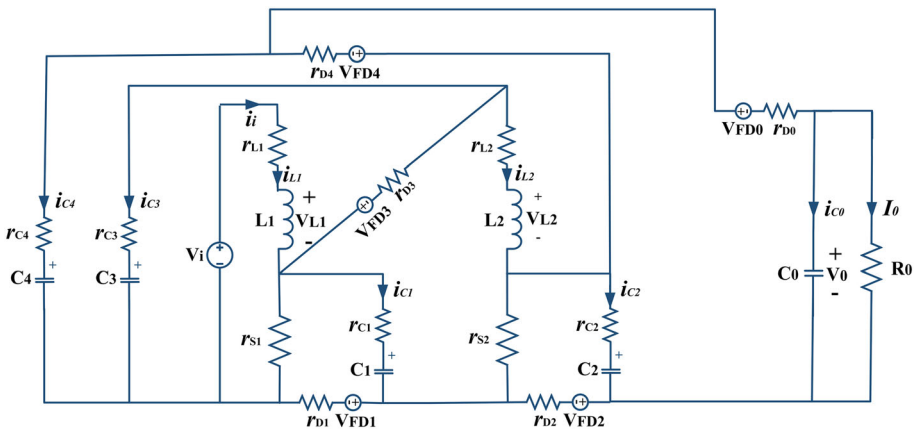


FIGURE 10 Equivalent circuit of ASC-QBC-II converter with element parasitics

$$b' = \frac{r_{L2}2(1-D) + r_S D(1-D^2) - r_C 2D(1-D) + r_S\{D(1+3D) + D(1-D^2)\} + r_{D1}2D(1-D)}{(1-D)^2}. \tag{42}$$

Since

$$V_0 = 2V_{C2} + V_{C1}. \tag{43}$$

Using (40) and (41) in the above equation, the output voltage of ASC-QBC-II converter under the influence of parasitic parameters is written as

$$V_0 = \frac{\frac{V_i(3+D)}{(1-D)^2} - DV_{FD0} - 3V_{FD1} - 2V_{FD2}}{1 + a'\left(\frac{r_{L1}}{R_0}\right) + b'\left(\frac{r_{L2}}{R_0}\right) + c'\left(\frac{r_C}{R_0}\right) + (d' + e')\left(\frac{r_S}{R_0}\right) + f'\left(\frac{r_{D0}}{R_0}\right) + g'\left(\frac{r_{D1}}{R_0}\right) + h'\left(\frac{r_{D2}}{R_0}\right)}, \tag{44}$$

where

$$a' = \frac{3+D}{(1-D)^3} \quad b' = \frac{4}{(1-D)^2} \quad c' = \frac{D^3 + D^2 - 6D + 4}{D(1-D)^2} \quad d' = \frac{(1+3D)(4-D)D}{(1-D)^3}$$
$$e' = \frac{D(3+D)}{(1-D)} \qquad f' = D \qquad g' = \frac{6D}{(1-D)^2} \qquad h' = \frac{2D}{(1-D)}.$$

Using (44), the efficiency of the proposed converter can be written as

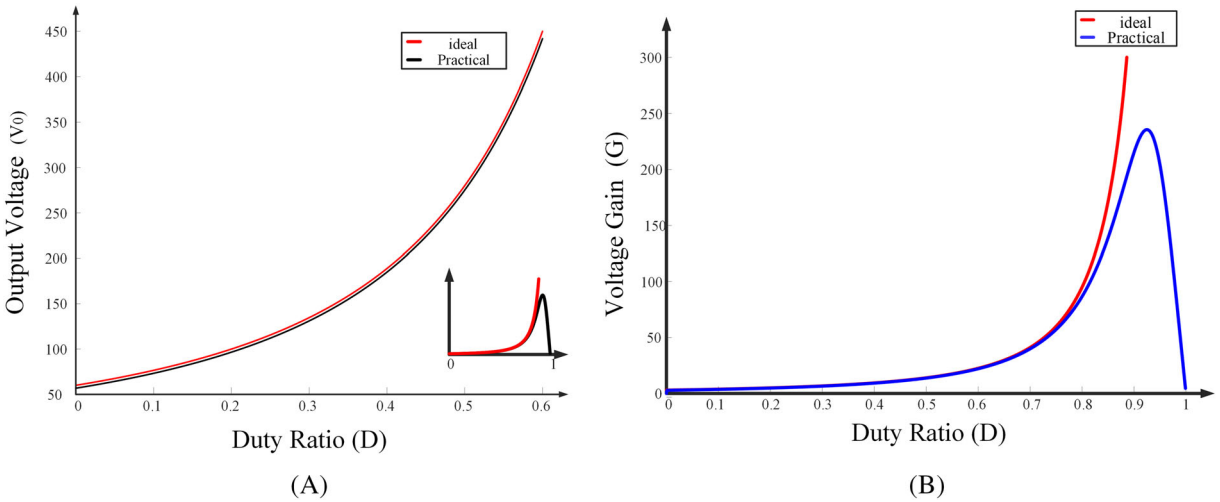


FIGURE 11 ASC-QBC-II converter nonideal: (A) terminal voltage; (B) voltage gain with element parasitics

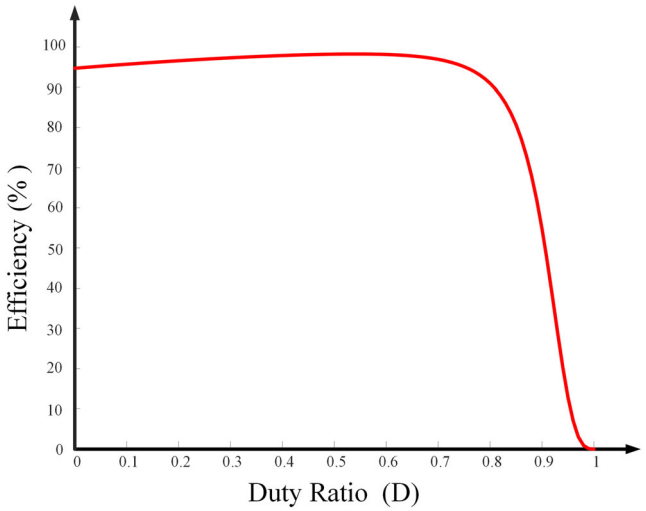


FIGURE 12 Efficiency versus duty ratio with element parasitics of ASC-QBC-II converter

$$\eta = \frac{1 - \left(\frac{DV_{FD0} + 3V_{FD1} + 2V_{FD2}}{V_{0-ideal}}\right)}{1 + a'\left(\frac{r_{L1}}{R_0}\right) + b'\left(\frac{r_{L2}}{R_0}\right) + c'\left(\frac{r_C}{R_0}\right) + (d' + e')\left(\frac{r_S}{R_0}\right) + f'\left(\frac{r_{D0}}{R_0}\right) + g'\left(\frac{r_{D1}}{R_0}\right) + h'\left(\frac{r_{D2}}{R_0}\right)}. \tag{45}$$

The ASC-QBC-II converter nonideal terminal voltage, voltage gain and efficiency under the influence of element parasitics are as shown in Figures 11 and 12, respectively. As mentioned in the previous converter, the observed voltage gain and efficiency from these plots are in good accord with the experimental values.

5 | CONTROL PERFORMANCE

The proposed converters control performance for varying input voltage and load conditions is done by standard state space modeling. Since the ripple voltage and instantaneous current profile of capacitors C_1 and C_2 are identical, hence instead of these two state variables, only one is considered. The small signal model of ASC-QBC-I converter is represented by the following equations

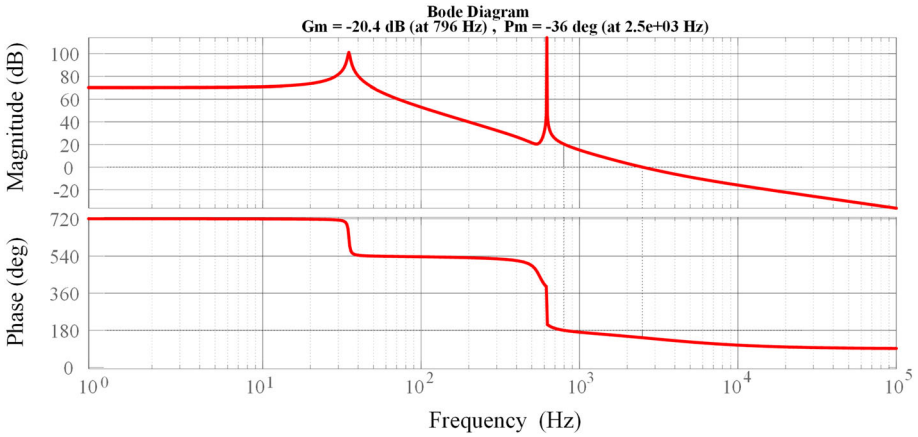
$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_C(t)}{dt} \\ \frac{d\hat{v}_{C0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d)}{L_1} & 0 \\ 0 & 0 & \frac{(1+d)}{L_2} & \frac{-(1-d)}{L_2} \\ \frac{(1-d)}{2C} & \frac{-(1+d)}{2C} & 0 & 0 \\ 0 & \frac{(1-d)}{C_0} & 0 & \frac{-1}{R_0C_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_C(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_i(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} \\ \frac{-1}{2C} & \frac{-1}{2C} & 0 & 0 \\ 0 & \frac{-1}{C_0} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_C \\ V_{C0} \end{bmatrix} \hat{d} \tag{46}$$

$$v_0(t) = [0 \;\; 0 \;\; 0 \;\; 1]\left[\hat{i}_{L1}(t) \;\; \hat{i}_{L2}(t) \;\; \hat{v}_C(t) \;\; \hat{v}_{C0}(t)\right]^T \tag{47}$$

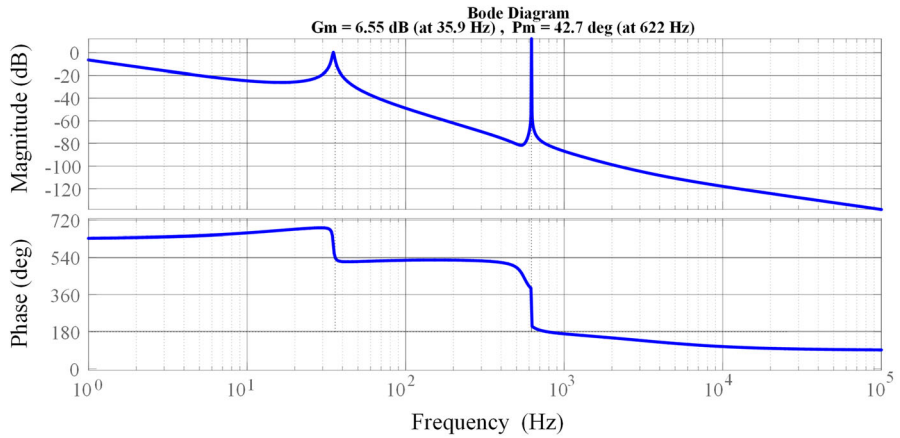
By using (46) and (47), the open loop control to output transfer function is written as

$$\left(\frac{\hat{v}_0(s)}{\hat{d}(s)}\Big|_{\hat{v}_i(s)=0}\right) = \frac{-2.796\times10^{28}\,s^3 + 5.708\times10^{32}\,s^2 - 6.967\times10^{35}\,s + 6.895\times10^{39}}{2.909\times10^{24}\,s^4 + 1.818\times10^{35}\,s^3 + 4.455\times10^{31}\,s^2 + 2.765\times10^{32}\,s + 2.146\times10^{36}}. \tag{48}$$

For the above-stated open loop transfer function bode plot is as shown in Figure 13A. The stable operation of the converter is achieved by using a single loop output voltage control as specified in (49), and bode plot for the corresponding closed-loop ASC-QBC-I converter is shown in Figure 13B.



(A)



(B)

FIGURE 13 Bode plot of ASC-QBC-I converter: (A) open loop and (B) closed loop

$$G_C(s) = K_p + \frac{K_i}{s}, \tag{49}$$

where

$$\begin{cases} \mathrm{K_p} = 0.0008 \\ \mathrm{K_i} = 0.00092 \end{cases}$$

The invalid state variables of a loop that contains all capacitors in ASC-QBC-II converter are avoided by using a small resistance of r (0.01 Ω) in that loop. The small signal modeling of the aforementioned converter is as follows

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{C1}(t)}{dt} \\ \frac{d\hat{v}_{C2}(t)}{dt} \\ \frac{d\hat{v}_{C3}(t)}{dt} \\ \frac{d\hat{v}_{C0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d)}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-r}{L_2} & \frac{1}{L_2} & \frac{-(1-d)}{L_2} & \frac{d}{L_2} & 0 \\ \frac{(1-d)}{C} & \frac{-1}{C} & \frac{-1}{Cr} & \frac{-2d}{Cr} & \frac{(1-d)}{Cr} & \frac{d(R_0-r)}{CR_0r} \\ 0 & \frac{(1-d)}{2C} & \frac{-d}{Cr} & \frac{-2d}{Cr} & 0 & \frac{d(R_0-r)}{CR_0r} \\ 0 & \frac{-d}{C} & \frac{(1-d)}{Cr} & 0 & \frac{-(1-d)}{Cr} & 0 \\ 0 & 0 & \frac{d}{Cr} & \frac{2d}{Cr} & 0 & -\left(\frac{d(R_0+r)}{CR_0r} + \frac{1-d}{C_0R_0}\right) \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C3}(t) \\ \hat{v}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_i(t)$$
$$+ \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} & 0 \\ \frac{-1}{C} & 0 & 0 & \frac{-2}{Cr} & \frac{-1}{Cr} & \frac{R_0-r}{CR_0r} \\ 0 & \frac{-1}{2C} & \frac{-2}{Cr} & \frac{-2}{Cr} & \frac{-1}{Cr} & \frac{R_0-r}{CR_0r} \\ 0 & \frac{-1}{C} & \frac{-1}{Cr} & 0 & \frac{1}{Cr} & 0 \\ 0 & 0 & \frac{1}{Cr} & \frac{2}{Cr} & 0 & \frac{-(R_0+r)}{CR_0r} + \frac{1}{R_0C_0} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C0} \end{bmatrix} \hat{d}$$

$$v_0(t) = [0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 1]\left[\hat{i}_{L1}(t) \;\; \hat{i}_{L2}(t) \;\; \hat{v}_{C1}(t) \;\; \hat{v}_{C2}(t) \;\; \hat{v}_{C3}(t) \;\; \hat{v}_{C0}(t)\right]^T$$

By using the aforementioned small signal model of the ASC-QBC-II converter, the open loop control to output transfer function is written as

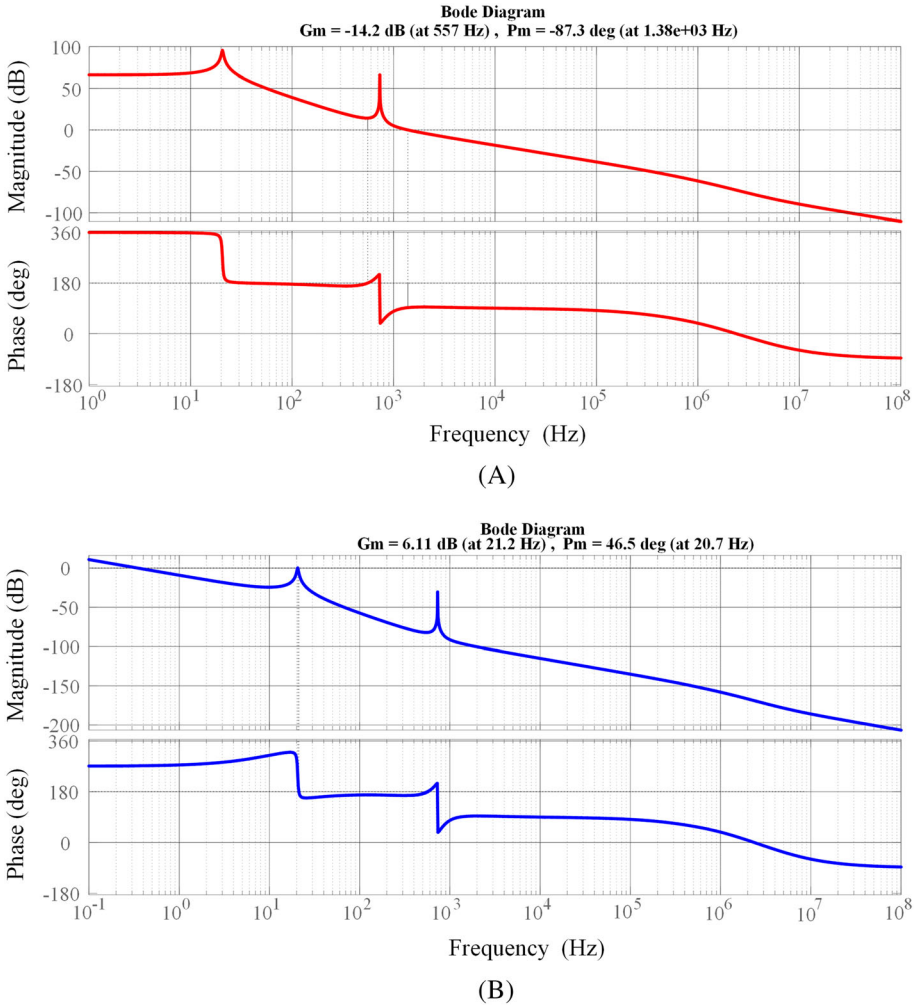


FIGURE 14 Bode plot of ASC-QBC-II converter: (A) open loop; (B) closed loop

$$\left(\frac{\widehat{v_0(s)}}{\widehat{d(s)}}\Big/_{\widehat{v_i}(s)=0}\right)=\frac{2.714\times10^{58}\,s^5-6.416\times10^{65}\,s^4-2.696\times10^{72}\,s^3+4.316\times10^{75}\,s^2-3.298\times10^{79}\,s+2.558\times10^{83}}{1.379\times10^{55}\,s^6+1.652\times10^{62}\,s^5+3.617\times10^{68}\,s^4+6.079\times10^{69}\,s^3+7.652\times10^{75}\,s^2+3.315\times10^{76}\,s+1.278\times10^{80}}. \quad (50)$$

A suitable PI controller with $K_p = 0.00015$ and $K_i = 0.0011$is used to acquire stable output voltage against perturbations in input voltage and output load conditions. The open loop and closed loop bode plots for the ASC-QBC-II converter are shown in Figure 14A,B.

6 | COMPARISON OF PROPOSED CONVERTERS WITH OTHER HIGH VOLTAGE GAIN CONVERTERS

The superiority of the proposed converters can be verified by the performance indices, i.e., voltage gain, semiconductor individual and total voltage stress, peak current stress on the switches, and component count as shown in Table 5.

TABLE 5 Performance Comparison

Topology	Voltage Gain	Normalized Switch Voltage Stress	Normalized Diode Voltage Stress	Normalized Total Voltage Standing	η_{max} or $\eta_{operating}$	Common Ground	Input Current	Switch Current Stress	L/C/S/D (Total)
Ref [22]	$\frac{D^2-3D+3}{(1-D)^2}$	$\frac{2-D}{D^2-3D+3}$ $D=\frac{(2G-3)-\sqrt{4G-3}}{2(G-1)}$	$\frac{5-3D}{D^2-3D+3}$	$\frac{7-4D}{D^2-3D+3}$	96.7%	YES	Pulsating	$\frac{D^2-3D+3}{(1-D)^2}$	2/3/2/3 (10)
Ref [23]	$\frac{1}{(1-D)^2}$	$\frac{1+\sqrt{G}}{\sqrt{G}}$	$\frac{2+\sqrt{G}}{\sqrt{G}}$	$\frac{3+2\sqrt{G}}{\sqrt{G}}$	93%	YES	Pulsating	$\frac{1}{(1-D)^2}$	2/2/2/2 (8)
Ref [24]	$\frac{1}{(1-D)^2}$	1	2	3	92.5%	YES	Non Pulsating	$\frac{2-D}{(1-D)^2}$	2/2/1/3 (8)
Ref [25]	$\frac{2-D}{(1-D)^2}$	$\frac{1}{2-D}$ $D=1-\frac{2}{G}-\sqrt{\frac{1}{4G^2}+\frac{1}{G}}$	$\frac{3}{2-D}$	$\frac{4}{2-D}$	95%	YES	Pulsating	$\frac{2-D}{(1-D)^2}$	2/3/1/4 (10)
Ref [26]	$\frac{2+D}{(1-D)^2}$	$\frac{2G-1+\sqrt{1+12G}}{6G+1-\sqrt{1+12G}}$	$\frac{8G-1+\sqrt{1+12G}}{6G+1-\sqrt{1+12G}}$	$\frac{2\left(5G-1+\sqrt{1+12G}\right)}{6G+1-\sqrt{1+12G}}$	95.22%	NO	Non Pulsating	$\frac{2+D}{(1-D)^2}$	3/6/2/5 (16)
Ref [27]	$\frac{5-D}{1-D}$	$\frac{2(G-1)}{3G}$	$\frac{8(G-1)}{3G}$	$\frac{10(G-1)}{3G}$	97.06%	YES	Pulsating	$\frac{5-D}{2(1-D)}$	3/5/2/4 (14)
Ref [28]	$\frac{1}{(1-D)^2}$	1	$2-\frac{1}{G}$	$3-\frac{1}{G}$	93%	YES	Pulsating	$\frac{2-D}{(1-D)^2}$	2/2/1/3 (8)
Ref [29]	$\frac{1}{(1-D)^2}$	1	2	3	93.11%	YES	Pulsating	$\frac{2-D}{(1-D)^2}$	2/2/1/3 (8)
Ref [30]	$\frac{1}{(1-D)^2}$	1	2	3	95.5%	YES	Pulsating	$\frac{1}{(1-D)^2}$	2/2/1/3 (8)
Ref [31]	$\frac{3-D}{1-D}$	$\frac{(G-1)}{2G}$	$\frac{4(G-1)}{2G}$	$\frac{5(G-1)}{2G}$	95.5%	YES	Pulsating	$\frac{3-D}{1-D}$	1/4/1/4 (10)
Ref [32]	$\frac{1+D-D^2}{(1-D)^2}$	$\frac{2-D}{1+D-D^2}$ $D=\frac{(2G+1)-\sqrt{8G+5}}{2(G+1)}$	$\frac{3-2D^2}{1+D-D^2}$	$\frac{5-D-2D^2}{1+D-D^2}$	93.7%	NO	Pulsating	$\frac{2D-D^2}{(1-D)^2}$	2/2/2/2 (8)
Ref [33]	$\frac{2(2-D)}{(1-D)^2}$	$\frac{2}{2(2-D)}$ $D=\frac{(2G-2)-\sqrt{8G+4}}{2G}$	$\frac{7-3D}{2(2-D)}$	$\frac{9-3D}{2(2-D)}$	94.5%	YES	Non Pulsating	$\frac{3-D^2}{D(1-D)^2}$	2/5/2/5 (14)
ASC-QBC-I	$\frac{1+D}{(1-D)^2}$	$\frac{2}{1+D}$ $D=\frac{2G+1-\sqrt{8G+1}}{2G}$	$\frac{3-D}{1+D}$	$\frac{5-D}{1+D}$	95%	NO	Pulsating	$\frac{1+D}{(1-D)^2}$	2/3/2/3 (10)
ASC-QBC-II	$\frac{3+D}{(1-D)^2}$	$\frac{2}{3+D}$	$\frac{7-D}{3+D}$ $D=\frac{(2G+1)-\sqrt{16G+1}}{2G}$	$\frac{9-D}{3+D}$	94%	NO	Non Pulsating	$\frac{1+3D}{D(1-D)^2}$	2/5/2/5 (14)

L= Inductor count, C= Capacitor count, S= Switch count, D= Diode count

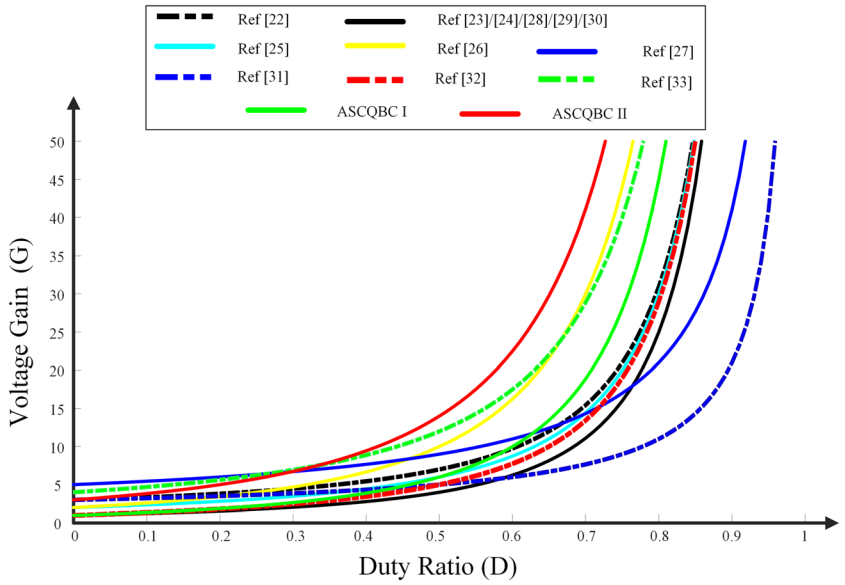


FIGURE 15 Voltage gain comparison with similar converters

6.1 | Voltage gain

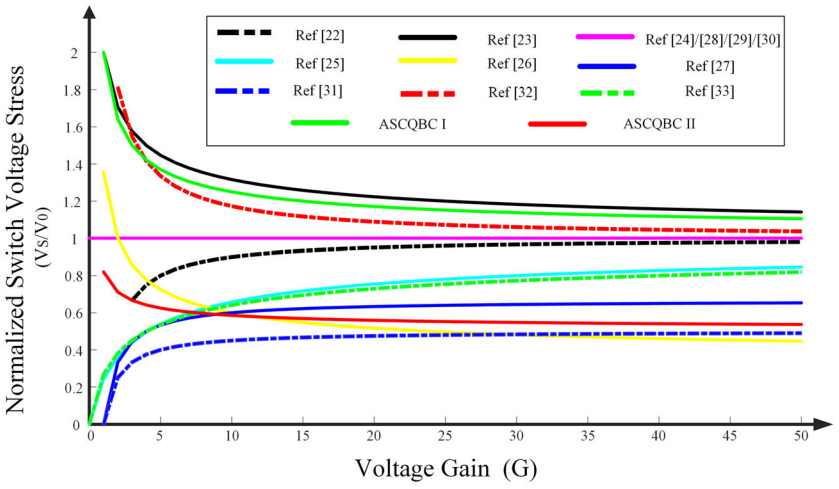
The voltage conversion factor is the prominent performance index in DC-DC converters. Hence, the comparison of different converter voltage gain concerning the variation in duty ratio is shown in Figure 15. From the plot, it is observed that the ASC-QBC-II converter has superior performance to all other converters, and ASC-QBC-I voltage gain is slightly less compared to the converters in Jalilzadeh et al.[26] and Khan et al.[33] The voltage gains of converters in previous studies[23-24,27,28-31] are far less than with other converters. However, if we consider voltage gain per component count then ASC-QBC- I, II performance is superior to all other converters.

6.2 | Element voltage stress

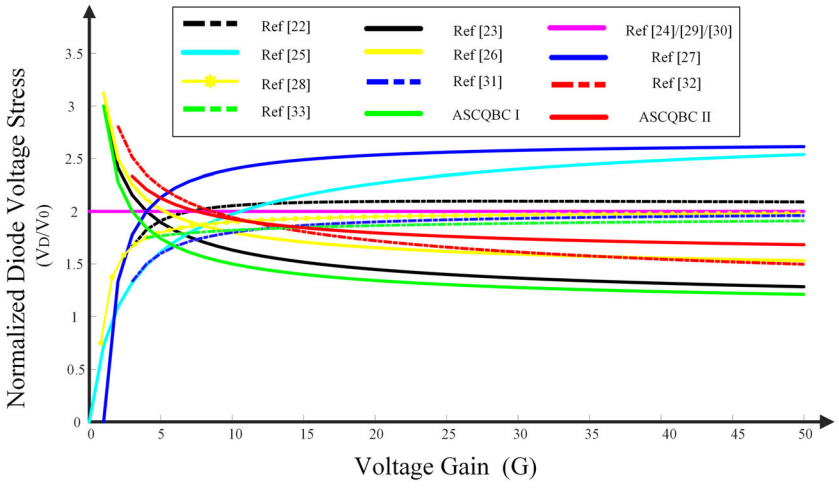
The element voltage stress is a crucial parameter for semiconductor element selection and inductor-capacitor design. This element voltage stress comparison is demonstrated in three different factors, normalized switch voltage stress (NSVS, v_S/v_0), normalized diode voltage stress (NDVS, v_D/v_0) and normalized total voltage standing (NTVS).

The NSVS of ASC-QBC-I is moderate as shown in Figure 16A. This is because the switch at the load end has to block the entire output voltage. In this regard, the ASC-QBC-II performance is superior, with an NSVS of around 0.5. In comparison to ASC-QBC-II, the remaining converters will have high NSVS expect the converter in Jalilzadeh et al.[26] and Li et al.[31]

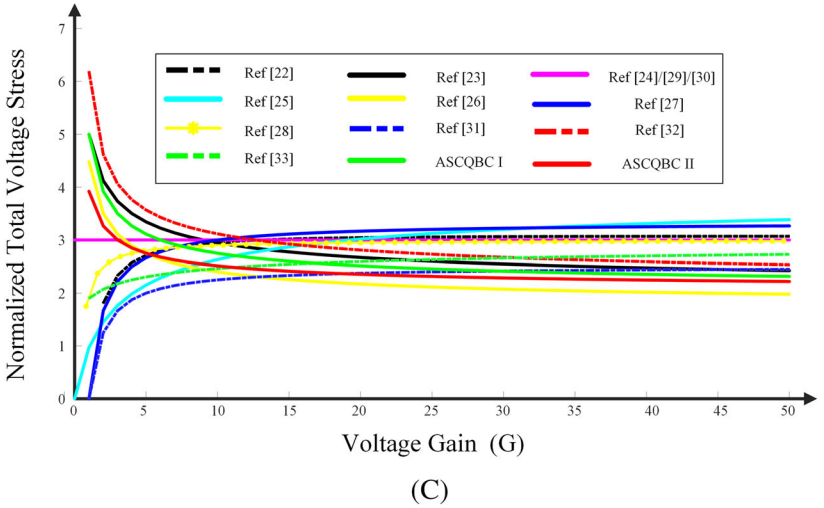
The NDVS for ASC-QBC-I is the lowest among all, whereas ASC-QBC-II performance is moderate by having NDVS factor less than 2 as shown in Figure 16B. It is interesting to note that even though the performance in NDVS and NSVS of ASC-QBC-I, II are not very much superior to other converters, but when it comes to NTVS, the proposed two converters' performance is substantially improved from that of other converters, as shown in Figure 16C.



(A)



(B)



(C)

FIGURE 16 Normalized voltage stress comparison of (A) switches, (B) diodes, and (C) total voltage standing

6.3 | Element current stress

The peak switch current stress $\left(\widehat{I}_s/I_0\right)$ with respect to output current as shown in Figure 17. For duty ratios greater than 0.6, the ASC-QBC-II converter will experience considerable current stress. This is the reason because of which the

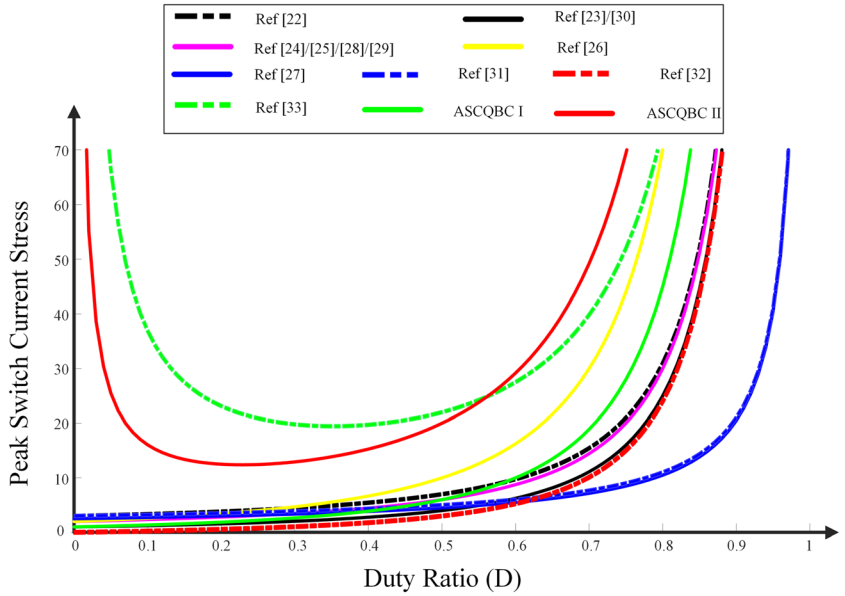
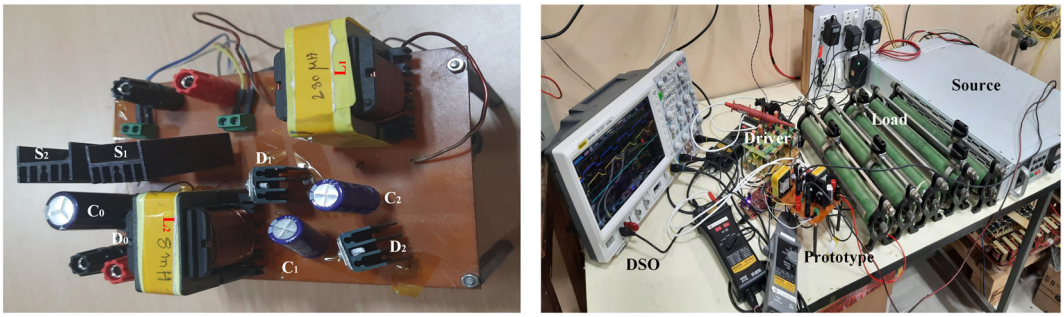


FIGURE 17 Switch current stress comparison

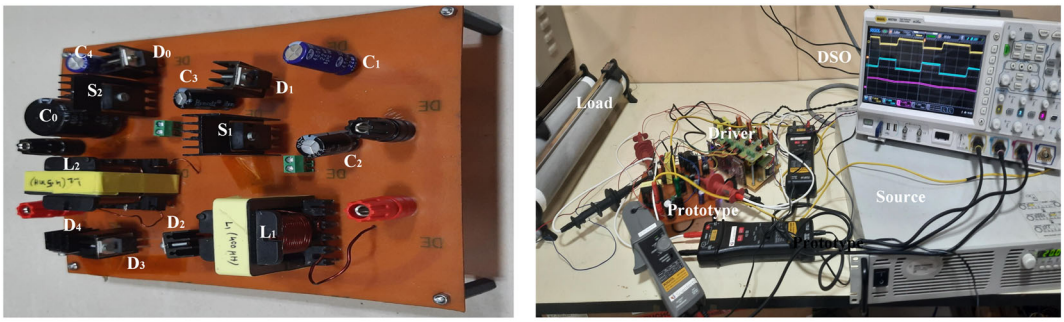
TABLE 6 Design specifications

Specification	ASC-QBC-I	ASC-QBC-II
Power	100 W	100 W
Input voltage	20 V	20 V
Output voltage	400 V	400 V
Inductors	$L_1 = 280$ μH, $L_2 = 8$ mH	$L_1 = 400$ μH, $L_2 = 4.5$ mH
capacitors	$C_0 = 100$ μF, C_1-$C_2 = 22$ μF	$C_0 = 220$ μF,C_1-$C_4 = 22$ μF



(A) (B)

FIGURE 18 ASC-QBC-I converter: (A) prototype; (B) experimental setup



(A) (B)

FIGURE 19 ASC-QBC-II converter: (A) prototype; (B) experimental setup

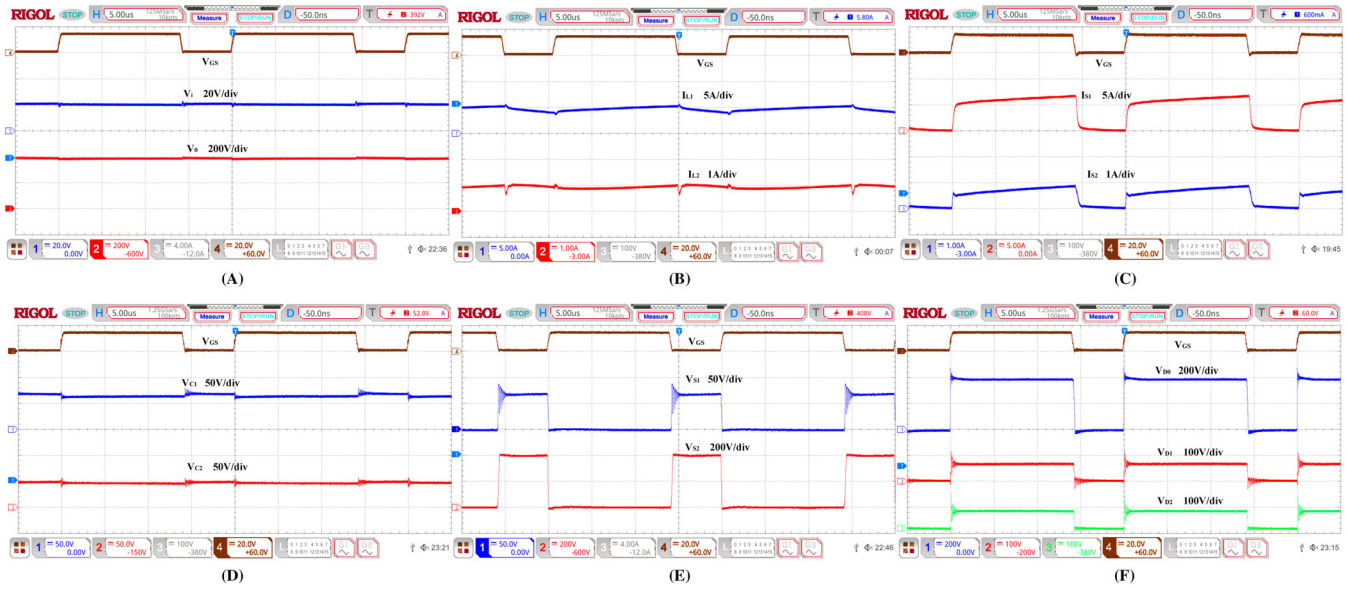


FIGURE 20 (ASC-QBC-I). (A) Input and output voltage (V_i and V_0); (B) inductor currents (i_{L1} and i_{L2}); (C) switch Currents (i_{S1} and i_{S2}); (D) capacitor voltages (V_{C1} and V_{C2}); (E) switch voltages (V_{S1} and V_{S2}); (F) diode voltages ($V_{D0} - V_{D2}$)

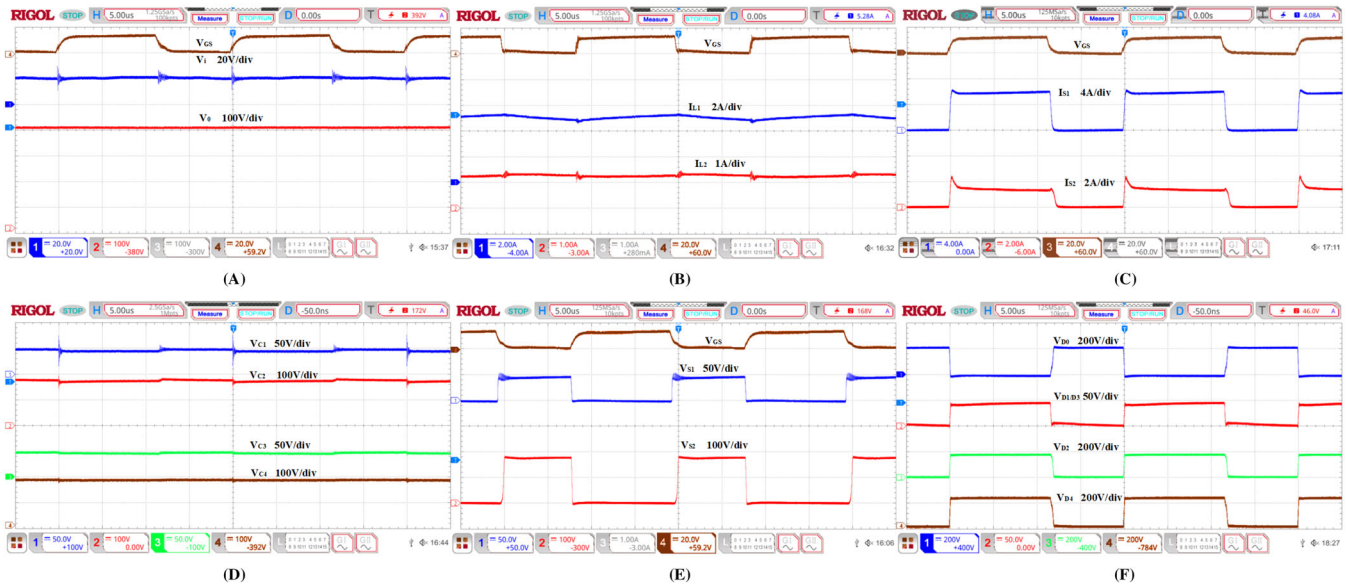


FIGURE 21 (ASC-QBC-II). (A) Input and output voltage (V_i and V_0); (B) inductor currents (i_{L1} and i_{L2}); (C) switch currents (i_{S1} and i_{S2}); (D) capacitor voltages ($V_{C1} - V_{C4}$); (E) switch voltages (V_{S1} and V_{S2}); (F) diode voltages ($V_{D0} - V_{D4}$).

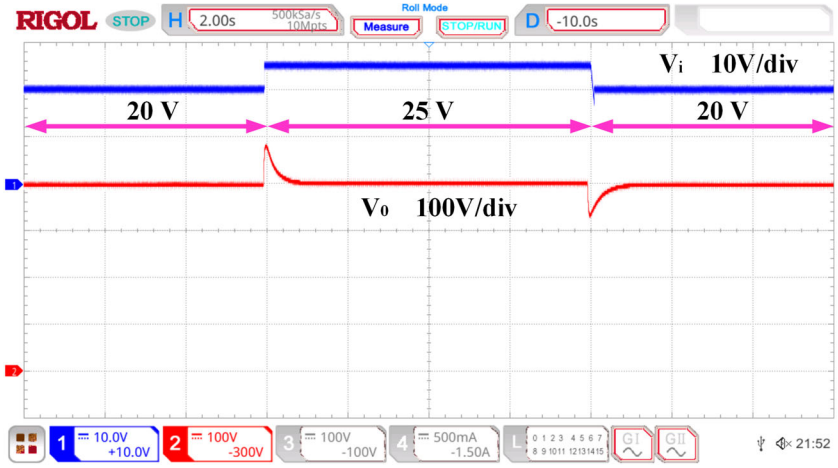
ASC-QBC-II converter is operated at a duty ratio of 0.577 in order to maintain a low current stress factor. The ASC-QBC-I converter current stress is moderate (at 20) with respect to the remaining converters.

6.4 | Miscellaneous performance indices

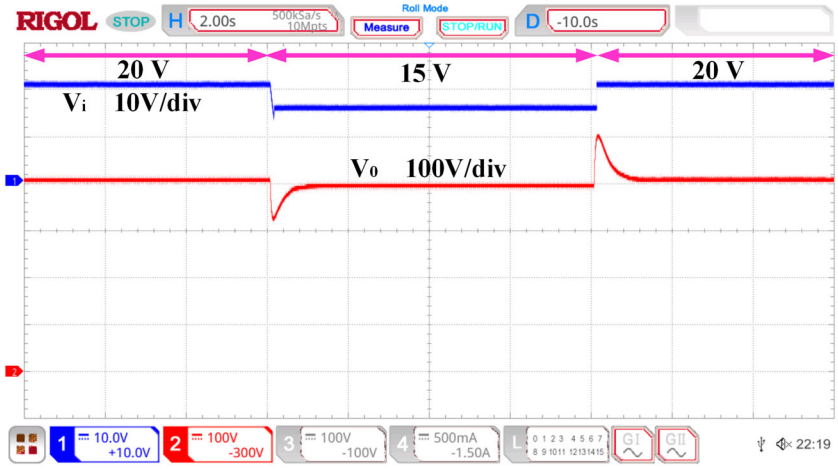
The overall component count (10) is moderate for the converter ASC-QBC-I, and for ASC-QBC-II, it is bit higher (14). This elevated component count can be justified by the fact that superiority in voltage gain at a low duty ratio. The only demerit of ASC-QBC-I, II is the lack of common ground between the source and the load. The ASC-QBC-II will have a very small amount of ripple current at the input terminals.

7 | EXPERIMENTAL VALIDATION

The theoretical analysis validation of ASC-QBC-I, II converters is done by fabricating the laboratory prototypes with the specifications mentioned in Table 6 and as shown in Figures 18 and 19. The applied input voltage for both the



(A)



(B)

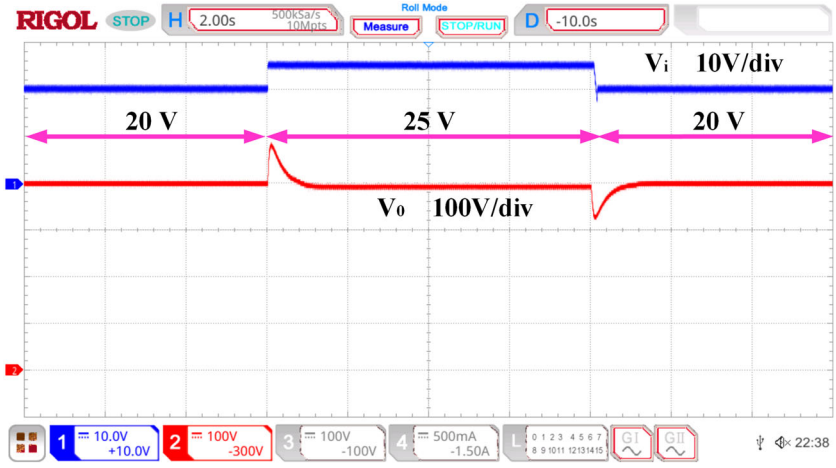
FIGURE 22 Closed loop performance of ASC-QBC-I converter for step variation in input voltage: (A) 20–25–20 V; (B) 20–15–20 V

converters is 20 V for which the output voltages obtained are 391 and 388 V as shown in Figures 20A and 21A, attaining an ultra-gain of 19.55 and 19.4 respectively. The average input current for both the converters observed to be 5.01 and 5.05 A making the operating efficiencies 95% and 94%, respectively.

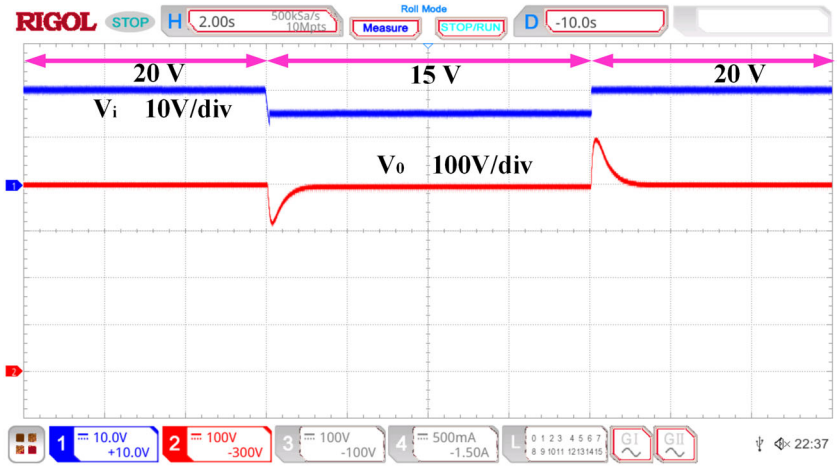
The inductor currents of the ASC-QBC-I and II converters are as shown in Figures 20B and 21B. since both the inductor currents are added in ASC-QBC-I to get the source current, the ripple content is high, whereas the source current passes through the inductor L_1 in the ASC-QBC-II converter and hence the ripple content is less. The switch current waveforms are as shown in Figure 20C and 21C. The peak current stress for the switches S_1, S_2 in ASC-QBC-I observed to be 6.5 A and 1.5 A and that of ASC-QBC-II are 6.4 A and 1.4 A, respectively.

The capacitor voltages of ASC-QBC-I, II are in good agreement with the ideal wave shapes as shown in Figures 20D and 21D. The average value of these capacitor voltages are almost near to their ideal case, with a smaller variance in the experimental state.

The voltage stress of diodes (D_0-D_2) and switches (S_1-S_2) in ASC-QBC-I are 391 V for V_{D0}, V_{S2} and 70 V for V_{D1}, V_{D2}, V_{S2} as shown in Figure 20E,F. Similarly, for the ASC-QBC-II converter, the diode-switch voltage stresses are as follows: 220 V for V_{D0}, 45 V for V_{D1}, V_{D3}, 175 V for V_{D2}, 230 V for V_{D4}, Switch S_1 with 45 V, and Switch S_2 at 180 V as shown in Figure 21E,F.



(A)

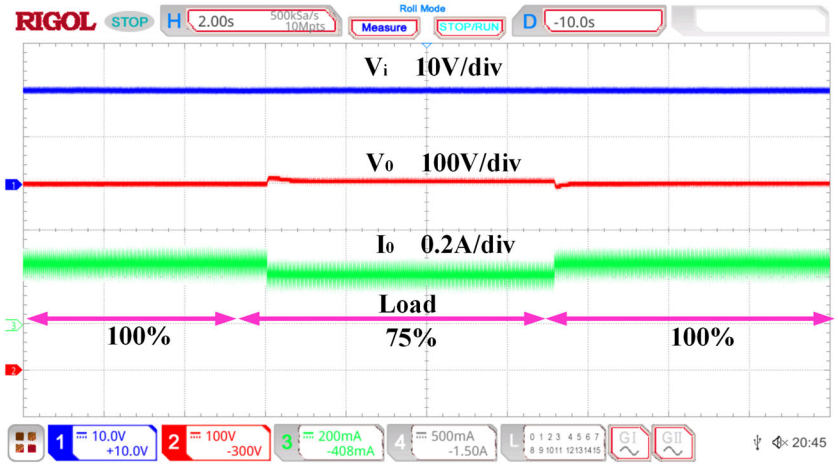


(B)

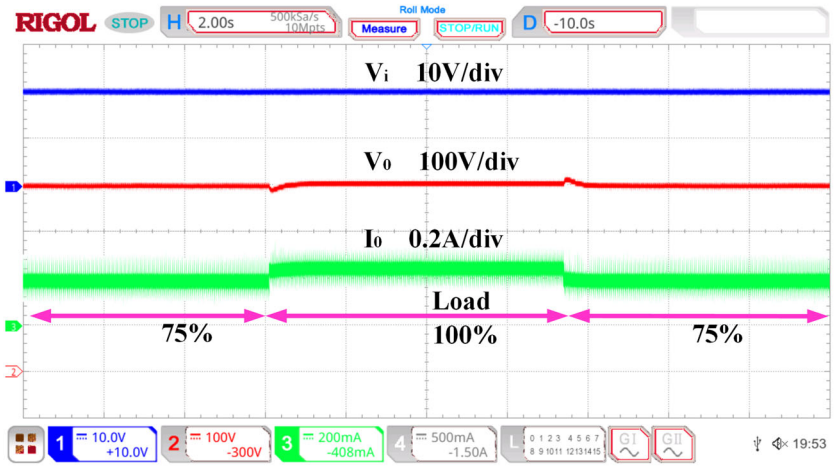
FIGURE 23 Closed loop performance of ASC-QBC-II converter for step variation in input voltage: (A) 20–25–20 V; (B) 20–15–20 V

The experimental validation of closed-loop performance is carried out for both the proposed converters at 100 W power rating with the aid of TMS320F28379D processor. The feasibility of stated converters to maintain a stiff output voltage at 400 V against the step variation of input voltage i.e., 20–25–20 V and 20–15–20 V is shown in Figure 22A,B for ASC-QBC-I converter, and for ASC-QBC-II converter, it is shown in Figure 23A, B. The perturbations of load are also taken into consideration by varying it from 75% to 100% as shown in Figure 24A,B for the two converters, respectively, attaining a steady voltage of 400 V at the output terminals.

The theoretical losses are calculated by using thermal analysis on PSIM platform with the specifications of the selected devices for the proposed topologies. The theoretical and experimental efficiency variations for different load powers are plotted as shown in Figure 25A,B. The maximum efficiencies for both the proposed converters are 95.15% and 94.2%, whereas the operating efficiencies for 100 W rating are 95% and 94%, respectively. The various types of losses and their distribution for the proposed converters are shown in Table 7. The loss distribution wheel for ASC-QBC- I, II as shown in Figure 26A,B, where in ASC-QBC-I the majority portion of losses is due to switches (58%) and in ASC-QBC-II is due to diodes (49%).



(A)



(B)

FIGURE 24 Closed loop performance of (A) ASC-QBC-I; (B) ASC-QBC-II converters for step variations in load

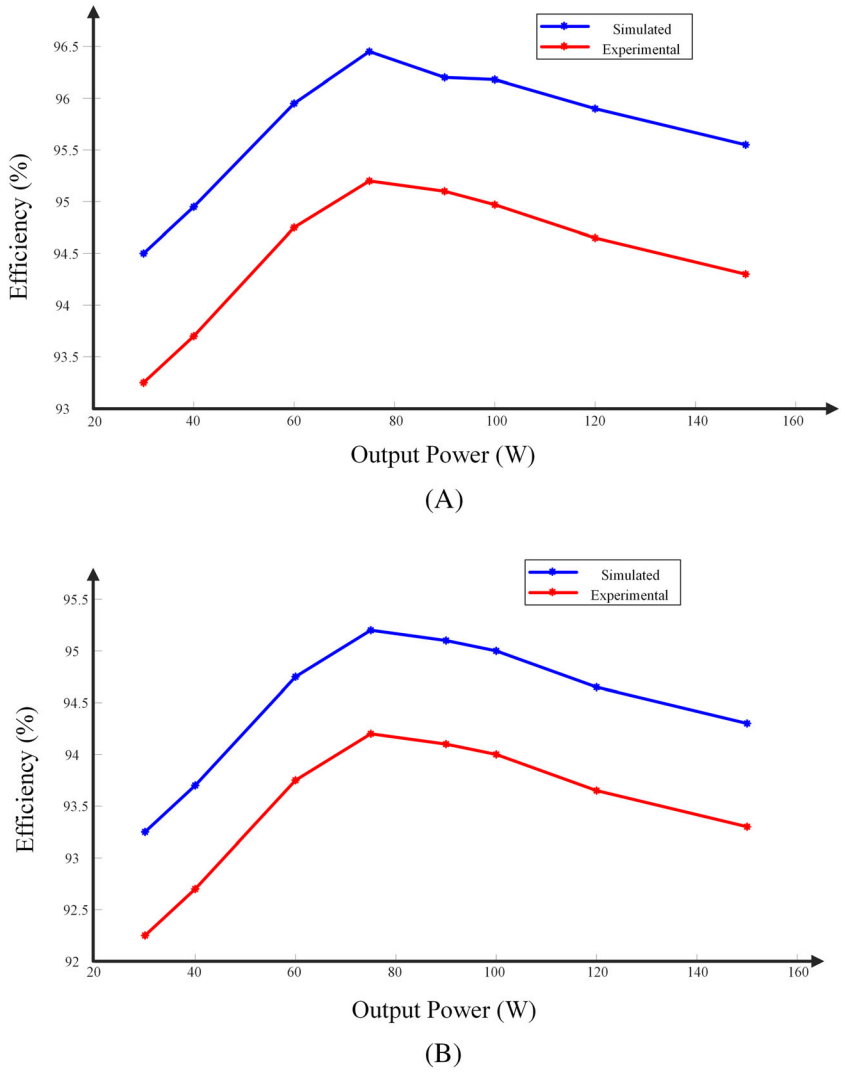


FIGURE 25 Efficiency versus output power of (A) ASC-QBC-I; (B) ASC-QBC-II converters

TABLE 7 Power loss distribution and comparison

		ASC-QBC-I		ASC-QBC-II	
Element	**Loss**	**Theoretical (W)**	**Practical (W)**	**Theoretical (W)**	**Practical (W)**
Inductor (ESR)	Conduction	0.67	0.876	1.12	1.388
Capacitor (ESR)	Conduction	0.058	0.038	0.058	0.0615
MOSFET (R_{DS} ON)	Conduction	1.1	1.655	0.485	0.6
MOSFET (switching)	Switching loss	1.07	1.27	0.89	1.009
Diodes (internal resistance)	Conduction	0.212	0.312	0.502	0.619
Diodes (forward drop)	Forward Drop loss	0.68	0.883	1.785	2.385

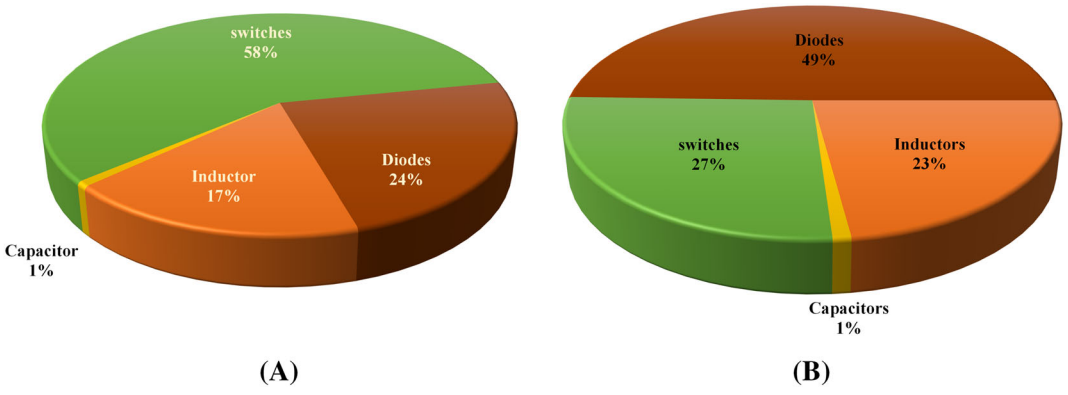


FIGURE 26 Loss distribution of (A) ASC-QBC-I; (B) ASC-QBC-II converters

8 | CONCLUSION

In this paper, an active switched capacitor based ultra-voltage gain quadratic boost converters have been presented. The theoretical steady-state analysis along with operating modes have been discussed. Moreover, to enlighten the merits of the proposed converters, a comparative analysis with similar quadratic boost and other high voltage gain topologies was done. Furthermore, from the experimental validation, it is evident that the ASC-QBC- I and II converters assimilated numerous merits such as ultra-gain, low overall component stress, low input current ripple (ASC-QBC-II), and low current stress for the switches. The green energy source-excited input current ripple aspects were experimentally demonstrated for both the proposed converters. The control performance of the converters with state space modeling was experimentally validated at a power rating of 100 W against the source voltage and load perturbations. As a proof of concept, a laboratory prototype was fabricated to validate the performance indices of the proposed converters.

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DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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