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Nonisolated high gain hybrid switched-inductor DC-DC converter with common switch grounding

M. F. Baba | **A. V. Giridhar** | **B. L. Narasimharaju**

Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India

Correspondence
M. F. Baba, Department of Electrical Engineering, National Institute of Technology, Warangal, Telangana 506004, India.
Email: mfbaba@student.nitw.ac.in

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Abstract

This paper presents a methodology that integrates the hybrid switched inductor (HSL) and split duty ratio techniques to synthesize a high gain converter with common switch grounding (HSL-CSG). The DC-DC converter's high gain feature is required for microsource power processing in low voltage renewable energy systems. The amplification in voltage gain of the proposed converter is achieved without using transformer, common core coupled inductors, voltage multipliers, intermediate capacitors, and voltage lifting methods so that the topology is simple in construction and operation. Moreover, with a split duty ratio the proposed converter switches are less prone to current stress due to reduction in extreme conducting duty intervals. The topological derivation, operating principle, analysis of both continuous conduction mode (CCM), and discontinuous conduction mode (DCM) are presented. The theoretical analysis is validated with the aid of a laboratory prototype.

KEYWORDS

hybrid switched inductor, long conducting duty cycle, nonisolated high gain DC-DC converter, split duty converter

1 | INTRODUCTION

Proliferation of green energy sources in the energy sector[1] becoming prominent and led to a greater reduction in the usages of conventional fossil fuels[2] for electric power generation. In recent times, data centers and telecommunication companies rely on photovoltaic (PV) energy in addition to the grid to meet the increased power demand and economical operation. Renewable energy sources require a power electronic interface[3,4] to deliver power to the DC grid[5,6] with satisfactory performance indices in terms of power quality. The power flow in DC microgrid in most of the times is unidirectional except the case with energy storage systems, and hence, the control is simple.[7] These sources, also known as microsources,[8] can be functional as independent and controllable when they are connected to the grid or operated in islanded mode. These microsources not only supply to the local load but also inject excess power to the grid via power conditioning or power electronic interface. The power electronic interface contains AC-DC conversion with power factor correction, DC-DC converters to maintain DC voltage profile, and DC-AC conversion to comply with the AC grid or load requirements. The output voltage of these microsources is small, and it would not comply with the grid integration requirements. Hence, high voltage amplification is required by the power processing converter to comply these microsources for grid integration. In addition to the grid integration, the voltage gain provided by these DC-DC converters is quite ample so that they are also used in the applications like data centers, telecommunication, lighting in automobiles, uninterruptible power supplies battery backup system, electric traction, and medical applications. The precise applications of the proposed topology in terms of power rating, input and output voltages are, street lightning: <200 W, <20 V,

<100 V; automobile head light: <200 W, <20 V, <100 V; LED lighting: <100 W, <20 V, <100 V; wireless transfer of power: <200 W, <20 V, <100 V.

The amplification of voltage can be done with two types of converters, that is, isolated and nonisolated. In isolated topologies to get the required voltage gain turns, ratio of the transformer is increased. Numerous drawbacks in isolated converters are as follows: the leakage inductance in high frequency transformer causes voltage spikes in the active switches, increased voltage stress across output diode, lower efficiency especially when operated for higher gains,[9] pulsating current at input terminals which makes them nonsuitable to PV applications because it reduces the life of PV array.[10] Recent dual active bridge topologies are capable of achieving zero voltage switching by the integration of resonant converters at fixed or variable frequency modulation. Some of the aforementioned demerits in isolated topologies can be overcome by adopting rectifiers, voltage doublers-quadruplers at the secondary side and more over reverse power flow, circulating currents can also completely eliminated as mentioned in Mustafa et al.[11]

Numerous voltage amplification techniques based on conventional boost converters,[12] switched inductors,[13–15] switched capacitors,[16–19] coupled inductors,[20–23] cascaded connections,[24,25] quadratic boost,[26] voltage lift,[27,28] voltage multiplier with capacitor-diode combination,[29,30] hybrid switched inductor with intermediate capacitor,[31,32] and quasi Z source type[33] are used for nonisolated converters. The merits of nonisolated converters such as simple in structure and low cost are preferable in applications where galvanic isolation is not necessary. However, each category of topologies has the following drawbacks such as low voltage gain by the classic boost converters; high current stress of passive switched inductor and switched capacitor topologies; increased component count, and reduced efficiency in voltage multipliers and voltage lift techniques-based converters.

Elegant switched inductor topologies with split duty and reduction in long conducting duty cycles for switches are presented in Lakshmi and Hemamalini.[34] However, the voltage applied across the inductors is reduced in the second switching state of the converter in Lakshmi and Hemamalini,[34] which reduces the voltage gain. To overcome the issue of low voltage gain, a converter in Samiullah et al.[35] is presented, but it contains a high component count. Both the converters in previous studies[34,35] are of floating ground in nature, thus unsuitable for PV fed microgrid applications. The common switch grounding phenomenon is introduced in Pan et al.[36] with high voltage gain at increased component count. Therefore, this paper proposes a topology with split duty ratio and hybrid switched inductor configuration, and the key merits are explained as follows:

1. Split duty control makes the proposed converter superior in terms of avoiding the longer conducting duty ratio that exists in single switch converters.
2. The switch proximate to the power supply will have voltage stress less than the output voltage.
3. Among the three switches, only one switch is operated at input current for a low duty cycle, whereas the remaining two switches are operated at half of the input current.
4. The proposed converter can achieve higher voltage amplification without using any clamping circuits, switched capacitor, and voltage multiplier cell techniques making the converter construction simple and compact.

2 | HSL-CSG TOPOLOGICAL DERIVATION

An active switched inductor with the common switch grounding structure (ASL-CSG) is derived by combining the active switched inductor (ASL) technique[13,34] with the common switch grounding arrangement[36] as shown in Figure 1A. This ASL-CSG network consists of two legs, in leg 1 the inductor L_1 is followed by switch S_1 and in leg 2 inductor L_2 is followed by switch S_2. The inductors are shunted across the source when the switches are turned on. Since one end of the two switches is connected to the ground and hence the name common switch grounding. Further, the passive switched inductor (P-SL) arrangement as depicted in Figure 1B is also integrated in ASL-CSG to develop the proposed hybrid switched inductor-common switch grounding network (HSL-CSG) topology as shown in Figure 2.

The split duty technique is proposed in Lakshmi and Hemamalini,[34] in which during the second switching period (D_2T_S) each inductor is powered by half of the supply voltage which makes the inductor di/dt to fall and store less energy. In the proposed converter with HSL-CSG topological enhancement, each inductor is applied with total input voltage even during the period of D_2T_S. To accomplish this, a third switch is incorporated in the proposed topology across the switch S_2. The parallel switches S_2 and S_3 will share the charging interval of the inductors.

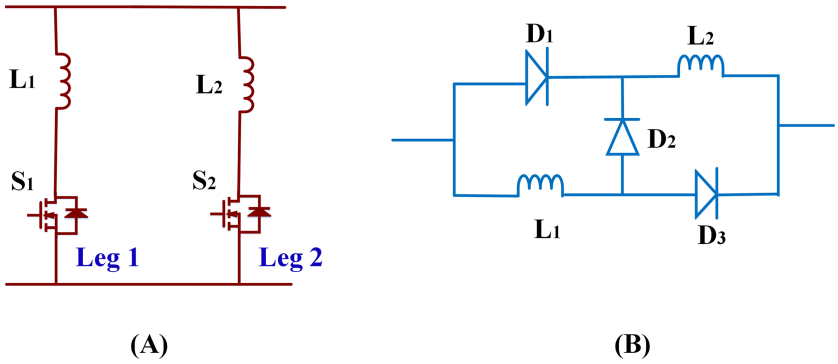

FIGURE 1 (A) ASL-CSG; (B) p-SL

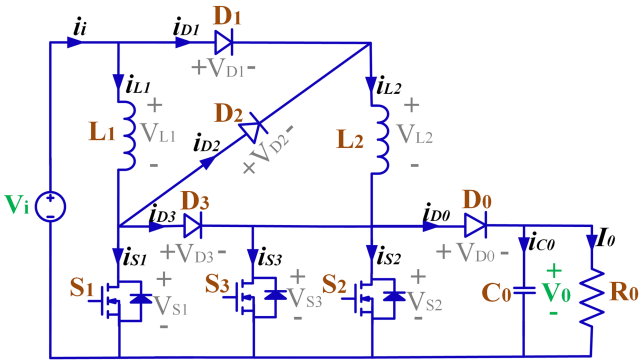

FIGURE 2 Proposed HSL-CSG topology

Since the switches, S_2 and S_3, are in parallel the choice of considering one switch in the place of two would not be feasible because it leads to additional current stress and long conducting interval for the residue switch.

3 | PROPOSED CONVERTER OPERATION AND ANALYSIS

3.1 | Circuit description

The proposed converter contains four diodes (D_0, D_1, D_2, and D_3), three switches (S_1, S_2, and S_3) followed by passive elements of two inductors (L_1 and L_2) and one capacitor (C_0) as shown in Figure 2. The two inductors contain an equal number of turns, and similar core is used; hence, these two are postulated to be identical.

$$L_1 = L_2 = L \tag{1}$$

For the steady-state operation equivalent series resistance (ESR) of all components, forward voltage drop of the diodes and the voltage drop due to ON state resistance of the switches are neglected to make the system ideal.

3.2 | CCM operation and analysis

In CCM, one operating cycle of the HSL-CSG converter there exists three different modes with two duty ratios as shown in Figure 3. The waveforms of various element voltages and currents are as shown in Figure 4A.

Mode I: In this mode (t_0-t_1), switch pair S_1, S_2 of leg 1 and leg 2 are turned ON by magnetizing the inductors L_1, L_2 with a voltage of V_i and intermediate switch S_3 being turned OFF. In this mode, diode D_3 is forward biased, that is,

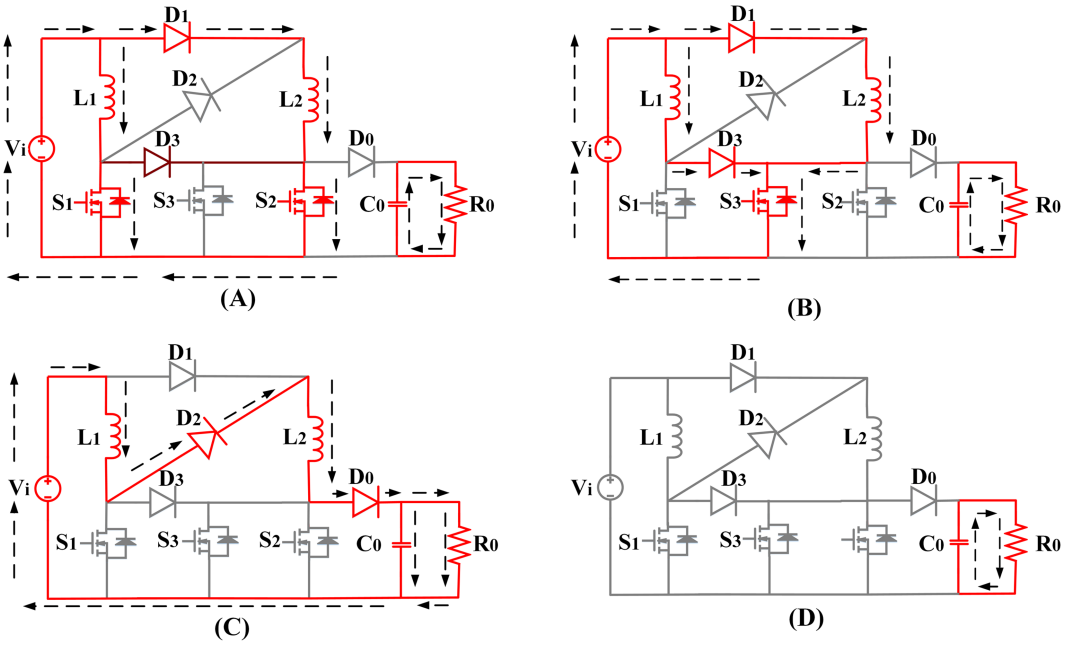

FIGURE 3 CCM and DCM operation (A) S_1, S_2 ON for Mode I; (B) S_3 is ON for Mode II; (C) S_1, S_2, S_3 are OFF for Mode III; (D) equivalent circuit of Mode IV (for DCM only)

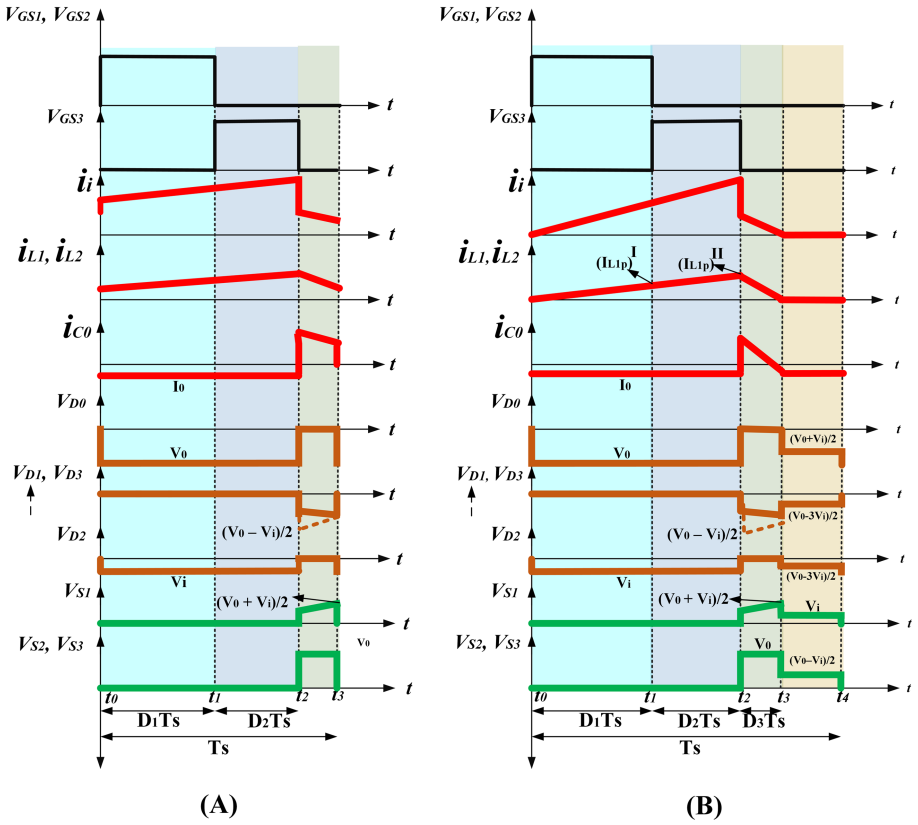

FIGURE 4 HSL-CSG converter typical waveforms in (A) CCM and (B) DCM

floating which makes the voltage across switch S_3 zero. The path for conduction with forward biased diode D_1 along with reverse biased diodes D_0, D_2 is as shown in Figure 3A and the capacitor (C_0) discharges through the load.

The identical voltage and current profile across the two inductors are specified by the following equations.

$$v_{L1} = v_{L2} = V_i \tag{2}$$

$$i_{L1} = i_{L2} = i_L \tag{3}$$

The gradient in inductor currents (5) is derived by using (2) and (3), which is as follows

$$L\frac{di_{L1}}{dt} = L\frac{di_{L2}}{dt} = L\frac{di_L}{dt} = V_i \tag{4}$$

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{di_L}{dt} = \frac{V_i}{L}, \quad t_0 \le t \le t_1 \tag{5}$$

Mode II: During this mode (t_1-t_2), the energization of inductors L_1, L_2 is similar to the previous mode by keeping S_3 at ON and S_1, S_2 are at OFF condition, which makes diode D_3 to conduct. Each inductor consists of total input voltage across it and the capacitor C_0 will power the load as depicted in Figure 3B.

The identical voltage and current profile of the two inductors are specified by the following equations.

$$v_{L1} = v_{L2} = V_i \tag{6}$$

$$i_{L1} = i_{L2} = i_L \tag{7}$$

The gradient in inductor current (8) is obtained using (6) and (7), which is as follows

$$\frac{di_L}{dt} = \frac{V_i}{L}, \quad t_1 \le t \le t_2 \tag{8}$$

Mode III: During this interval of time (t_2-t_3) switch pair S_1, S_2 and intermediate switch S_3 are at OFF condition with diodes D_1, D_3 are reverse biased. The conduction path is as shown in Figure 3C, which contains forward biased diodes D_0 and D_2. In this mode, the source along with two inductors charge the combination of capacitor C_0 and load R_0.

The inductor voltages and currents are as follows

$$v_{L1} = v_{L2} = \frac{V_i - V_0}{2} \tag{9}$$

$$i_{L1} = i_{L2} = i_L \tag{10}$$

Solving (9) and (10) for the rate of change of inductor current, which is as follows

$$\frac{di_L}{dt} = \frac{V_i - V_0}{2L}, \quad t_2 \le t \le t_3 \tag{11}$$

By applying state space averaging method on (5), (8), and (11) the following equation is obtained.

$$\int_0^{D_1 T_S} \left(\frac{di_L}{dt}\right)^{I} dt + \int_0^{D_2 T_S} \left(\frac{di_L}{dt}\right)^{II} dt + \int_0^{(1-D_1-D_2)T_S} \left(\frac{di_L}{dt}\right)^{III} dt = 0 \tag{12}$$

The superscripts denote the corresponding mode of operation. By solving (12), the HSL-CSG converter CCM voltage gain is as follows

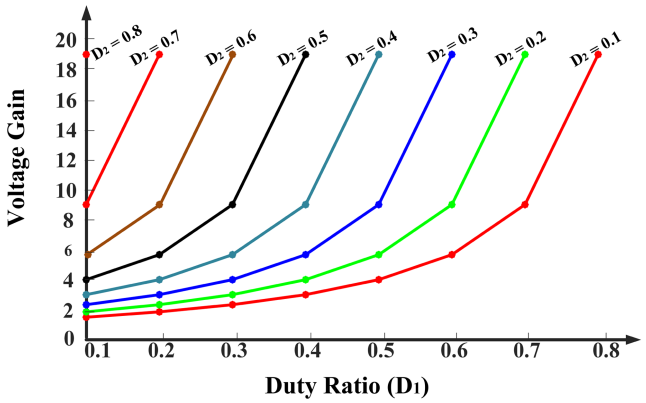

FIGURE 5 Voltage gain (CCM) corresponding to variation in D_1

$$G_{CCM} = \frac{V_0}{V_i} = \frac{1 + D_1 + D_2}{1 - D_1 - D_2} \tag{13}$$

The voltage gain in (13) for fixed duty ratio D_2 is plotted against the duty ratio D_1 as shown in Figure 5 and for the vice-versa case, the plot is identical because voltage gain is symmetrical even if the duty ratios D_1 and D_2 are interchanged in (13). It is evident from the plot that if the duty ratio D_1 or D_2 is increased then gain will also increase in proportion with a factor specified in (13).

3.3 | Inductor and capacitor selection

The selection of inductors ($L_1 = L_2 = L$) and output capacitor C_0[37] depends on the factors like input voltage (V_i), duty ratio (D_1), inductor ripple current (Δi_L), switching frequency (f_s); load wattage (P_0), rated voltage (V_0) and voltage ripple of capacitor (ΔV_c). The critical values of inductors (L_{1c}, L_{2c}) and capacitor (C_{0c}) for CCM operation are as follows

$$L_{1c} = L_{2c} = \frac{V_i D_1}{\Delta i_L f_s} \tag{14}$$

$$C_{0c} = \frac{P_0}{V_0 \Delta V_c f_s} \tag{15}$$

3.4 | DCM operation and analysis

The DCM analysis for each operating cycle has four modes. Some of the typical waveforms under this mode of operation are as shown in Figure 4B.

Mode I: This mode is analogous to Mode I of HSL-CSG converter CCM operation where switches of leg 1, leg 2 are at ON condition and Figure 3A is also equally valid. The inductor peak currents are written as

$$\left(I_{L1p}\right)^I = \left(I_{L2p}\right)^I = \frac{V_i}{L} D_1 T_S \tag{16}$$

Mode II: This mode is analogous to Mode II of CCM operation where the switches S_1, S_2 are at OFF condition and S_3 is at ON condition as shown in Figure 3B. The inductor peak currents are as follows

$$\left(I_{L1p}\right)^{II} = \left(I_{L2p}\right)^{II} = \frac{V_i}{L}\left(D_1 + D_2\right)T_S \tag{17}$$

Mode III: In this Mode III, leg 1 and leg 2 switch pair along with intermediate switch are at OFF condition like in the case of CCM operation as shown in Figure 3C. The peak currents of the inductors L_1 and L_2 are as follows.

$$\left(I_{L1p}\right)^{III} = \left(I_{L2p}\right)^{III} = \frac{V_0 - V_i}{2L} D_3 T_S \tag{18}$$

Mode IV: In this mode also, all switches remain to be turned OFF and inductors energy is zero, that is, they are completely discharged. Thus, only capacitor C_0 powers the load R_0 as shown in Figure 3D.

From Figure 4B, the peak currents of two inductors L_1 and L_2 at (the end of) Mode II and (the beginning of) Mode III are equal. Hence, equating (17) and (18)

$$\left(I_{L1p}\right)^{II} = \left(I_{L1p}\right)^{III} \tag{19}$$

$$\frac{V_i}{L}\left(D_1 + D_2\right)T_S = \frac{V_0 - V_i}{2L} D_3 T_S \tag{20}$$

Solving the (20) gives duty ratio D_3, which is as follows

$$D_3 = \frac{2V_i(D_1 + D_2)}{V_0 - V_i} \tag{21}$$

The average current of the capacitor C_0 is given by

$$I_{C0} = \frac{1/2\left(D_3\, T_S\right)\left(I_{L1p}\right)^{II}}{T_S} - I_0 \tag{22}$$

Since the steady state capacitor current is equal to zero, rewriting the above expression of I_{C0}

$$\frac{1/2\left(D_3\, T_S\right)\left(I_{L1p}\right)^{II}}{T_S} = \frac{V_0}{R_0} \tag{23}$$

Substituting (17) and (21) in (23) and solving for DCM voltage gain

$$G_{DCM} = \frac{V_0}{V_i} = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{\left(D_1 + D_2\right)^2}{\tau_L}} \tag{24}$$

Where normalized inductor time constant is defined as

$$\tau_L = \frac{Lf_s}{R_0} \tag{25}$$

The DCM voltage gain and duty ratio D_1 plot corresponding to fixed duty ratio D_2 for an inductor time constant (τ_L) of 0.02 is shown in Figure 6A, and the graph will be identical even D_1 and D_2 are interchanged in (24).

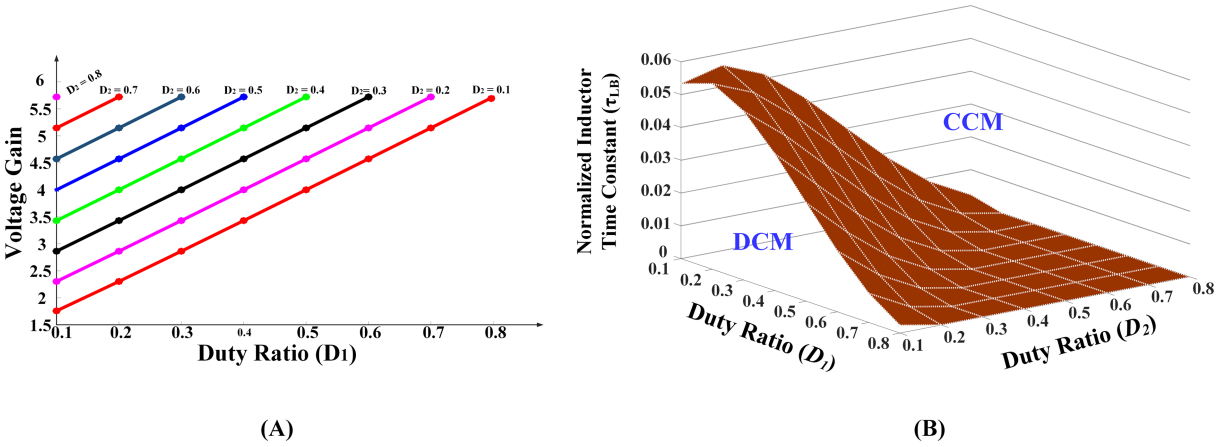

FIGURE 6 Gain and time constant plots in DCM. (A) Voltage gain (DCM) versus variation in D_1; (B) boundary inductor time constant versus duty ratio D_1 and D_2

3.5 | Boundary operating condition of CCM and DCM

The boundary of CCM and DCM will have equal voltage gains, hence equating (13) and (24) inductor time constant at the boundary can be obtained as

$$\tau_{LB} = \frac{(D_1 + D_2)\,(1 - (D_1 + D_2))^2}{2(1 + D_1 + D_2)} \tag{26}$$

The following conditions in (27) and (28) are necessary for the HSL-CSG converter to operate in CCM and DCM.

$$\tau_{LB} < \tau \rightarrow \quad \frac{(D_1 + D_2)\,(1 - (D_1 + D_2))^2}{2(1 + D_1 + D_2)} < \frac{Lf_s}{R_0} \tag{27}$$

$$\tau_{LB} > \tau \rightarrow \quad \frac{(D_1 + D_2)\,(1 - (D_1 + D_2))^2}{2(1 + D_1 + D_2)} > \frac{Lf_s}{R_0} \tag{28}$$

The variation of boundary inductor time constant with respect to duty ratios is as shown in Figure 6B.

3.6 | Efficiency analysis

The majority portion of performance indices of any power converter depends on parasitics of the elements in the power circuit. Hence, topological visualization of these parasitic parameters is shown in Figure 7, where r_{L1}, r_{L2}, r_{C0} are the ESR of the passive elements L_1, L_2 and C_0. The ESR and forward voltage drops of the diodes are r_{D0}, r_{D1}, r_{D2}, r_{D3} and V_{D0}, V_{D1}, V_{D2}, V_{D3}, respectively.

Similarly, r_{S1}, r_{S2}, r_{S3} represents the conduction resistance (drain to source) of S_1, S_2, and S_3, respectively. Further, the capacitor current analysis is carried out by neglecting the ESR voltage drop because it is very small and also to make the calculations simple.

Mode I: In this mode, switch pair S1, S2 are operated as shown in Figure 8, Mode I. The forward voltage drop V_{D1} of diode D_1 is neglected on the basis that the percentage deviation caused by V_{D1} in the inductor current i_{L2} (from i_{L1}) is 0.76%, 4% concerning inductor current I_{L1} and ripple current ΔI_{L1}, respectively. This assumption makes the two inductor currents identical in this mode of operation.

The capacitor current and inductor voltages are as follows

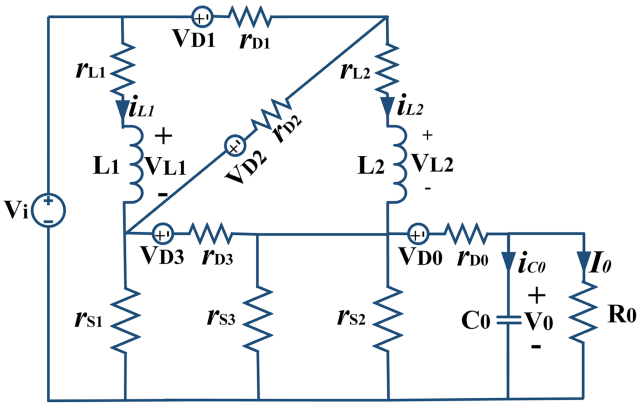

FIGURE 7 Equivalent circuit with parasitic parameters

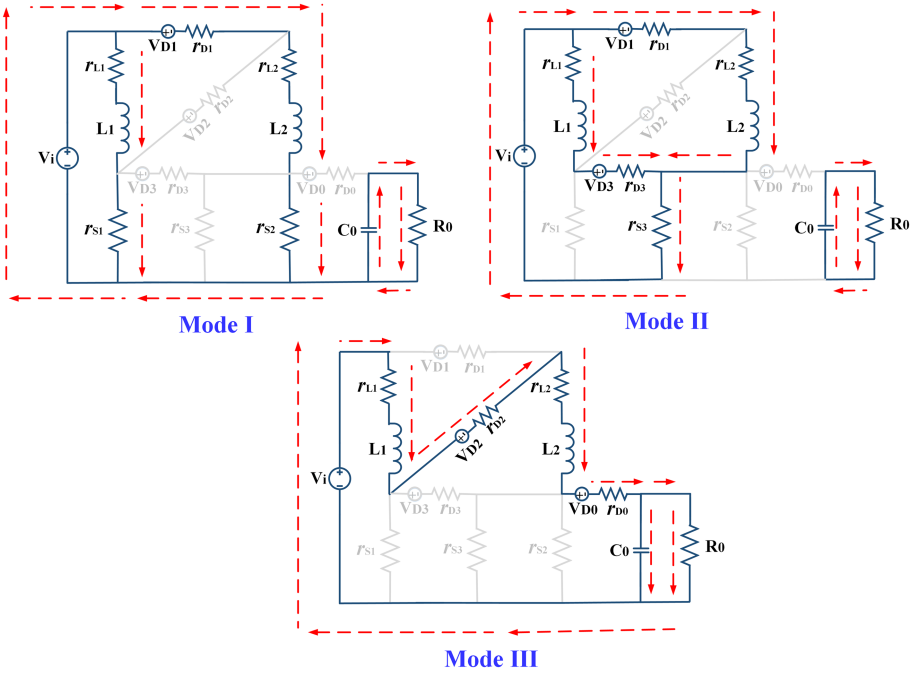

FIGURE 8 Modes of operation with parasitic parameters

$$(I_{C0})^{I} = -\frac{V_0}{R_0} \tag{29}$$

$$(V_{L1})^{I} = V_i - i_{L1}(r_{L1} + r_{S1}) \tag{30}$$

Mode II: In this mode, intermediate switch is operated as shown in Figure 8, Mode II. The capacitor current and inductor voltages are given by the following equation.

$$(I_{C0})^{II} = -\frac{V_0}{R_0} \tag{31}$$

$$(V_{L1})^{II} = V_i - i_{L1}(r_{L1} + r_{D3} + 2r_{S3}) - V_{D3} \tag{32}$$

Mode III: In this mode S1, S2 and S3 are at OFF condition as shown in Figure 8, Mode I. The capacitor current and inductor voltages are specified as follows

$$(I_{C0})^{III} = I_{L1} - \frac{V_0}{R_0} \tag{33}$$

$$(V_{L1})^{III} = \frac{V_i - i_{L1}(r_{L1} + r_{L2} + r_{D2} + r_{D0} + r_{C0}) - (V_{D2} + V_{D0}) - V_0}{2} \tag{34}$$

Applying the amp-sec balance for the capacitor C_0

$$\int_0^{D_1 T_S} (I_{C0})^I \, dt + \int_0^{D_2 T_S} (I_{C0})^{II} \, dt + \int_0^{(1-D_1-D_2)T_S} (I_{C0})^{III} \, dt = 0 \tag{35}$$

Substituting (29), (31), and (33) in (35) and solving for I_{L1}

$$I_{L1} = \frac{V_0}{R_0(1 - D_1 - D_2)} \tag{36}$$

Similarly applying volt-sec balance to inductor L_1

$$\int_0^{D_1 T_S} (V_{L1})^I \, dt + \int_0^{D_2 T_S} (V_{L1})^{II} \, dt + \int_0^{(1-D_1-D_2)T_S} (V_{L1})^{III} \, dt = 0 \tag{37}$$

Substituting (30), (32), and (34) in (37) and solving for V_0

$$V_0 = \frac{\mathrm{V_i}(1 + \mathrm{D_1} + \mathrm{D_2}) - (2\mathrm{V_{D3}})\mathrm{D_2} - (\mathrm{V_{D2}} + \mathrm{V_{D0}})(1 - \mathrm{D_1} - \mathrm{D_2})}{(1 - \mathrm{D_1} - \mathrm{D_2}) + 2\left(\frac{\mathrm{AD_1} + \mathrm{BD_2} + \mathrm{C}(1 - \mathrm{D_1} - \mathrm{D_2})}{\mathrm{R_0}(1 - \mathrm{D_1} - \mathrm{D_2})}\right)} \tag{38}$$

where

$$\begin{cases} \mathrm{A} = (\mathrm{r_{L1}} + \mathrm{r_{S1}}) \\ \mathrm{B} = (\mathrm{r_{L1}} + \mathrm{r_{D3}} + 2\mathrm{r_{S3}}) \\ \mathrm{C} = (\mathrm{r_{L1}} + \mathrm{r_{L2}} + \mathrm{r_{D2}} + \mathrm{r_{D0}} + \mathrm{r_{C0}}) \end{cases}$$

The proposed HSL-CSG converter input and output powers are acquired as follows

$$P_i = 2\,V_i\,I_{L1}(D_1 + D_2) + V_i\,I_{L1}\,(1 - D_1 - D_2) \tag{39}$$

Using (36) in (39) the input power is written as

$$P_i = \frac{V_i V_0}{R_0}\left(\frac{1 + D_1 + D_2}{1 - D_1 - D_2}\right) \tag{40}$$

The HSL-CSG converter output power is written as

$$P_0 = \frac{{V_0}^2}{R_0} \tag{41}$$

From (38), (40), and (41), the efficiency of proposed converter is written as

$$\eta = \frac{\left(1-(D_1+D_2)^2\right) - \left(\frac{(2V_{D3})(1-D_1-D_2)+(V_{D2}+V_{D0})(1-D_1-D_2)^2}{V_i}\right)}{(1+D_1+D_2)\left\{(1-D_1-D_2)+2\left(\frac{AD_1+BD_2+C(1-D_1-D_2)}{R_0(1-D_1-D_2)}\right)\right\}} \tag{42}$$

The switching losses must be deducted from (41) to account for this portion of losses in efficiency calculations.

3.7 | Voltage and current stress analysis

The switches and diodes peak current stresses in the HSC-CSG topology are as follows

$$I_{D1p} = \frac{I_i}{2}(2-D_1-D_2) + \frac{V_i}{2Lf_s}(D_2) \tag{43}$$

$$I_{D2p} = \frac{I_i}{2}(2-D_1-D_2) + \frac{V_0-V_i}{4Lf_s}(1-D_1-D_2) \tag{44}$$

$$I_{D3p} = \frac{I_i}{2}(2-D_1-D_2) + \frac{V_i}{2Lf_s}(D_2) \tag{45}$$

$$I_{D0p} = \frac{I_i}{2}(2-D_1-D_2) + \frac{V_0-V_i}{4Lf_s}(1-D_1-D_2) \tag{46}$$

$$I_{S1p} = \frac{I_i}{2}(2-D_1-D_2) + \frac{V_i}{2Lf_s}(D_1) \tag{47}$$

$$I_{S2p} = \frac{I_i}{2}(2-D_1-D_2) + \frac{V_i}{2Lf_s}(D_1) \tag{48}$$

$$I_{S3p} = 2\left(\frac{I_i}{2}(2-D_1-D_2) + \frac{V_i}{2Lf_s}(D_2)\right) \tag{49}$$

4 | PERFORMANCE COMPARISON

The comparative analysis of proposed converter with existing high gain converters in terms of stepup gain, element count, device voltage stress, that is, normalized voltage stress of diodes, switches, total voltage standing, peak current stress on switches, possibility of split duty, common grounding between source and load is provided in Table 1. The split duty converters[34,35,38] in comparison with the single duty converters will reduce the long conducting duty cycles for the switches. As depicted in Figure 9, for the duty ratio $D_1 = 0.6$ and $D_2 = 0.35$ the theoretical voltage gain attained by HSL-CSG converter is 39, whereas the gain of the converters in previous studies[34,38] are 32 and 33, respectively. These voltage gains are far superior to those of the converters in previous studies[13,15,19] which provide a voltage gain of 4 and 3.5 for the same operating conditions stated above and among the previous studies[31–33]; only Mahmood et al.[33] is in par interms of the voltage gain for the aforementioned conditions.

TABLE 1 Comparison of nonisolated and split duty converters

Topology	Voltage gain (G)	Voltage gain per component (G/C)at D = 0.85 or D = 0.43[b]	Normalized diode voltage stress (V_D/Vo)	Normalized switch voltage stress (V_S/Vo)	Normalized Total voltage standing	Peak switch current stress $\left(\widehat{I_S}/I_o\right)$	Common ground
[13]◊	$\left(\frac{1+D}{1-D}\right)$	2.5	$\frac{1}{2}+\frac{1}{2G}$	$1+\frac{1}{G}$	$\frac{3+3G}{2G}$	$\frac{1+D}{2(1-D)}$	No
[15]Δ	$\left(\frac{1+D}{1-D}\right)$	1.5	2	1	3	$\frac{1+D}{1-D}$	Yes
[19]□	$\left(\frac{2-D}{1-D}\right)$	0.8	$1-\frac{1}{G}$	$1-\frac{1}{G}$	$2-\frac{2}{G}$	$\frac{2-D}{D(1-D)}$	No
[31]	$\left(\frac{5+D}{1-D}\right)$	2.8	$\frac{1+G}{2G}$	$\frac{1+G}{G}$	$\frac{3+3G}{2G}$	$\frac{3+D}{D(1-D)}$	No
[32]	$\left(\frac{3+D}{1-D}\right)$	1.8	$\frac{1+2G}{G}$	$\frac{1+G}{G}$	$\frac{2+3G}{G}$	$\frac{1+D}{D(1-D)}$	No
[33]	$\left(\frac{3-3D-2D^2}{(1-D)(1-2D)}\right)$	1.2[b]	$\frac{8D-1}{3-3D-2D^2}$ $D=\frac{(3G-3)-\sqrt{(3G-3)^2-(4(2G+2)(G-3))}}{2(G+2)}$	$\frac{2-3D}{3-3D-2D^2}$	$\frac{3+5D}{3-3D-2D^2}$	$\frac{1+2D}{D(1-2D)}$	No
Split duty converters							
[34]	$\left(\frac{1+D_1}{1-D_1-D_2}\right)$	1.3	$1+\frac{2}{G}$	$2+\frac{1}{G}$	$3+\frac{3}{G}$	$\frac{1}{1-D_1-D_2}$	No
[38][a]	$\left(\frac{2-D_2}{1-D_1-D_2}\right)$	1.1	$\frac{3}{2}+\frac{1}{G}$	$2-\frac{1}{G}$	$\frac{7}{2}$	$\frac{1}{1-D_1-D_2}$	Yes
HSL-CSG[a]	$\left(\frac{1+D_1+D_2}{1-D_1-D_2}\right)$	1.2	$\frac{5}{2}+\frac{1}{2G}$	2	$\frac{9}{2}+\frac{1}{2G}$	$\frac{(1+D_1+D_2)(2-D_1-D_2)}{1-D_1-D_2}$	Yes

◊ = converter 1, Δ = Figure 9, □ = sepic derived (switch and load side diode only), G = voltage gain, C_S = switch count, C_D = diode count, C_L = inductor count, C_C = capacitor count.
[a]Magnitude of device voltage stress is only considered.
[b]The value 1.2 belong to the case of D=0.43 and rest all belong to D=0.85.

TABLE 1 (Continued)

Topology	Constant input current	Split duty	Long conducting duty ratio	% η at 100 W	Element count			
					C_S	C_D	C_L	C_C
[13]◊	No	No	Yes	92%	2	1	2	1
[15]Δ	Yes	No	Yes	88%	1	4	2	1
[19]□	Yes	No	Yes	86%	1	3	2	4
[31]	No	No	Yes	94.8%	2	5	4	3
[32]	No	No	Yes	96.7%	2	5	4	3
[33]	No	No	Yes	94%	2	4	3	5
Split duty converters								
[34]	No	Yes	No	93.6%	3	2	2	1
[38][a]	No	Yes	No	91%	3	4	2	1
HSL-CSG[a]	No	Yes	No	93.2%	3	4	2	1

◊ = converter 1, Δ = Figure 9, □ = sepic derived (switch and load side diode only), G = voltage gain, C_S = switch count, C_D = diode count, C_L = inductor count, C_C = capacitor count.
[a]Magnitude of device voltage stress is only considered.
[b]The value 1.2 belong to the case of D=0.43 and rest all belong to D=0.85.

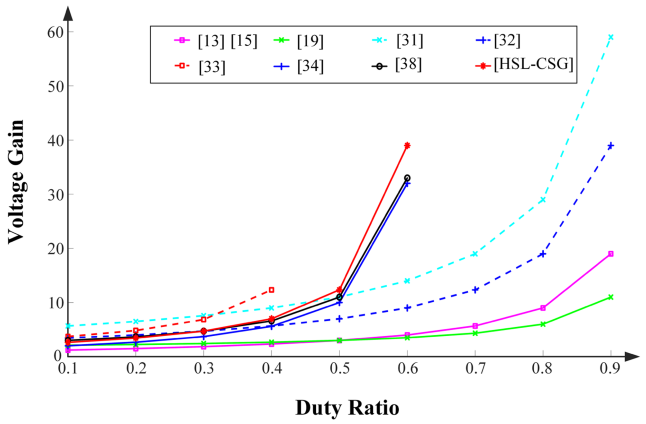

FIGURE 9 Voltage gain comparison

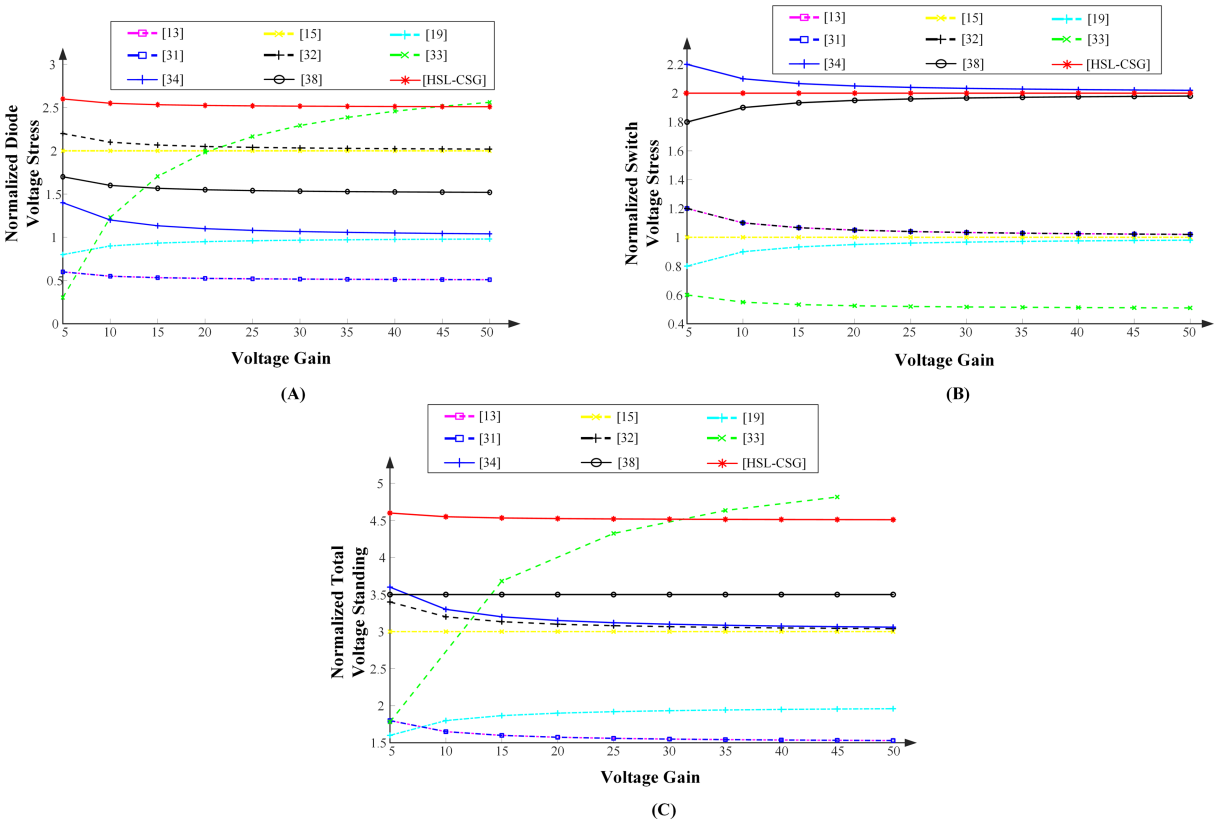

FIGURE 10 Normalized voltage stress versus voltage gain of (A) diodes (B) switches (C) total voltage standing

The normalized voltage stress across various elements of different converters in comparison with the proposed converter are presented in Table 1 and as shown in Figure 10A–C. The normalized voltage stress on diodes of HSL-CSG is similar to the converters in previous studies[34,38] and this is higher comparing to the other converters because of no intermediate capacitors in the proposed converter as shown in Figure 10A. The switch voltage stress and total voltage standing as shown in Figure 10B, C, it is similar to above mentioned switch voltage profile. The proposed converter switch count is the same as that of the converters in previous studies.[34,38] The inductor and capacitor counts are equal to the converters in previous studies[13,15,34] and this count is less than the converters in previous studies.[19,31–33] The switches S_2, S_3 will have high voltage stress and this is permissible because of the facts that split in overall duty and

high voltage gain provided by the HSL-CSG converter. The voltage gain per device count and the efficiency are also moderate for the HSL-CSG converter comparing with the other converters.

The intermediate switch S_3 will have the highest current stress compared to all elements because it has to carry the entire input current for a time period of D_2T_s as shown in Figure 11. The current stress profile of the HSL-CSG converter is better than the converters in previous studies.[31–33]

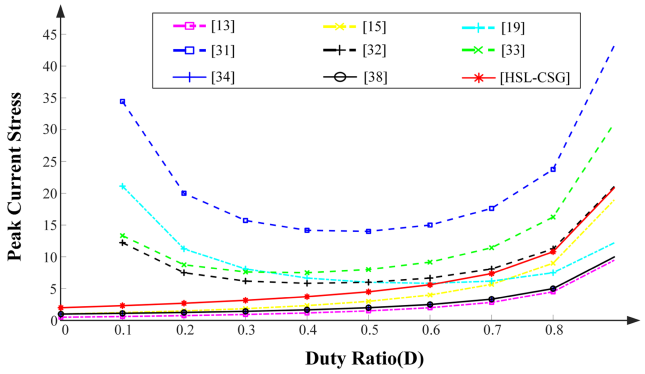

FIGURE 11 Peak current stress versus duty ratio of switches

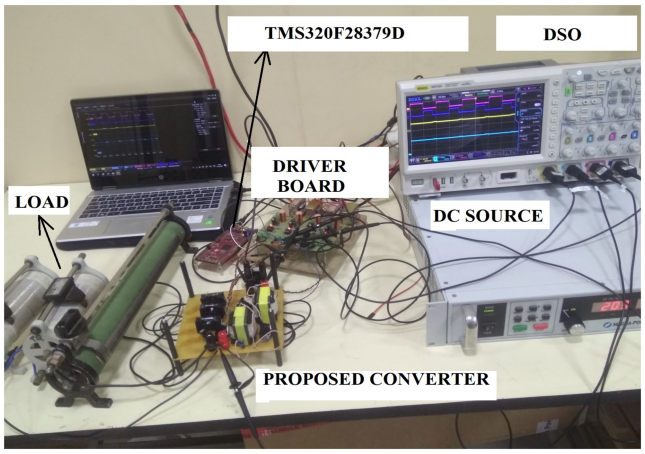

FIGURE 12 Experimental setup

TABLE 2 Prototype specifications

Rated power (P_0)	≅150 W
Input voltage (V_i)	20 V
Duty ratio (D_1)	50%
Duty ratio (D_2)	35%
Switching frequency (f_s)	50 kHz
Inductors (L_1, L_2)	400 μH
Capacitor (C_0)	10 μF
Mosfet (S_1, S_2 and S_3)	STW28N65M2
Diode (D_0)	STPSC10H065

5 | EXPERIMENTAL RESULTS

The proposed converter theoretical analysis has been validated with a prototype as shown in Figure 12 and its specifications are provided in Table 2. The gate pulses V_{GS1}, V_{GS2} are of 50% duty ratio and identical to each other as shown in Figure 13. The gate pulse V_{GS3} is of 35% duty ratio and 180° phase shift with respect toV_{GS1}.

A voltage gain of 11.75 is attained for an input voltage of 20 V. The HSL-CSG converter draws an average input current (i_i) of 7.4 A to deliver a load current (i_0) of 590 mA as shown in Figure 13B. Since the converter operates in CCM the inductor currents i_{L1} and i_{L2} are continuous as shown in Figure 13C. The instantaneous capacitor current i_{C0} is

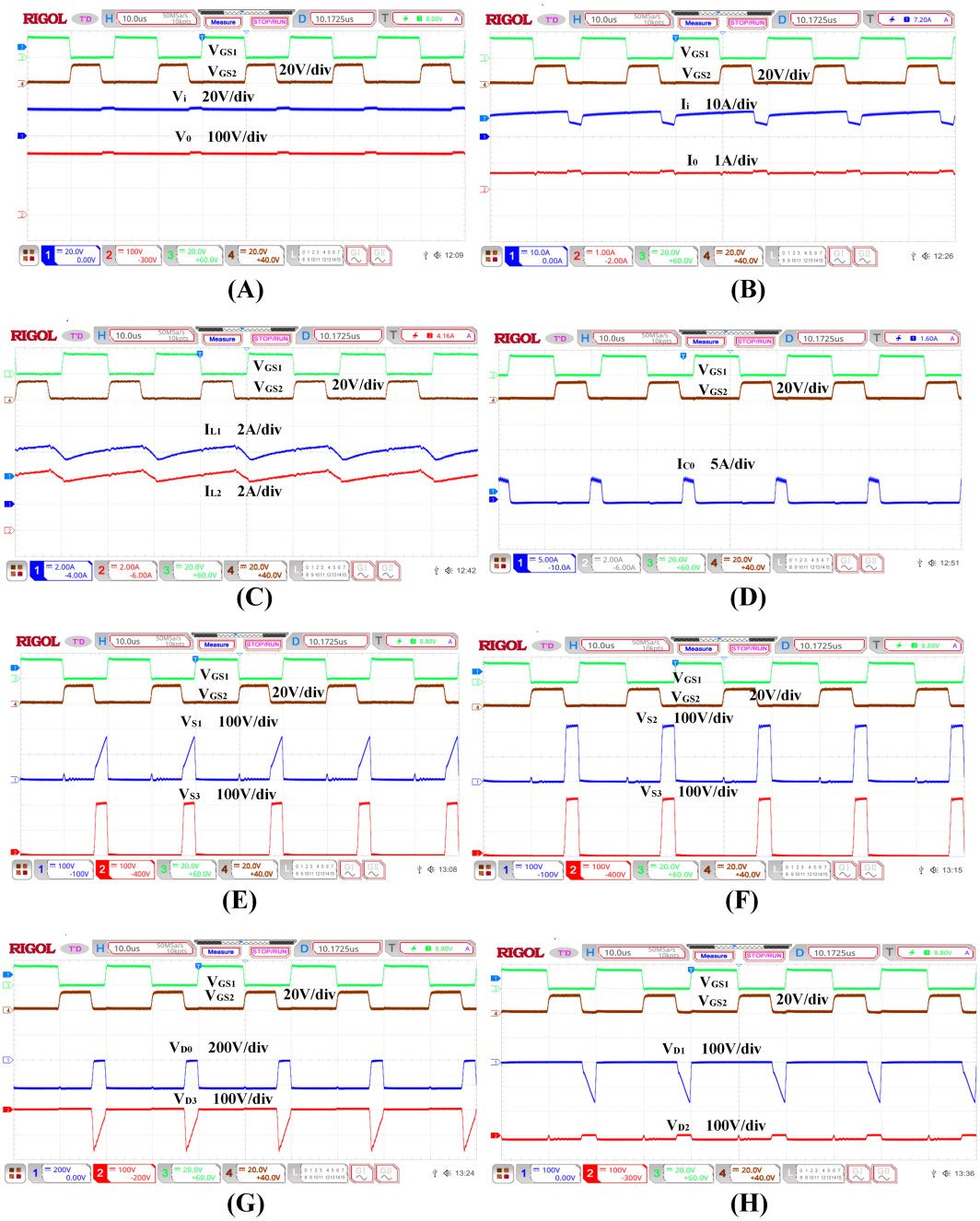

FIGURE 13 Experimental results. (A) Input and output voltages (V_i and V_0); (B) input and output currents ($i_i$and i_0); (C) inductor currents ($i_{L1}$and i_{L2}); (D) capacitor current (i_{C0}); (E) switch voltages ($V_{S1}$and V_{S3}); (F) switch voltages ($V_{S2}$and V_{S3}); (G) diode voltages ($V_{D0}$and V_{D3}); (H) diode voltages ($V_{D1}$and V_{D2})

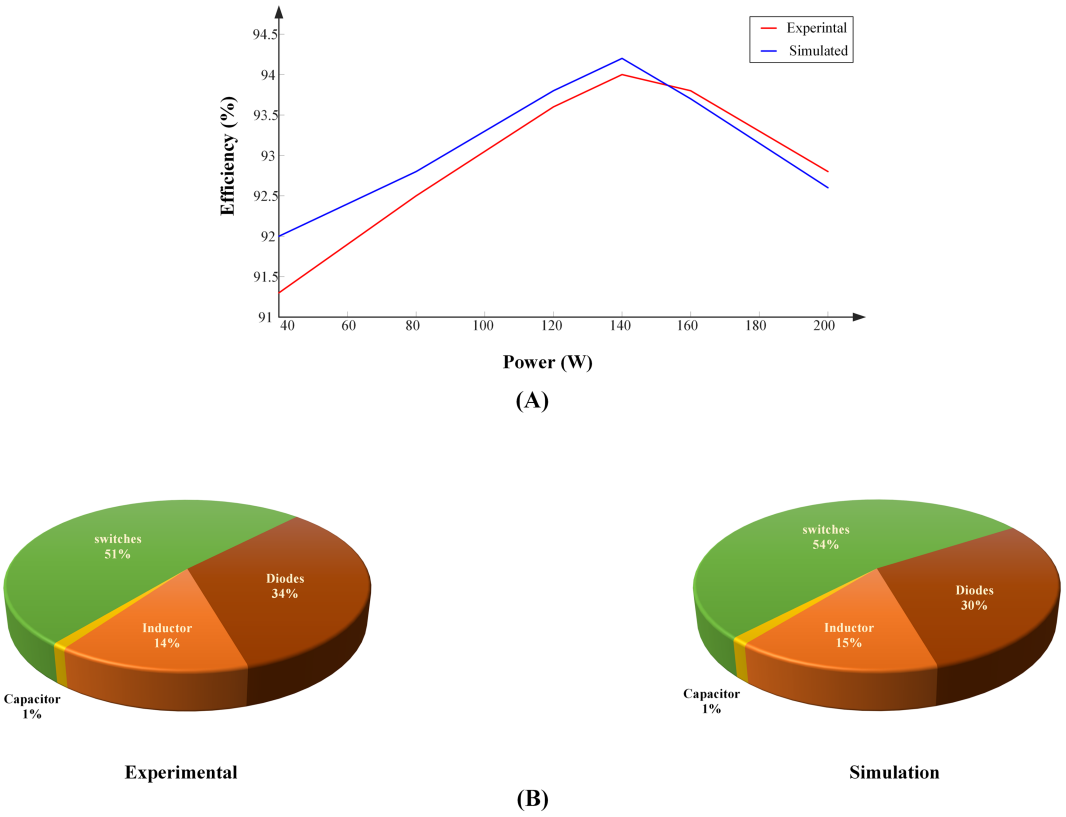

FIGURE 14 (A) Efficiency corresponding to output powers. (B) Power loss distribution

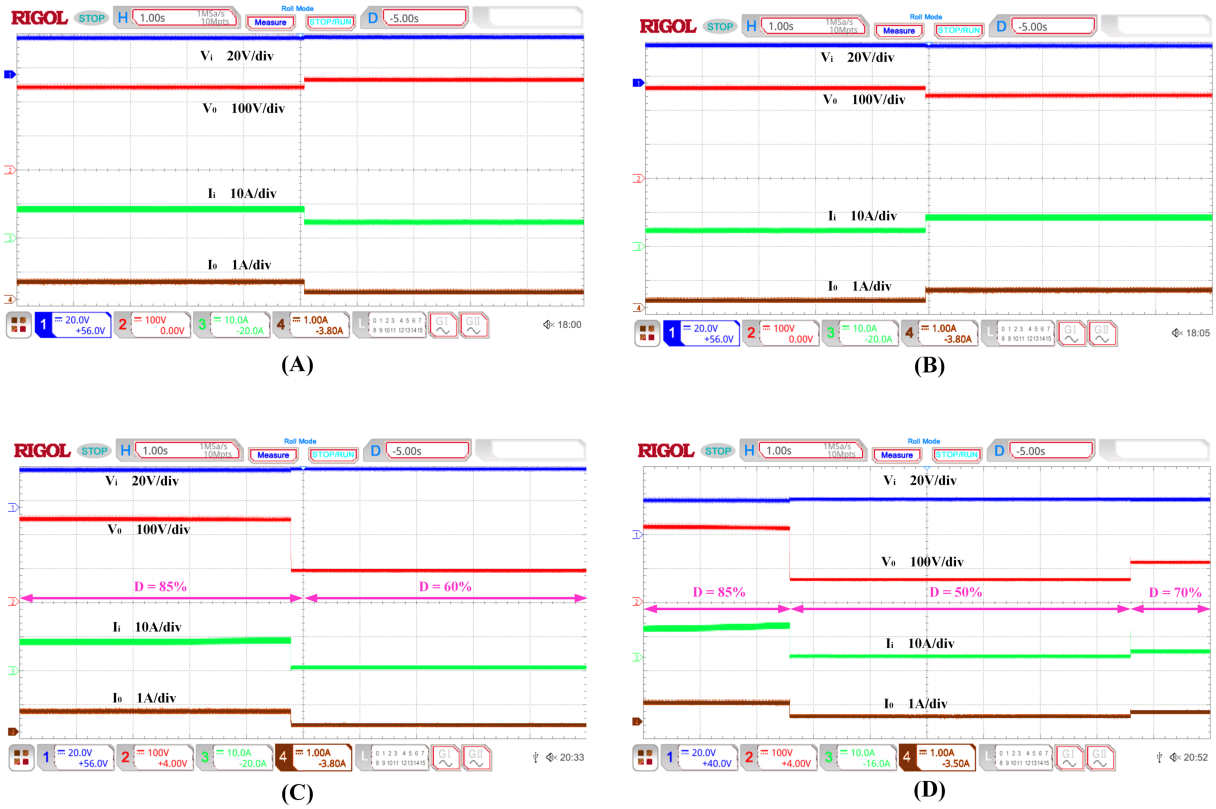

FIGURE 15 Dynamic variation of HSL-CSG converter in terms of (A) load increase; (B) load decrease; (C) two step variation in duty ratio; (D) three step variation in duty ratio

shown in Figure 13D. The blocking voltage of switch S_1 is equal to an average of V_i, V_0 and that of S_2 and S_3 is V_0 as shown in Figure 13E and F. From Figure 13G, H it is evident that the diodes D_0 and D_2 are at a voltage stress of V_0 and V_i, respectively. The diodes D_1 and D_3 will have equal voltage stress of half of the difference of V_i and V_0.

The proposed converter is operating with an experimental efficiency of 93.7% at rated power condition. From Figure 14A it is evident that the proposed converter efficiency is well above 91% for different load conditions. The proposed HSL-CSG converter distribution of power loss is shown in Figure 14B, where the switches are having the highest loss proportion of 51% and next diodes with a loss proportion of 34%. In other words, among total power loss 85% is contributed by only switches and diodes.

The feasibility of HSL-CSG converter for dynamic changes in the load and duty ratio is experimentally validated as shown in Figure 15A–D. The load variations are considered from half load to full load and vice versa. The variation in the duty ratio is considered in two cases as shown in Figure 15C, D, where in the first schematic the duty variation is from 85% to 60% and that of in the second three step variation of duty ratio is 85%:50%:70% considered.

6 | CONCLUSION

This paper presented a high gain nonisolated DC-DC converter namely HSL-CSG by integrating switched inductor and spit duty ratio flexibility. The converter operates with a split duty ratio to reduce the long conducting time intervals of the switches thus, make them less prone to failure. High stepup voltage gain was accomplished without transformers, voltage multipliers cells and numerous voltage lifting techniques. The proposed converter experimental validation was done with a prototype to verify voltage gain, efficiency, voltage stresses; the feasibility of the converter for dynamic variations in terms of load and duty ratio is also validated. A comparative analysis had been presented by considering existing similar switched inductor-capacitor topologies and other ultra-voltage gain converters including the converter based on quasi z source paradigm. The converter operated well above 91% efficiency for all load conditions and for full load an efficiency of 93.7% was attained. Finally, the proposed converter provides high voltage gain of 11.75 with HSL and split duty ratio flexibility.

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DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

ORCID

M. F. Baba https://orcid.org/0000-0003-4026-7175
B. L. Narasimharaju https://orcid.org/0000-0002-3033-5712

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