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RESEARCH ARTICLE

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A new buck-boost integrated multilevel inverter with reduced capacitors and capacitor size for low-frequency AC applications

Madhu Babu Sambhani[1] | **Narasimharaju B.L.**[1] | **Akshay Kumar Rathore**[2]

[1]Department of Electrical Engineering, National Institute of Technology Warangal, Telangana, India

[2]Department of Electrical and Computer Engineering, Concordia University, Montreal, Canada

Correspondence
Madhu Babu Sambhani, Department of Electrical Engineering, National Institute of Technology Warangal, Telangana, 506004, India.
Email: sam1729@student.nitw.ac.in

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Summary

This paper proposes a new buck-boost integrated multilevel inverter with reduced capacitors and capacitor size. The proposed multilevel inverter consists of a 5-level basic unit formed by two interleaved buck-boost converters, whose outputs are cascaded with the source to achieve a voltage gain of five. The capacitors present in the buck-boost converters are charged at the high switching frequency; therefore, the proposed multilevel inverter utilizes small capacitors compared to the existing switched capacitor multilevel inverter (SCMLI) topologies. Moreover, capacitors presented in the conventional SCMLI are limited to fixed voltage charging, whereas the capacitors of the proposed inverter can be charged to desired voltages by adjusting respective buck-boost converter duty cycles. Hence, the proposed inverter requires a relatively less number of compact capacitors to produce the higher number of voltage levels. In this paper, the design and operation of the proposed 11-level inverter are presented. A 500 W proof-of-concept is developed and the experimental results are presented for linear and nonlinear loads under static and dynamic load conditions. In addition, a comprehensive comparative study of the proposed inverter and the recent SCMLIs is presented.

KEYWORDS

buck-boost integrated, multilevel inverter, step-up inverter, switched capacitor

1 | INTRODUCTION

Recently, multilevel inverter (MLI) topologies became popular in various applications such as photovoltaic (PV) energy conversion, electric vehicles (EV), and power quality improvement, etc., over the conventional two-level inverters. The

List of Symbols and Abbreviations: $C_{1,min}$ & $C_{2,min}$, critical inductance of C_1 & C_2; car1 & car2, carrier signals; d_1 & d_2, duty cycles of buck BBCs 1 & 2; E_{dc}, E_{C1} & E_{C2}, energies processed by source, BBCs 1& 2; E_{Total}, total energy delivered to the load; f_s, switching frequency of BBCs; i_1, i_{L1} and i_{L2}, instantaneous currents of source and inductors L_1 & L_2; i_{lg}, leakage current; k_1 and k_2, percentage voltage ripples of C_1 & C_2; $L_{1,cri}$ & L_{2cri}, critical inductance of L_1 & L_2; P_{C1} & P_{C2}, powers handled by BBCs 1 & 2; $P_{o,max}$ & $P_{dc,max}$, peak output power and peak source power; $\%P_{C1,max}$ & $\%P_{C2,max}$, percentage of peak power shared by each BBC; $\%P_{dc,max}$, percentage of peak power shared by the source; v_{ar} & v_{br}, pole voltages of the MLI; v_{C1} & v_{C2}, instantaneous voltages of capacitor C_1 & C_2; V_{dc}, source voltage; v_o & i_o, instantaneous voltage and currents the MLI output; v_R & i_R, instantaneous voltage and currents the rectifier output; $V_{o,max}$, peak of the load voltage; x_1 & x_2, boost factor of BBC 1 & 2; BBC, buck-boost converters; CHB, cascaded H bridge; *CMV*, common mode voltage; EV, electric vehicles; MLI, multilevel inverter; PEC, packed E-cell; PUC, packed U-cell; PWM, pulse width modulation; PV, photovoltaic; SCMLI, switched capacitor multilevel inverter; *T*, time period of voltage waveform; THD, total harmonic distortion.

cascaded H bridge (CHB) MLIs require more number of isolated sources and switching components. To reduce the device count, various symmetrical and asymmetrical MLIs[1-4] are presented. However, the MLIs[1-4] are unable to provide voltage gain which is essential in PV and EV applications. In recent times, switched capacitor MLI (SCMLI) topologies are widely used due to their simple operation and voltage gain features.[5,6] Cascaded SCMLI topologies[7] for high frequency applications are presented to increase the number of levels with multiple DC sources and increased components. SCMLIs with asymmetrical DC sources[8-10] are presented to provide more levels with reduced device count, but require multiple isolated asymmetrical DC sources. The inverters with high voltage gain are attached to the PV panel which are also called as AC module are useful to extract maximum power and achieve modular operation. Cost effective packed U-cell (PUC) structures[11,12] are presented for grid-connected PV applications. However, the majority of the PUC based MLIs can produce a maximum of 7-level output voltage only with voltage gain lesser than 1.5. A nine-level packed E-cell (PEC) MLI[13] is presented however, it only provides voltage gain of one. The SCMLIs[14-21] with a single DC source and high voltage gain are useful in solar and EV applications; however, require more number of bulky capacitors and switches to produce more number of levels.

The SCMLI topologies[7,8,10,14-20] use parallel charging and series discharging technique in order to increase the gain and number of levels. The basic unit of conventional SC cell is depicted in Figure 1A and the respective model waveforms are depicted in Figure 2A. From Figure 2A, it can be observed that during level-2, the capacitor voltage is decreasing with respect to time. The ripple voltage depends on the load resistance and level-2 duration. Hence, the conventional SCMLI with less load resistance needs bulky capacitors to limit the ripple voltage. Further, it can be observed that the capacitor drawing an impulse charging current at beginning of the level-1, therefore conventional SC cell requires devices with the high current rating.

To limit the impulse charging currents, quasi-resonant SCMLIs[22-24] use a bulky inductor in the charging path of the capacitor as shown in Figure 1B and the respective model waveforms are shown in Figure 2B. From the figure, it can be noticed that the capacitor charging current magnitude is reduced and hence, device with low current rating can be utilized. The quasi-resonant SC cell also uses parallel charging and series discharging technique similar to the convention SC cell. Hence, it also having capacitor voltage drooping issue and requires bulky capacitors to limit the ripple voltage. The SCMLI[22] is unable to provide voltage gain and the SCMLIs[23,24] are able to step-up the voltage with increased use of bulky capacitors and switches.

To address these issues, buck-boost integrated SC cell is developed as shown in Figure 1C and the respective model waveforms are shown in Figure 2C. Unlike the conventional and quasi-resonant SC cells, the buck-boost integrated SC cell charges the capacitor at high switching frequency while it delivering the load, hence the capacitor voltage can be regulated to the desired value and avoids the drooping issue. The buck-boost inductor will take care of the charging current. The high frequency operation of buck-boost integrated SC-cell reduces the size of both inductor and capacitor compared to the conventional and quasi-resonant SC cells. The adjustable voltage gain of the buck-boost integrated SC-cell will help to produce more number of levels with reduced number of devices.

As the bulky electrolytic capacitors are more prone to failure, the reduced capacitor size, and capacitor count[25,26] improves the reliability of the inverter. The SCMLI[25] provides a voltage gain of 3 and uses two isolated symmetrical sources.

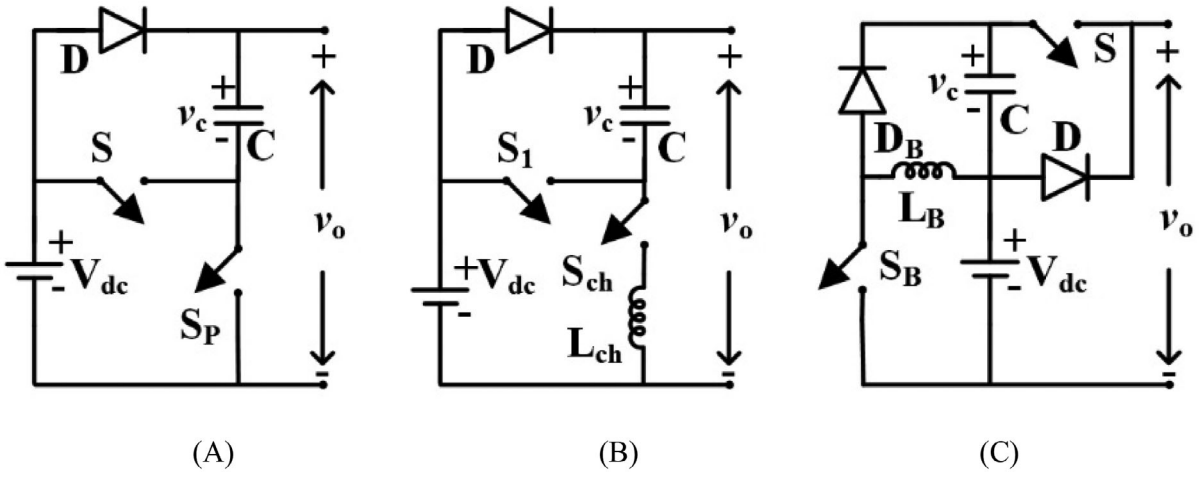

FIGURE 1 Basic units of (A) parallel charge SCMLI[14-21] (B) quasi-resonant SCMLI[22-24] (C) proposed buck-boost integrated SCMLI[25]

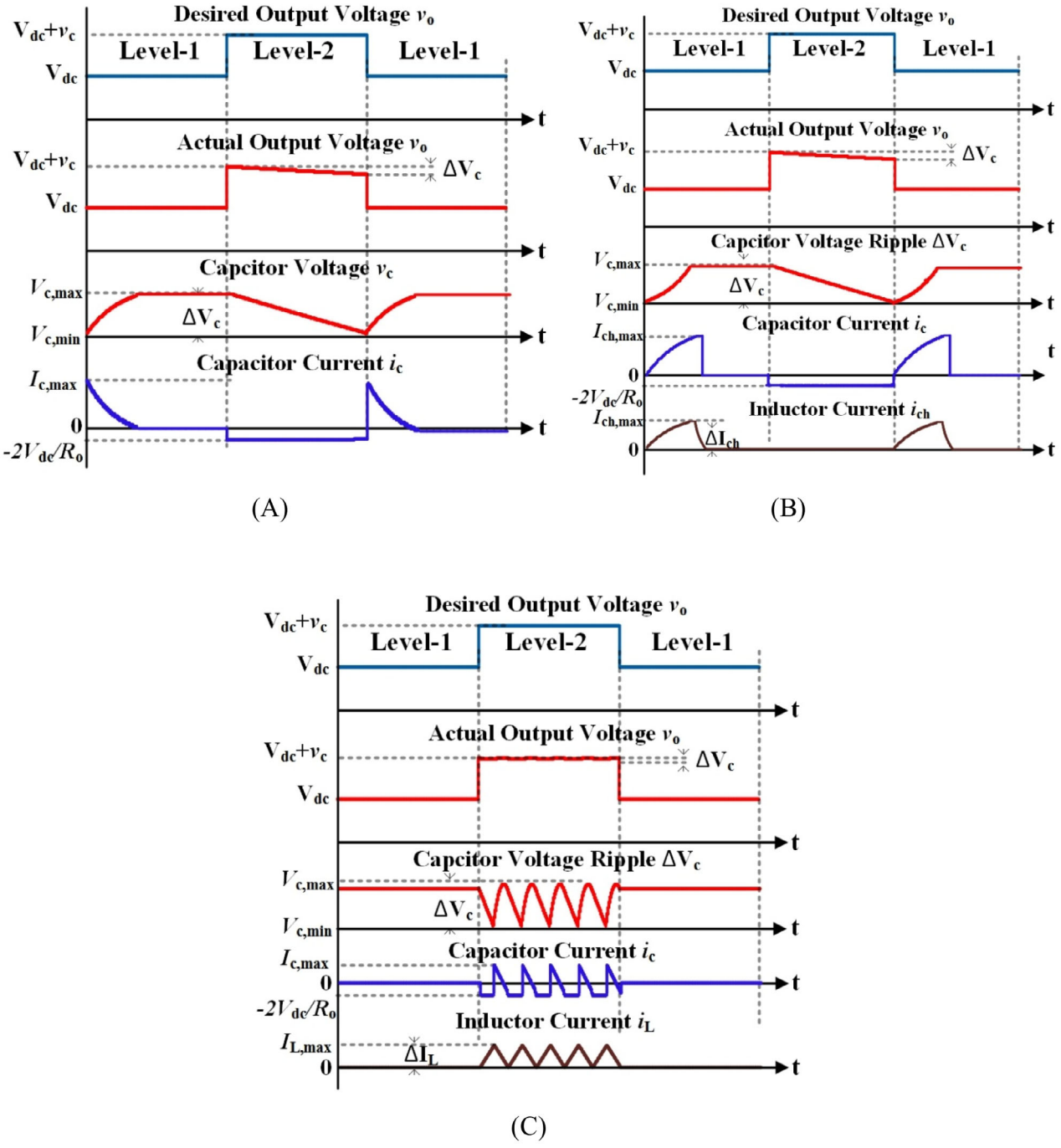

FIGURE 2 Model waveforms of (A) parallel charge SCMLI (B) quasi-resonant SCMLI (C) buck-boost integrated SCMLI

To address these issues, this paper proposes a new buck-boost integrated multilevel inverter with single DC source for low-frequency AC applications that offers various merits such as voltage gain of 5, reduced component count, capacitors' size, and charging current as well.

2 | PROPOSED MULTILEVEL INVERTER

The proposed multilevel inverter (MLI) is depicted in the Figure 3. It consists of a basic unit and H-bridge inverter. Further, the basic unit contains a buck-boost network and a level selector network. The buck-boost network employs two buck-boost converters which are energized from the input voltage source. The output voltages of buck-boost converters

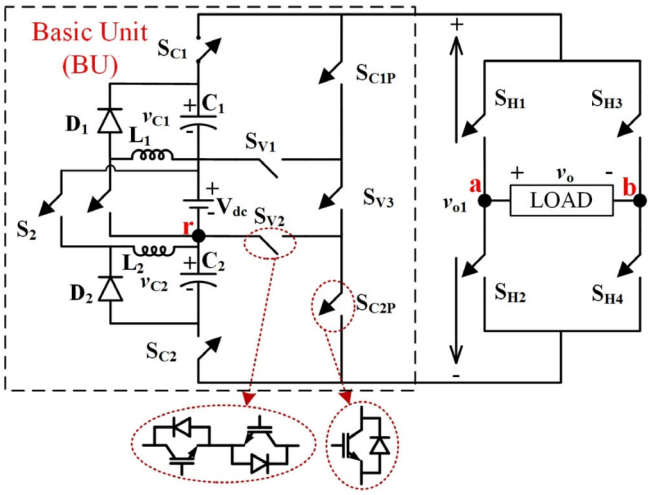

FIGURE 3 Proposed buck-boost integrated multilevel inverter

(ie, capacitor C_1 and C_2 voltages) are connected in series with the source to provide voltage gain and two more voltage levels. Each buck-boost converter (BBC) comprises of a switch, diode, inductor, and capacitor. The capacitor C_1 and C_2 voltages v_{C1} and v_{C2} are x_1 and x_2 times of the source voltage V_{dc} respectively. Boost factors x_1 and x_2 of the buck-boost converters either 1 and 3 or 3 and 1 to produce maximum number of five levels using a basic unit. The level selector network is formed by the switches S_{C1}, S_{C1P}, S_{C2}, S_{C2P}, S_{V1}, S_{V2}, S_{V3} to select the required combination of voltages of buck-boost network. Table 1 describes the corresponding switching states of the level selector network and buck-boost converters state of operation for different output voltage levels of basic unit.

The proposed basic units can be cascaded to generate more number of levels and the H-bridge inverter unfolds the waveform. With one basic unit, the proposed inverter produces a 11-level output voltage waveform. The capacitor voltage ratios are taken as $x_1 = 1$ and $x_2 = 3$, that means $v_{C1} = V_{\text{dc}}$ and $v_{C2} = 3V_{\text{dc}}$. The duty cycles d_1 and d_2 of buck-boost converters are expressed as.

$$d_1 = \frac{x_1}{1+x_1} \tag{1}$$

$$d_2 = \frac{x_2}{1+x_2} \tag{2}$$

Operation of a buck-boost converter depends upon the output level as specified in the Table 1. The nearest level controller as shown in Figure 4 is utilized to realize switching levels of the proposed inverter. Equivalent circuits of the basic unit for different levels of operation are presented in Figure 5, whereas the buck-boost converters are represented by their output voltages.

3 | CONTROL OF THE PROPOSED MULTILEVEL INVERTER AND ITS COMPARISON STUDY WITH THE EXISTING MULTILEVEL INVERTERS

3.1 | Design of inductors and capacitors

The highest level of the proposed multilevel inverter is considered for the design of inductor and capacitors of the buck-boost converters. The equivalent circuit is illustrated in Figure 6 with a resistive load R_o. The respective peak load current $I_{o,\max}$ can be expressed as

$$I_{o,\max} = \frac{V_{\text{dc}} + v_{C1} + v_{C2}}{R_o} = \frac{V_{o,\max}}{R_o} \tag{3}$$

where $V_{o,\max}$ is the peak of the load voltage, which is the sum of the voltages V_{dc}, v_{C1} and v_{C2} .

TABLE 1 Switching States of the basic unit

	Boost converter		
On state devices	**BBC-1**	**BBC-2**	v_{0X}
S_{C1P}, S_{V1}, S_{V2}, S_{C2P}	OFF	OFF	0
S_{C1}, S_{V1}, S_{V3}, S_{C2P}			V_1
S_{C1}, S_{V1}, S_{V3}, S_{C2P}	ON	OFF	$v_{C1} = V_1$
S_{C1}, S_{V2}, S_{C2P}	ON	OFF	$V_1 + v_{C1} = 2\ V_1$
S_{C1P}, S_{V3}, S_{V2}, S_{C2}	OFF	ON	$v_{C2} = 3\ V_1$
S_{C1P}, S_{V1}, S_{C2}	OFF	ON	$V_1 + v_{C2} = 4\ V_1$
S_{C1}, S_{C2}	ON	ON	$V_1 + v_{C1} + v_{C2} = 5\ V_1$

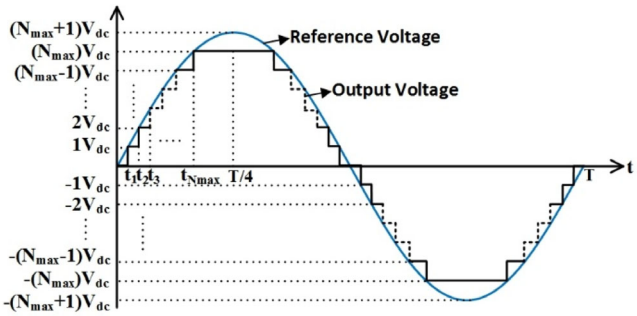

FIGURE 4 Model waveform of the MLIs with nearest level control

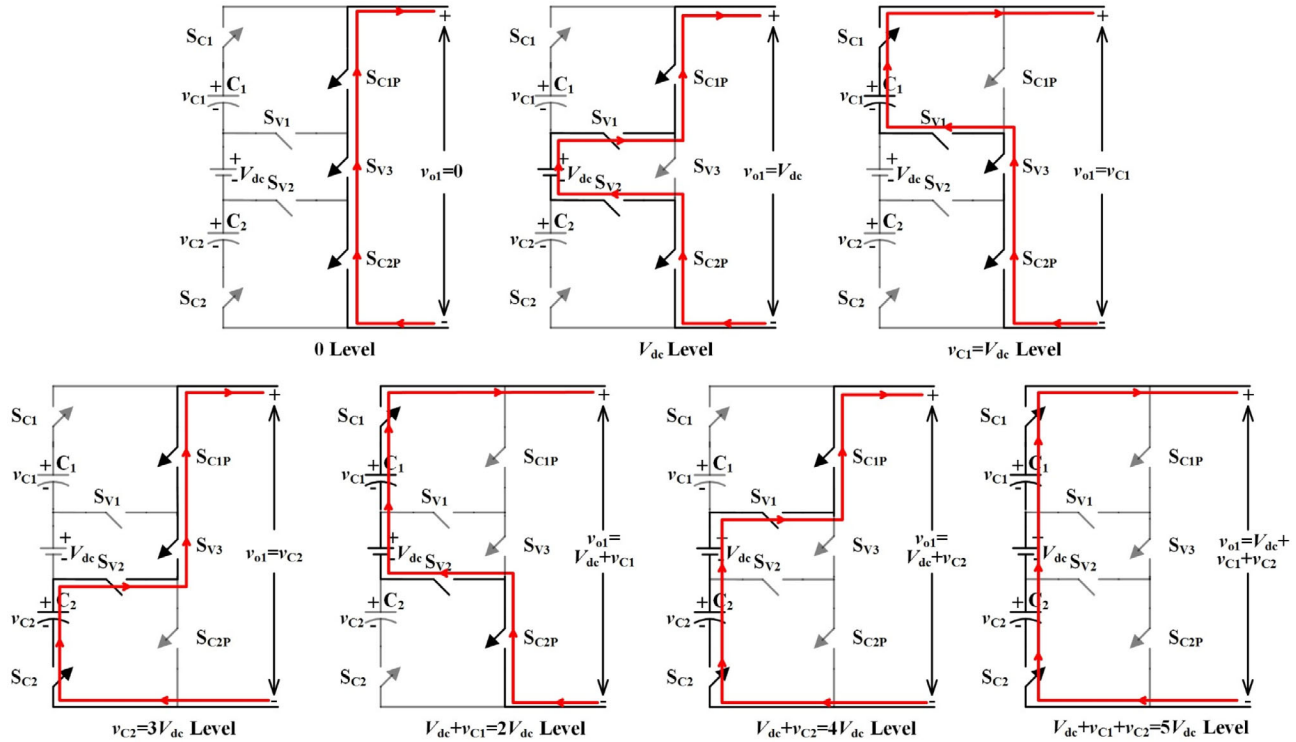

FIGURE 5 Modes of operation of the proposed basic unit

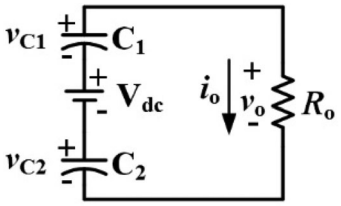

FIGURE 6 Equivalent circuit of the proposed inverter for the peak output voltage level

The powers P_{C1} and P_{C2} handled by the capacitors of the buck boost converters are given as follows

$$P_{C1} = V_{C1} I_{o,\max} \tag{4}$$

$$P_{C2} = V_{C2} I_{o,\max} \tag{5}$$

Equivalent resistance seen by each buck boost converter is

$$R_{C1} = \frac{v_{C1}^2}{P_{C1}} = \frac{v_{C1} R_0}{V_{o,\max}} \tag{6}$$

$$R_{C2} = \frac{v_{C2}^2}{P_{C2}} = \frac{v_{C2} R_0}{V_{o,\max}} \tag{7}$$

By assuming the boundary conduction mode, the critical inductances $L_{1,cri}$ and $L_{2,cri}$ of respective L_1 and L_2 are obtained by equating the energy stored in the respective inductor during ON period and equivalent energy transferred by the buck-boost converter, which are expressed as

$$L_{1,cri} = \frac{d_1^2 R_0}{2x_1(1+x_1+x_2)f_s} \tag{8}$$

$$L_{2,cri} = \frac{d_2^2 R_0}{2x_2(1+x_1+x_2)f_s} \tag{9}$$

where f_s = switching frequency of buck boost converters.

The minimum capacitance values $C_{1,\min}$ and $C_{2,\min}$ of C_1 and C_2 required to maintain respective percentage capacitor voltage ripples k_1 and k_2 of buck-boost converter-1 and 2 are given by

$$C_{1,\min} = \frac{(1+x_1+x_2)d_1 * 100}{k_1 x_1 R_0 f_s} \tag{10}$$

$$C_{2,\min} = \frac{(1+x_1+x_2)d_2 * 100}{k_2 x_2 R_0 f_s} \tag{11}$$

With the help of (8) and (9), the critical inductances $L_{1,cri}$ and $L_{2,cri}$ required for different load resistance at different switching frequencies can be obtained as illustrated in Figure 7A. Similarly, (10) and (11) are utilized for calculation of minimum capacitances $C_{1,\min}$ and $C_{2,\min}$ required to maintain 5% capacitor ripple voltage as depicted in Figure 7B.

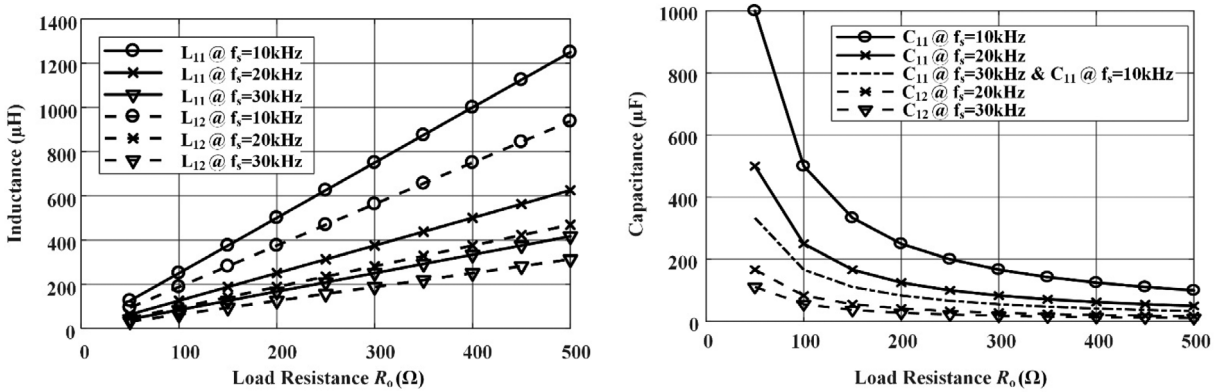

FIGURE 7 Design characteristics of (A) critical inductances $L_{1,cri}$ and $L_{2,cri}$ (B) minimum capacitances $C_{1,min}$ and $C_{2,min}$ for 5% ripple voltage with respect load current at different switching frequencies

3.2 | Control of buck boost converters

To maintain desired capacitor voltages of buck-boost converters with dynamic load conditions, two voltage control loops with PI controller are employed for each converter as shown in the Figure 8. In the figure, *car*1 and *car*2 are the carrier signals with frequency equals to the f_s, which are used for the PWM generation of BBC-1 and BBC-2 respectively. The generated pulses from the two control loops are fed to buck-boost converter switches S_1 and S_2, respectively. These pulses are realized by the interleaved pulse width modulation to reduce input ripple current.

3.3 | Power handling ratio of buck-boost converters

In the proposed multilevel inverter, considerable amount of power is processed by the buck-boost converters and the remaining is delivered from the voltage source. The maximum power handling ratio of each buck-boost converter can be obtained from the peak power instant of the inverter. The peak output power $P_{o,\max}$ and respective source power $P_{\mathrm{dc,max}}$ can be expressed as

$$P_{\mathrm{o,max}} = V_{o,\max} I_{o,\max} \tag{12}$$

$$P_{\mathrm{dc,max}} = V_{\mathrm{dc}} I_{o,\max} \tag{13}$$

By using (4), (5), (12), and (13) the percentage of peak power shared by each buck-boost converter ($\%P_{C1,\max}$ & $\%P_{C2,\max}$) and source ($\%P_{\mathrm{dc,max}}$) are calculated as follows

$$\%P_{C1,\max} = \frac{v_{C1} I_{o,\max}}{V_{o,\max} I_{o,\max}} \times 100 = 20\% \tag{14}$$

$$\%P_{C2,\max} = \frac{v_{C2} I_{o,\max}}{V_{o,\max} I_{o,\max}} \times 100 = 60\% \tag{15}$$

$$\%P_{dc,max} = \frac{V_{\mathrm{dc}} I_{o,\max}}{V_{o,\max} I_{o,\max}} \times 100 = 20\% \tag{16}$$

From the above equations, it is confirmed that the both buck-boost converters together are only rated for 80% out of total rated power. The instantaneous powers of source (P_{dc}) and buck-boost converters (P_{C1} and P_{C2}) shared at different voltage levels are shown in Figure 9.

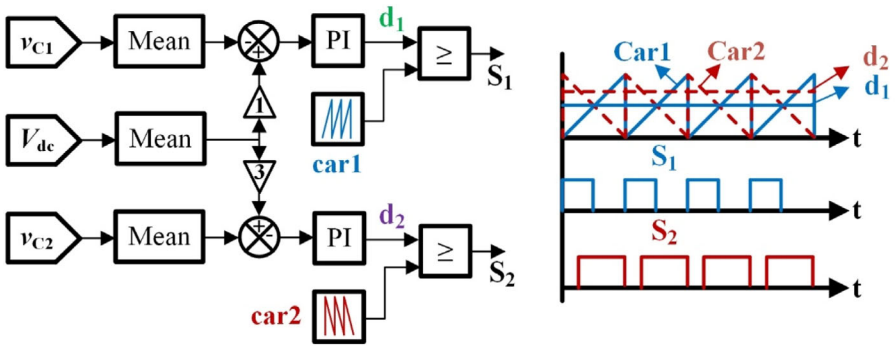

FIGURE 8 Block diagram of closed loop control and pulse generation of BBCs

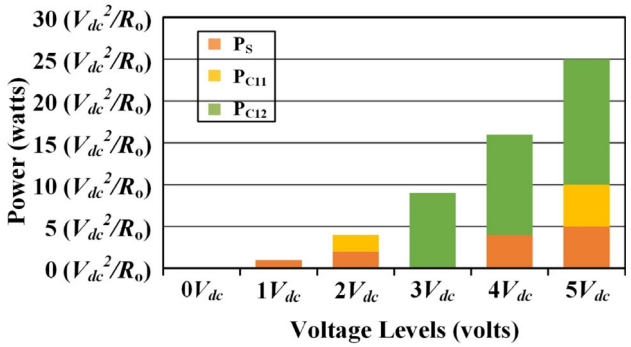

FIGURE 9 Power shared by DC source and buck boost converters at different operating voltage levels

Assume T is the total time period of voltage waveform; E_{Total} is the total energy delivered to the load during the $T/4$ period; E_{dc}, E_{C1}, and E_{C2} are the energies processed by source and buck-boost converters respectively in $T/4$ duration. The energies E_{Total}, E_{dc}, E_{C1}, and E_{C2} can be obtained as follows

$$E_{\text{Total}} = \sum_{i=0}^{5} (t_{i+1} - t_i) * (i * V_{\text{dc}})^2 / R_o \tag{17}$$

$$E_{\text{dc}} = \sum_{i=1,2,4,5} (t_{i+1} - t_i) * \left(i * V_{\text{dc}}^2\right) / R_o \tag{18}$$

$$E_{C1} = \sum_{i=2,5} (t_{i+1} - t_i) * \left(i * V_{\text{dc}}^2\right) / R_o \tag{19}$$

$$E_{C2} = \sum_{i=3}^{5} (t_{i+1} - t_i) * \left(3i * V_{\text{dc}}^2\right) / R_o \tag{20}$$

where i is a positive integer from 0 to 5, t_i and t_{i+1} are the starting and ending instants of the i^{th} level. By using (17), (18), (19), and (20), the utilization ratios of source, buck-boost converters 1 and 2 are calculated as 20.873%, 15.3215%, and 63.8055% respectively.

3.4 | Comparison

To verify the advantages of the proposed inverter in contrast with the recent 11-level SCMLI topologies, a comparative study is carried out and the data are presented in Tables 2 and 3. Various parameters like number of switches, diodes,

TABLE 2 Comparative study of the proposed inverter with the recent 11-level SCMLIs

Parameter	22 (2017)	15 (2018)	18 (2019)	27 (2019)	19 (2020)	20 (2020)	23 (2021)	Proposed
No.of sources	1	1	1	1	1	1	1	1
No.of switches	12	24	13	13	12	12	20	15
No.of diodes	5	4	4	0	0	2	8	2
No.of capacitors	5	4	4	4	4	4	8	2
Capacitor Size	Bulky	Bulky	Bulky	Bulky	Bulky	Bulky	Bulky	Small
No.of inductors	1	0	0	0	0	0	1	2
No.of drivers	12	24	13	13	12	12	20	15
Gain	1	5	5	5	2.5	5	5	5
Inrush current	No	Yes	Yes	Yes	Yes	Yes	No	No
Efficiency (%)	93.5	88.9	—	—	93.0	92.1	96.0	93.0
No. of levels	11	11	11	11	11	11	11	11

TABLE 3 Comparative study of the proposed inverter and the recent SCMLIs in generalized operation

Parameter	15	18	20	22	23	Proposed
No. of levels	$2n + 1$	$2n + 3$	$10n + 1$	$2n + 1$	$2n + 3$	$10n + 1$
No.of sources	1	1	n	1	1	n
No.of switches	5n-1	$2n + 5$	12n	$2n + 2$	$4n + 4$	15n
No.of diodes	0	n	2n	n	2n	2n
No.of capacitors	$n - 1$	n	4n	n	2n	2n
Capacitor size	Bulky	Bulky	Bulky	Bulky	Bulky	Small
No.of inductors	0	0	0	1	1	2n
No.of drivers	$5n - 1$	$2n + 5$	12n	$2n + 2$	$4n + 4$	13n
Inrush current	Yes	Yes	Yes	No	No	No
Gain	$n + 1$	$n + 1$	5	1	$n + 1$	5

sources, inductors, capacitors, capacitors' size, voltage gain, inrush current during capacitor charging, and efficiency of the proposed inverter and the recent SCMLIs for 11-level operation are compared. The proposed MLI requires less number of small capacitors vis-á-vis MLIs,[15,18-20,22,23,27] hence improves the reliability of the inverter. Although the SCMLIs[19,22] require less number of switches, they provide the voltage gains of 2.5 and 1 respectively, whereas the proposed MLI provides a voltage gain of 5. However, SCMLI[18] utilizes less number of switches and provides voltage gain of 5, it uses higher number of diodes and bulky capacitors. The SCMLIs[15,23] use a higher number of devices and bulky capacitors as compared to the proposed MLI. During the charging period of the capacitors, the SCMLIs[15,18-20,27] draw impulsive current, hence require high current rated switches. Whereas, the buck-boost inductor in the proposed MLI limit the inductor capacitor charging current. Except the proposed MLI, all other SCMLIs presented in Table 2 use parallel charge and series discharge of capacitors, thus suffer from capacitor voltage droop problem at high power ratings. Whereas, the capacitor voltages of the proposed inverter are controlled by the closed-loop controllers, hence free from voltage drooping issues.

3.4.1 | Inrush current during capacitor charging

Basic unit of parallel charge SCMLIs[15,18-20,27] is presented in Figure 1A and its equivalent circuit during capacitor charging is depicted in Figure 10A. R_C is the equivalent series resistance (ESR) of the capacitor C and $R_{SP,ON}$ is the equivalent on state resistance of the switch S_P. The peak value $I_{C,\text{peak}}$ of capacitor current i_C can be expressed as follows

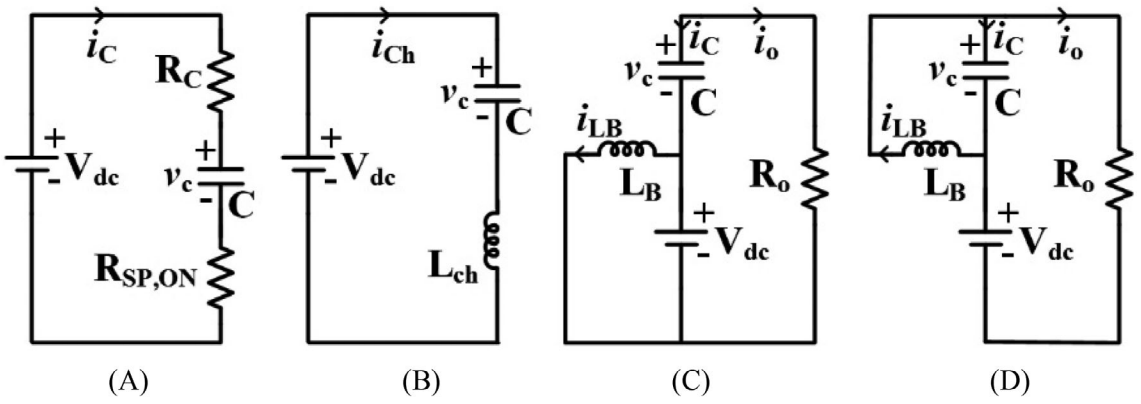

FIGURE 10 Equivalent circuits of basic units during charging of the (A) capacitor in parallel charge SCMLI (B) capacitor in quasi-resonant SCMLI (C) inductor in buck-boost integrated SCMLI (D) capacitor in buck-boost integrated SCMLI

$$I_{C,\text{peak}} = \frac{V_{dc} - v_C}{R_C + R_{\text{SP,ON}}} \tag{21}$$

Usually, the R_C and $R_{\text{SP,ON}}$ are small and hence the peak of the charging current will be high.

Basic unit of quasi-resonant SCMLIs[22,23] is presented in Figure 1B and its equivalent circuit during capacitor charging is depicted in Figure 10B. The inductor L_{ch} presented in the charging path provides high impedance and reduces the peak value $I_{\text{Ch,peak}}$ of capacitor charging current i_{Ch}. The $I_{\text{Ch,peak}}$ is expressed as follows

$$I_{\text{Ch,peak}} = \frac{V_{dc} - v_C}{\omega_{\text{ch}} L_{\text{ch}}} \tag{22}$$

where $\omega_{\text{ch}} = \frac{1}{\sqrt{L_{ch}C}}$ is the natural frequency of the charging circuit. From (22), it can be observed that the peak value of the capacitor charging current in quasi-resonant SCMLIs will be reduced by using high value of inductor L_{Ch} or with high ω_{Ch}. However, the parallel charge and series discharge technique used by the quasi-resonant SCMLI requires a large capacitance to limit the ripple voltage.

Basic unit of the proposed inverter containing integrated buck-boost converter is presented in Figure 1C. The equivalent circuits during inductor and capacitor charging are depicted in Figure 10C,D respectively. The peak value $I_{\text{LB,peak}}$ of the inductor current i_{LB} during its charging is expressed as follows

$$I_{\text{LB,peak}} = \frac{V_{\text{dc}} D}{L f_s} \tag{23}$$

where D is the duty cycle of the buck-boost converter. From Figure 10D, the peak value $I_{C,\text{peak}}$ of the capacitor current i_C is expressed as follows

$$I_{C,\text{peak}} = I_{\text{LB,peak}} - i_o = \frac{V_{\text{dc}} D}{L f_s} - i_o \tag{24}$$

From the (24), it is evident that the peak current is inversely proportional to the switching frequency. By using high switching frequency for the buck-boost converter operation, the peak currents of the inductor and capacitor can be reduced. Therefore, the peak current during the capacitor charging is lesser in the proposed inverter compared to the conventional and quasi-resonant SCMLIs.

3.4.2 | Capacitor size

In both parallel charge SCMLIs[15,18-20,27] and quasi-resonant SCMLIs,[22,23] the capacitor will be charged at low switching frequency, which is equals to the fundamental frequency of inverter output voltage. Also, the ripple voltage of the

capacitor increases with increase of load power. Hence, bulky capacitors will be required in parallel charge and quasi-resonant SCMLIs for low frequency high power applications. Let C_A is the capacitor in parallel charge and quasi-resonant SCMLIs and Δv_{CA} is its ripple voltage then the required C_A is expressed as follows.

$$C_A \propto \frac{1}{\Delta v_{CA} f_o} \tag{25}$$

Whereas, in the proposed buck-boost integrated SCMLIs, the capacitors will be charged at high switching frequency. Also, there is the path for capacitor charging while delivering power to the load. Thus, the capacitor size significantly less compared to the parallel charge SCMLIs and quasi-resonant SCMLIs. Let C_B is the capacitor in the proposed buck-boost charge SCMLI and Δv_{CB} is its ripple voltage then the required C_B is expressed as follows.

$$C_B \propto \frac{1}{\Delta v_{CB} f_s} \tag{26}$$

From (25) and (26), with $f_s >> f_o$ and to maintain same ripple voltages, the proposed inverter needs small capacitor.

4 | EXPERIMENTAL RESULTS

To verify the desired function of the proposed inverter, a proof-of-concept is developed as shown in Figure 11 for the specifications mentioned in the Table 4. TMS320F28379D digital signal processor is used to generate the gate pulses required for the proposed inverter.

The proposed inverter dynamic performance is examined with linear loads and the respective experimental waveforms of load voltage (v_o), load current (i_o) and capacitors voltages (v_{C1} and v_{C2}) are presented in Figure 12. The corresponding waveforms for the step change in R load (ie, from 510 W R load to 260 W R load) and load type (ie, from 510 W R load to 339 VA R-L load with 0.8 power factor) are shown in Figure 12A,B respectively. In both cases, it can

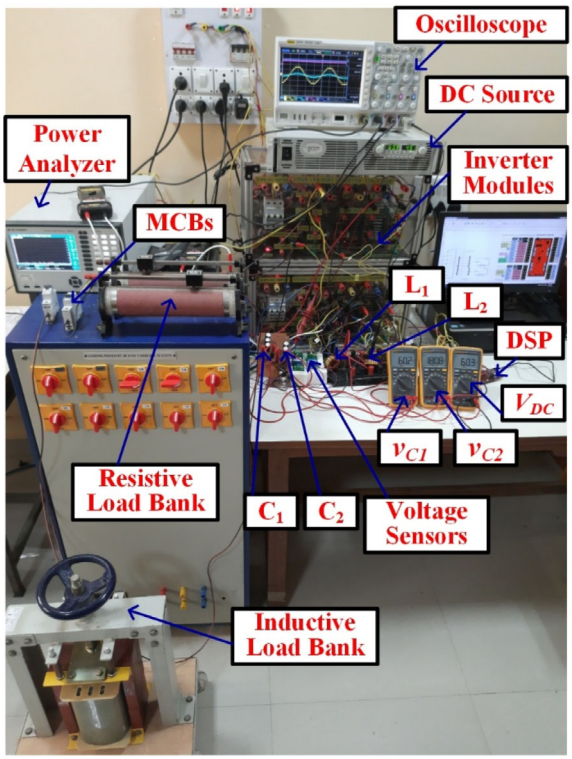

FIGURE 11 Experimental setup of the proposed inverter

TABLE 4 Specifications and design parameters of the proposed MLI for 11-level operation

Parameter	Value/part number
Input voltage (V_1)	60 V
Output voltage (V_o, RMS)	220 V
BBC's capacitors voltages (v_{C1}, v_{C2})	60 V, 180 V
Output frequency (f_o)	50 Hz
Switching frequency (f_s)	20 kHz
Peak output Power (P_o)	500 W
BBC's inductors (L_1, L_2)	156 μH, 117 μH
BBC's capacitors (C_1, C_2)	300 μF/400 V, 200 μF/400 V
Switches	IKW40T120
Diodes	STPSC2006CW
R load	95 Ω for 510 W load 180 Ω for 260 W load
R-L load	95 Ω & 200 mH for 339 VA, 0.8 P.F load 180 Ω & 200 mH for 228 VA, 0.94 P.F load
Nonlinear load	95 Ω & 400 mH for 405 W load
(with rectifier and R-L load)	180 Ω & 400 mH for 213 W load

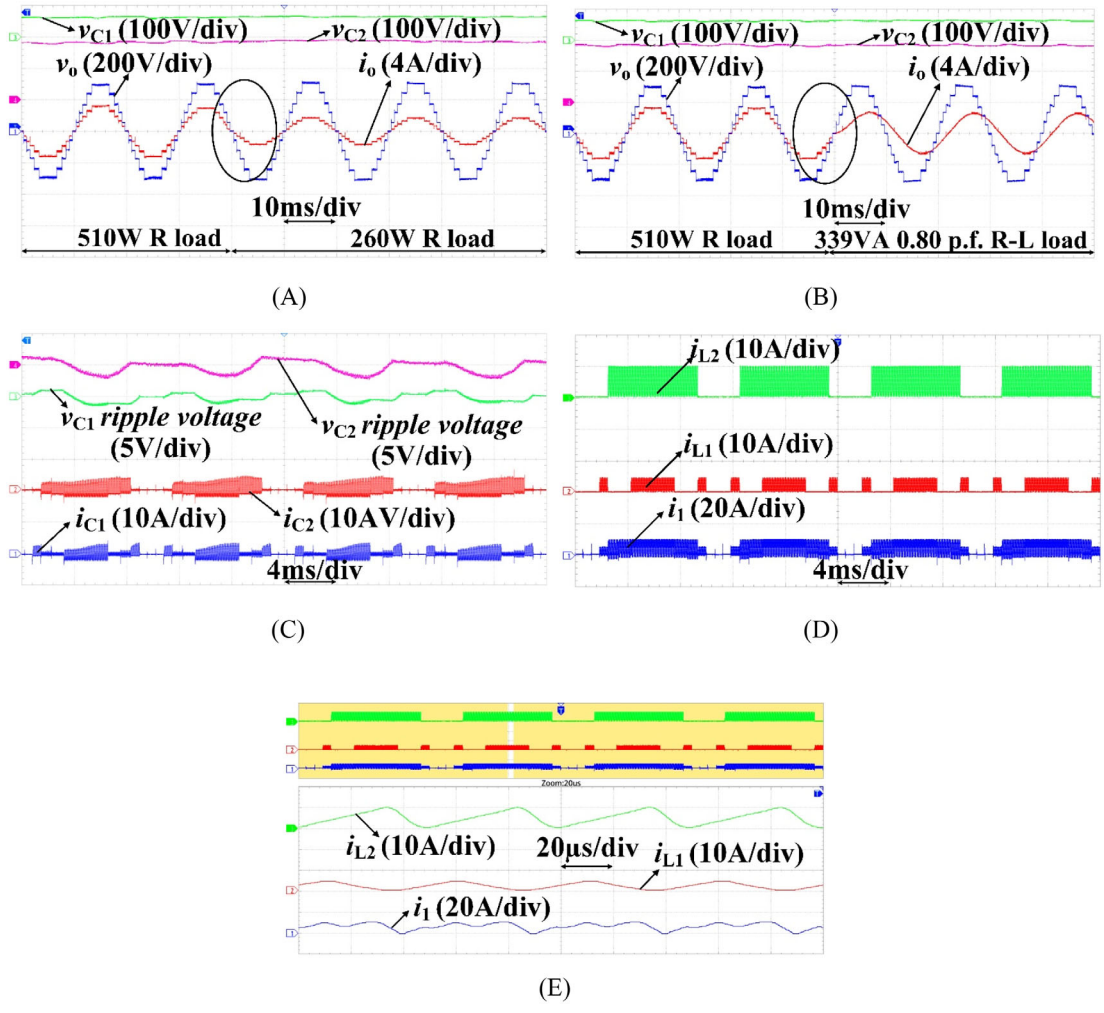

FIGURE 12 Experimental waveforms of the proposed inverter: (A) load voltage (v_o), load current (i_o) and capacitor voltages (v_{C1} and v_{C2}) during step change in R load for (ie, 510 W R load to 260 W R load) (B) v_o, i_o, v_{C1} and v_{C2} during step change in load type (ie, 510 W R load to 339 VA, 0.8 power factor R-L load) (C) capacitors C_1 & C_2 currents and ripple voltages (D) source current i_1, inductor currents i_{L1} and i_{L2} (E) zoomed version of source current i_1, inductor currents i_{L1} and i_{L2}

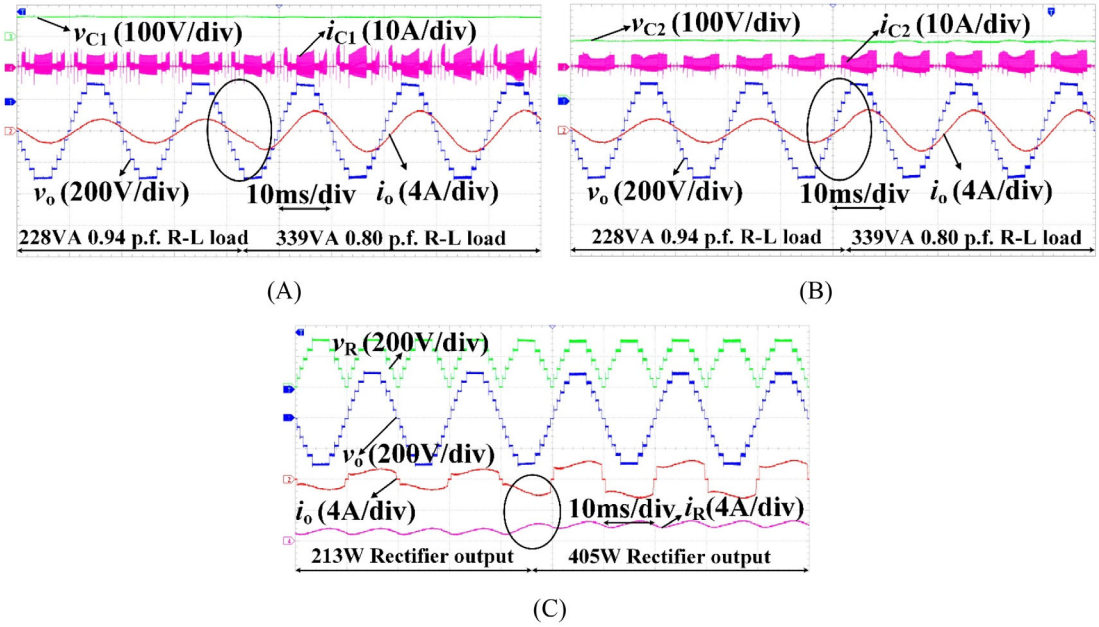

FIGURE 13 Experimental waveforms of the proposed inverter: (a) v_o, i_o, v_{C1} and i_{C1} during step change in RL load (ie, 228 VA, 0.94 power factor RL load to 339 VA, 0.8 power factor R-L load) (b) v_o, i_o, v_{C2} and i_{C2} during step change in RL load (ie, 228 VA, 0.94 power factor RL load to 339 VA, 0.8 power factor R-L load) (c) v_o, i_o, rectifier output voltage and output currents v_R and i_R during step change in nonlinear load (ie, 213- 405 W)

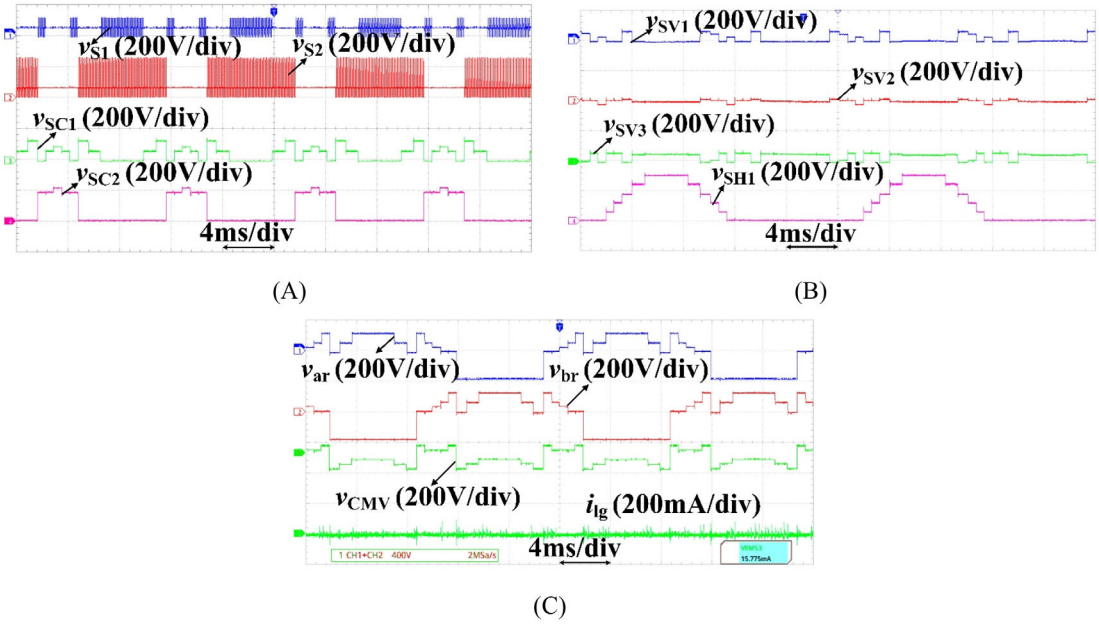

FIGURE 14 Experimental waveforms of the proposed inverter: (A) voltages of switches S_1, S_2, S_{C1} and S_{C2} (B) voltages of switches S_{V1}, S_{V2}, S_{V3} and S_{H1} (C) pole voltages v_{ar}, v_{br}, CMV and leakage current i_{lg}

be observed that the capacitor voltages (v_{C1} and v_{C2}) and load voltage (v_o) are unaltered and ensures the firm dynamic operation of the proposed inverter. The current and ripple voltage waveforms of capacitors C_1 and C_2 depicted in Figure 12C confirms that the ripple voltage is below 5%. Input current (i_1) and inductor currents (i_{L1} and i_{L2}) are depicted in Figure 12D. Also, the proposed inverter dynamic response during step change in R-L load is verified and the respective experimental waveforms of load voltage (v_o), load current (i_o), capacitors voltages (v_{C1} and v_{C2}), and capacitors currents (i_{C1} and i_{C2}) are presented in Figure 13A,B respectively.

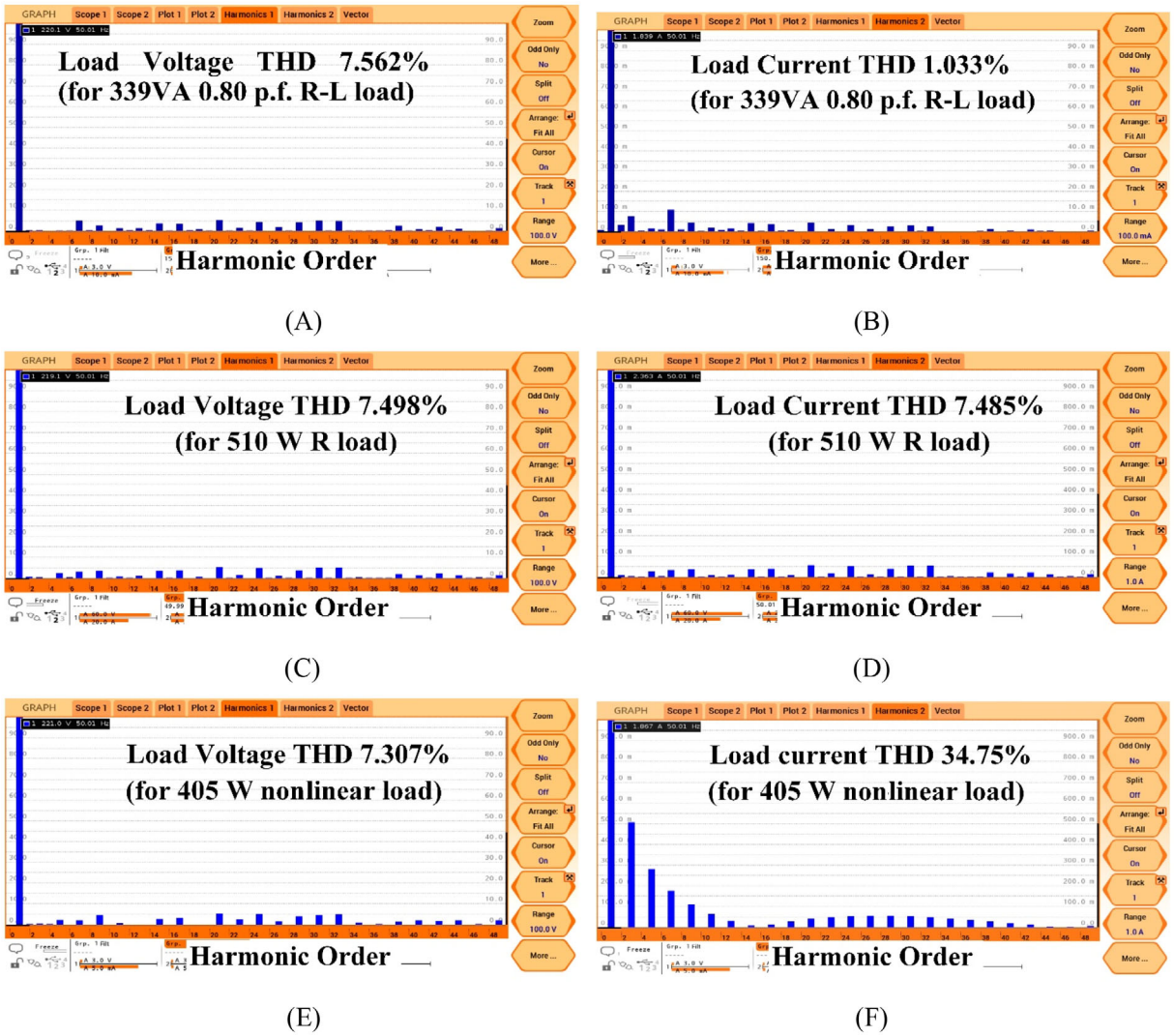

FIGURE 15 Experimental waveforms of the proposed inverter: (A) & (B) harmonic spectrum of v_o and i_o for 339 VA, 0.8 power factor R-L load respectively (C) and (D) harmonic spectrum of v_o and i_o for 510 W R load respectively (E) & (F) harmonic spectrum of v_o and i_o for 405 W nonlinear load respectively

TABLE 5 Power loss distribution of proposed inverter at different power ratings

Cond_INV (W)	0.90	1.81	2.82	3.77	4.58	5.72	6.70	7.68	11.77	12.81
Swi_INV (W)	0.08	0.08	0.08	0.09	0.09	0.10	0.10	0.10	0.13	0.13
Cond_BBC (W)	1.04	2.18	3.37	4.63	5.58	7.04	8.35	9.74	13.11	16.79
Swi_BBC (W)	3.12	3.97	4.68	5.34	5.81	6.48	7.04	7.61	9.77	10.28
Cond_L&C (W)	0.27	0.74	1.35	2.08	2.69	3.41	4.62	8.96	9.11	11.51
Total losses (W)	5.41	8.77	12.30	15.90	18.76	22.75	26.81	34.10	43.88	51.53
Output power (W)	50	100	150	200	250	300	350	400	450	500
Efficiency (%)	90.23	91.93	92.42	92.63	93.02	92.95	92.89	92.15	91.11	90.66

To verify the operation of the proposed inverter with nonlinear load, a rectifier with R-L load is considered and the load parameters are specified in Table 4. The corresponding load voltage (v_o), load current (i_o), rectifier output voltage (v_R), rectifier output current (i_R) waveforms for the step change in nonlinear load (ie, from 230 to 405 W) are shown in Figure 13C.

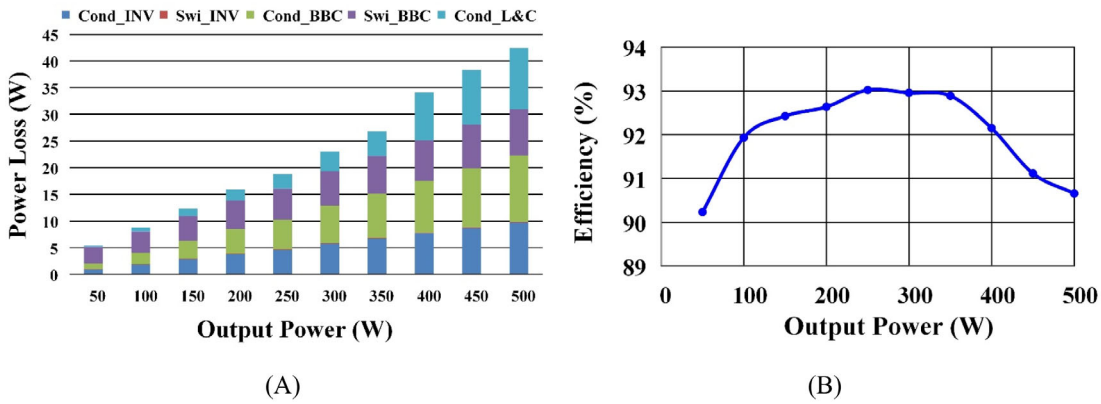

FIGURE 16 Proposed inverter: (A) Power loss distribution and (B) efficiency characteristics for 11-level operation at different output power conditions

The blocking voltage waveforms of the proposed inverter switches are depicted in Figure 14A,B. From these waveforms, it can be noticed that all the waveforms are of low frequency except for switches S_1 and S_2. Further, the pole voltages (v_{ar} and v_{br}), CMV and leakage current (i_{lg}) are presented in Figure 14C. As the switching frequency of the H-bridge and DC-link voltage are low, thus produces low frequency CMV, which results in low leakage current. From Figure 14C, the measured RMS value of the leakage current is 15.775 mA, which is significantly less than the VDE 0126-1-1 standard limit of 30 mA.

Without filter, the measured THD of load voltage and load current for 510 W R load are 7.498% and 7.485%, for 339 VA, 0.8 p.f R-L load are 7.562% and 1.033% and for 405 W nonlinear load are 7.307% and 34.75% respectively.

The voltage and current harmonics for 510 W R load, 339 VA, 0.8 p.f R-L load and 405 W nonlinear load are presented in Figure 15.

Thermal model of the proposed inverter is developed by using PLECS software to evaluate the power losses of the various sections presented in the proposed inverter. The calculated switching losses (Swi_Inv and Swi_BBC) and conduction losses (Con_Inv and Con_BBC) of inverter and buck-boost network of the proposed inverter are presented in Table 5 and Figure 16A for different output power conditions. It can be observed that the buck-boost network constitutes majority losses than the other network of the proposed inverter. Further, the efficiency curves of the proposed inverter for the input voltage of 60 V at different output powers are presented in Figure 16B.

5 | CONCLUSIONS

A new buck-boost integrated multilevel inverter with reduced components and capacitor size is proposed. The design procedure and generalized operation of the proposed inverter are presented. A 500 W proof-of-concept of the proposed inverter for 11-level operation is developed. The detailed experimental results for dynamic R load, R-L load, and nonlinear load is demonstrated. The THD of output voltage without filter is obtained as 7.498% and 7.562% for R load and R-L load, respectively. A comprehensive comparative study of the proposed topology and recent SCMLIs for 11-level operation is presented, which shows that the proposed inverter offers a voltage gain of 5 with reduced components and compact capacitors. Also, it provides low frequency CMV and low leakage current of 15.775 mA (RMS) which is significantly less than the VDE 0126-1-1 standard limit of 30 mA. Hence, it is a potential candidate for PV and EV applications with low input voltage.

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PEER REVIEW

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available within the article and also appropriate references are cited.

ORCID

Madhu Babu Sambhani https://orcid.org/0000-0001-5309-3157
Narasimharaju B.L. https://orcid.org/0000-0002-3033-5712

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