Two-quadrant Clamping Inverter Scheme for Three-level Open-end Winding Induction Motor Drive

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***Abstract*—This article proposes a space-vector based pulse width modulation (SVPWM) scheme for a three-level dual-inverter-fed open-end winding induction motor drive. The proposed method introduces clamping of one inverter for 180^o span of the rotation of the reference space vector. The proposed scheme neither requires sector identification nor lookup tables for the generation of the gating pulses. The switching pattern adopted in the present work ensures alternative clamping and switching modes every 180^o for both the inverters. In the present scheme, the zero sequence currents are denied a path by using isolated power supplies. The proposed switching strategy envisages two-quadrant clamping of the inverters which results in lowering of the losses that occur in power electronic switches. Simulation studies have been carried out for the proposed SVPWM strategy using MATLAB/Simulink.**

Keywords—pwm; space vector, open-end winding, induction motor, clamping, three-level, nshc.

I. INTRODUCTION

Multilevel inverters are capable of generating stepped output voltage waveform with less harmonic content [1]. Since the source voltages are lesser in a multilevel inverter, the stresses that occur in the power electronic switching devices are significantly reduced. With less device raring and with several stages, a pure sinusoidal output could be obtained, which made them as a better alternative for medium and high power ac drives. Several topologies have been put forward by researchers: Neutral-Point Clamped (NPC) inverters [1], cascaded H-bridge inverters [2], flying capacitor multilevel inverters [3] and dual-inverter fed open-end winding induction motor (OEWIM) drive [4] are the few popular topologies which are suitable for high power industrial applications.

Since the DC-link capacitors have to carry the load current, the Neutral-Point-Clamped multilevel inverters experience neutral-point fluctuations. In flying capacitor topology, the neutral clamping diodes are eliminated but require as many capacitors as floating DC-link sources. Higher number of levels is obtainable with series connected hybrid topology are more complex [5][6]. The cascaded topology is generally employed in high power industrial drives, electric vehicles, and grid connection of photovoltaic cell generation systems [7]. Open-end winding induction motor drive topology is chosen for the present work due to the absence of neutral-point fluctuations, more switching redundancies and half-rated DC-link. Pulse Width Modulation (PWM) techniques are the best suited control techniques for multilevel inverters. SVPWM is a v/f control technique in which the null vectors are equally placed at both the ends of a sampling period sandwiching the effective time period in between them. This results in lower Total Harmonic Distortion (THD) [8].

A new SVPWM scheme is proposed for three-level open-end winding induction motor drive. The proposed scheme neither requires sector identification nor lookup tables for the generation of the gating pulses.

II. THREE-LEVEL OPEN-END WINDING INDUCTION MOTOR DRIVE WITH ISOLATED POWER SUPPLIES

Three-level inversion can be realized by two two-level inverters feeding from either ends of an open-end winding induction motor. Practically, the open-end induction motor is formed by removing the star point of the stator forming two terminals per phase of the stator winding. Thus six terminals are available in an open-end winding induction motor. This modified induction motor can be connected to two-level inverters from either ends. This arrangement of open-end winding induction motor drive results in the generation of three-level output voltage which is similar to other popular topologies such as NPC, flying capacitor and H-bridge multilevel inverters as shown in Fig.1. Additionally, the topology considered in the proposed work requires half-rated DC-link capacitors. With the reduced DC-link capacitors the device ratings are also reduced by half, which results in lesser switching losses compared to the conventional multilevel configurations. Moreover, OWEIM drive offers affluent switching redundancy. Thus for realizing a space vector, different switching combinations are possible with OEWIM drive.

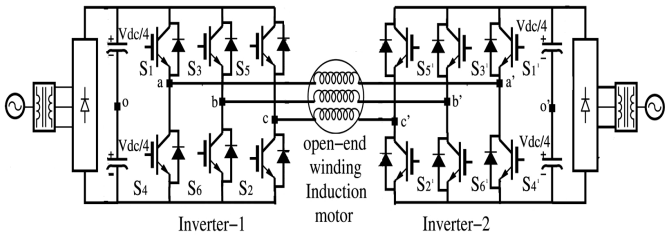

Fig.1. Schematic of Dual inverter-fed three-level OEWIM with electrical isolation

Fig.2. shows the space vector locations for inverter-1 and inverter-2 wherein the switching states of individual inverters

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are shown in Table I and the resultant space vector combinations and their locations is shown in Fig.3. in which there are 64 space vector combinations, which form the vertices of 24 equilateral sectors that are spread across the 19-space vector locations.

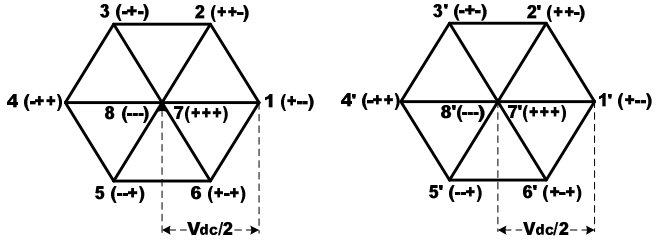

Fig.2. Space vector locations of inverter-1 (left) and inverter-2 (right)

Also it can be observed that there exist a base hexagon with its centre 'O' and its boundaries are marked by the 'A, B, C, D, E, F', which again forms the centers of six concurrent hexagons.

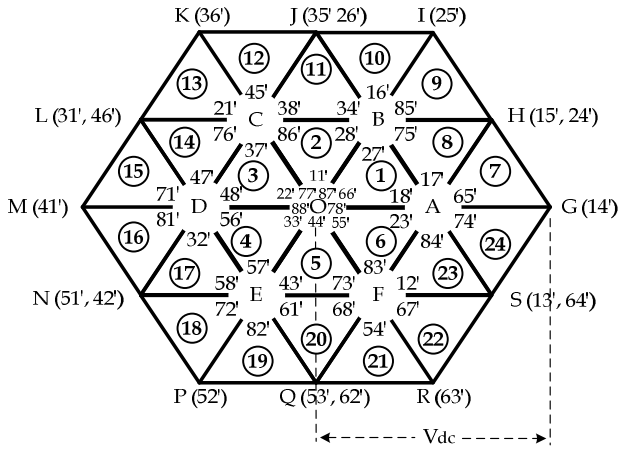

Fig. 3. Resultant space vector combinations for dual-inverter scheme

V_{a0}, V_{b0} and V_{c0} represents pole voltages of inverter-1 and $V_{a'0'}$, $V_{b'0'}$ and $V_{c'0'}$ represents pole voltages of inverter-2. The individual pole voltage of inverter-1 and inverter-2 can attain either $V_{dc}/2$ or $-V_{dc}/2$.

TABLE I
SWITCHING STATES OF INDIVIDUAL INVERTERS

State of Inverter-1	Switches turned ON	State of Inverter-2	Switches turned ON
1 (+ - -)	S6, S1, S2	1' (+ - -)	S6', S1', S2'
2 (+ + -)	S1, S2, S3	2' (+ + -)	S1', S2', S3'
3 (- + -)	S2, S3, S4	3' (- + -)	S2', S3', S4'
4 (- + +)	S3, S4, S5	4' (- + +)	S3', S4', S5'
5 (- - +)	S4, S5, S6	5' (- - +)	S4', S5', S6'
6 (+ - +)	S5, S6, S1	6' (+ - +)	S5', S6', S1'
7 (+ + +)	S1, S3, S5	7' (+ + +)	S1', S3', S5'
8 (- - -)	S2, S4, S6	8' (- - -)	S2', S4', S6'

The difference of the pole voltages will show the three-levels such as V_{dc} , 0 and $-V_{dc}$ of the OEWIM drive denoted by $V_{aa'}$, $V_{bb'}$ and $V_{cc'}$ as shown in Table II. This configuration offers high degree of freedom in choosing the switching combinations to realize a given space vector.

TABLE II
POLE VOLTAGES OF INDIVIDUAL INVERTERS AND MOTOR PHASE VOLTAGE

Pole Voltage of Inverter-1	Pole Voltage of Inverter-2	Motor Phase Voltage
$V_{dc}/2$	$V_{dc}/2$	0
$V_{dc}/2$	$-V_{dc}/2$	V_{dc}
$-V_{dc}/2$	$-V_{dc}/2$	0
$-V_{dc}/2$	$V_{dc}/2$	V_{dc}

The Zero Sequence Voltage (V_{zs}) corresponding to the motor phase voltages $V_{aa'}$, $V_{bb'}$ and $V_{cc'}$ is defined as $V_{zs} = (1/3)(V_{aa'} + V_{bb'} + V_{cc'})$. The zero sequence voltages can be arrested by using two isolated power supplies and the zero sequence voltage is dropped across O and O' as shown in Fig .1.

III. TWO-QUADRANT CLAMPING INVERTER SCHEME

The principle of two-quadrant clamping inverter scheme is depicted in Fig. 4. In Fig.4, OT represents the voltage space vector with its tip situated in sector-7 [10]. Modulation index (m_a) is defined as the ratio of the length of the reference space vector OT to the DC-link voltage (i.e. $|OT|/V_{dc}$). Vector OT can be split into two components namely OA & AT. The output of inverter-1 is the component OA and the output of the inverter-2 in the average sense is realized for obtaining the component AT by switching around the SHC 'A' as shown by the shaded region in Fig. 4. To obtain OA, inverter-1 is clamped to state-1 (+ - -) and AT is synthesized by the switching inverter-2 amongst the nearest three vertices of the triangular sector in which it is situated. When the reference space vector exits the SHC-A and enters into SHC-B, inverter-1 is clamped to state 2 (+ + -), while inverter-2 is switched. Thus inverter-1 is clamped to states 1 (+ + -), 2(+ + -), 3 (- + -) and 4 (- + +) if the SHC is A, B, C or D. Thus inverter-1 is in clamping mode for the entire 180° (two quadrants) of the rotation of the reference space vector, while inverter-2 will be in switching mode. During the subsequent quadrants, the inverter-2 is clamped to states 1' (+ + -), 2' (+ + -), 3' (- + -) and 4' (- + +) if the SHC is D, E, F or A. Thus inverter-2 is in clamping mode for the entire 180° (two quadrants) of the rotation of the reference space vector, while inverter-1 will be in switching mode.

It should be noted from Fig.4 that SHC-A and SHC-D are the only two SHCs where there is a transition in the clamping inverters between inverter-1 to inverter-2 and vice-versa respectively. This phenomenon can be explained by considering SHC-A, depending upon the value of , the entire 60° marked by OSGH can be split into two regions, OSG & OGH which lies within 330° to 0° and 0° to 30° respectively. If the reference space vector lies within the first region (i.e. OSG), inverter-2 is clamping inverter with a clamping state of

4' (- + +) and inverter-1 is the switching inverter. If the reference space vector lies within the next region (i.e. OGH), inverter-1 is the clamping inverter with clamping state of 1 (+ - -), while inverter-2 is the switching inverter. Similarly, the in the region OLMN, if the reference space vector is in OLM, inverter-1 is clamping inverter which is being clamped to state 4 (- + +), while inverter-2 is in switching mode and during 180^o to 210^o (i.e. region OMN), inverter-2 is clamped to state 1 (+ - -) while inverter-1 is switched around it.

Thus inverter-1 will always be in clamping mode and inverter-2 will be in switching mode for the values of ranging between 0^o and 180^o. Similarly, on the other hand, if the location of the reference space vector lies within 180^o to 360^o and depending upon the SHC, inverter-2 is the clamping inverter, while inverter-1 is the switching inverter.

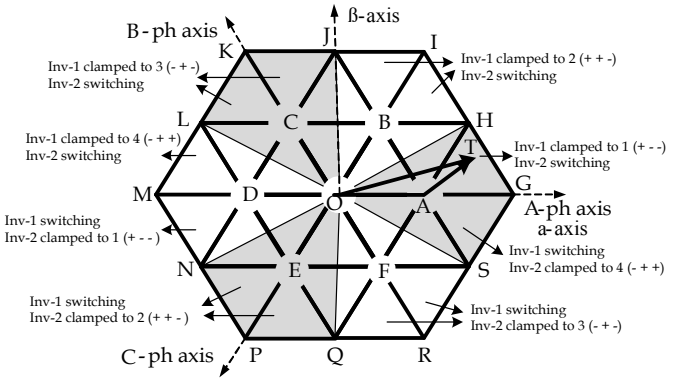

Fig.4. Principle of two-quadrant clamping inverter PWM strategy

The instantaneous three phase references corresponding to the reference vector OT are denoted by V^*a , V^*b, and V^*c. The components of OT along the $\alpha-$ and the $\beta-$axes, namely OU and OX in Fig.4 are respectively denoted as $V^*\alpha$ and $V^*\beta$. The modified instantaneous voltage phase references corresponding to the switching vector AT, denoted by Va , Vb *and* Vc are obtained by the following procedure [10]:

A. The instantanesous three phase reference voltage corresponding to the reference vector OT are transformed into the equivalent two-phase system refrences $V^*\alpha$ *and* $V^*\beta$ using the classical 3-ph to 2-ph transformation.

B. The SHC situated nearest to the tip of the reference vector OT (NSHC) is then determined.

C. Whenever inverter-1 is used as the clamping inverter (at SHCs A, B, C & D), the corresponding vector (OA, OB , OC or OD) is output by inverter-1. The co-ordinates of the switching vector (AT in the present case) denoted as $V\alpha,sw$ and $V\beta,sw$ are given by:

$V\alpha,sw = V^*\alpha - V\alpha,nshc$ and $V\beta,sw = V^*\beta - V\beta,nshc$;

where $V\alpha,nshc$ and $V\beta,nshc$ are the co-ordinates of the NSHC.

The modified reference voltages V_a, V_b and V_c for the swithcing inverter are then obtained by transforming $V\alpha,sw$, $V\beta,sw$ into the corresponding three phase variables by using the classical 2-ph to 3-ph transformation.

D. When inverter-2 is employed as the clamping inverter, the modified references are used directly to generate the switching vector AT with inverter-1. On the other hand, if inverter-1 is used as the claming inverter, the modified references must be negated to generate the switching vector AT with inverter-2.

The switching algorithm presented in [11] for a conventional 2-level inverter is extended to this three-level dual-inverter drive, to generate the gating signals for the switching inverter.

IV. RESULTS AND DISCUSSION

The proposed PWM scheme for three-level dual inverter fed open- end winding induction motor drive is validated with simulation studies using MATLAB/Simulink.

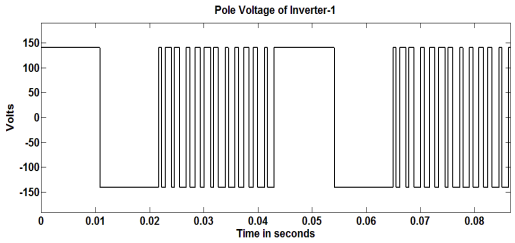

Fig. 5. Pole Voltage of Inverter-1 (ma=0.4)

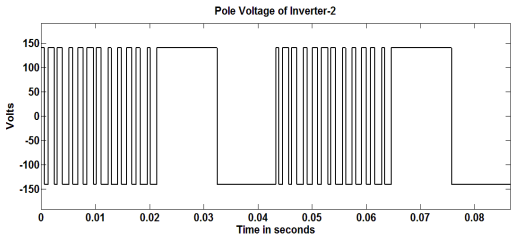

Fig. 6. Pole Voltage of Inverter-2 (ma=0.4)

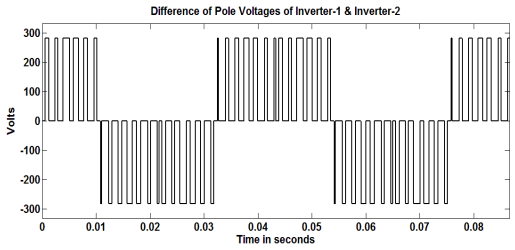

Fig. 7. Difference of Pole Voltage of Inverter-1 & Inverter-2 (ma=0.4)

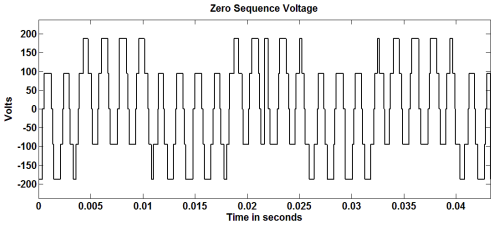

Fig. 8. Zero Sequence Voltage (ma=0.4)

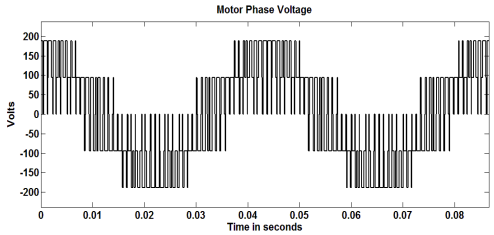

Fig. 9. Motor Phase Voltage (ma=0.4)

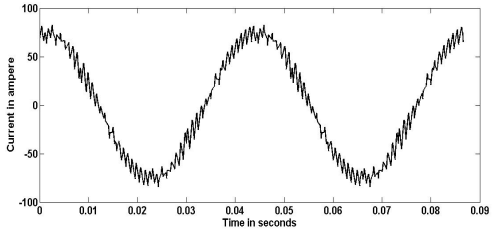

Fig. 10. Motor Phase Current (ma=0.4)

Fig.5 to Fig.10 shows the simulated waveforms for the modulation index of 0.4. Fig.5 shows the pole voltage of Inverter-1 and Fig.6 shows the pole votlage of Inverter-2. The three-level inversion for an open-end winding induction motor can be realized from the difference of the pole voltages of Inverter-1 and Inverter-2, which is depicted in Fig.7. As mentioned earlier, since the present scheme is operated with isolated power supplies, the zero sequence voltage is dropped across *O* and *O'* which is shown in Fig.8. Fig.9 depicts the motor phase voltage after subtracting the zero sequence voltage from the difference of the pole voltages of inverter-1 and inverter-2 for the modulation index of 0.4. The motor phase voltage obtained from the proposed switching strategy is fed to preset induction motor model in Simulink and the obtained motor current waveform is shown in Fig.10.

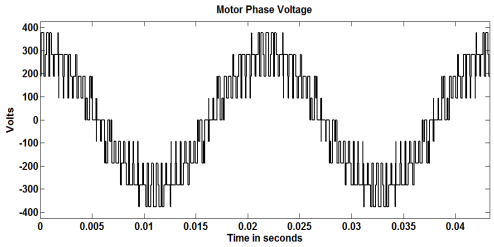

Fig. 11. Motor Phase Voltage (ma=0.8)

Fig.11 and Fig.12 depicts the motor phase voltage after subtracting the zero sequecne voltage from the difference of the pole voltatges of inverter-1 and inverter-2 (which are not presented here for the sake of limiting the total number figures) for modulation indices of 0.8 and 1 respectively.

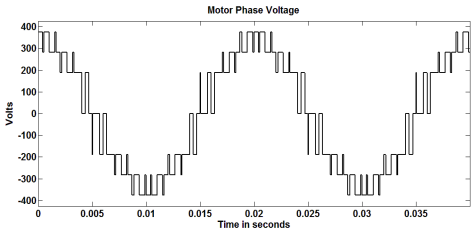

Fig. 12. Motor Phase Voltage (ma=1)

V. CONCLUSION

A new space-vector based pulse width modulation (SVPWM) scheme for a three-level dual-inverter-fed open-end winding induction motor drive has been proposed. Look up tables and sector identification is not necessary for the generating gating pulses, which reduces the computing. The proposed switching scheme ensures alternating of clamping- and switching- modes every 180^o for both the inverters. Two isolated power supplies with electrical isolation are used to forbid the flow of zero sequence currents. Since the inverters are clamped for 180^o, the proposed PWM scheme may lower the losses that occur in the power semiconductor switches.

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