New Single-Stage Boost Multilevel Inverter

Sambhani Madhu Babu
Dept. of Electrical Engineering
NIT Warangal, India
sam1729@student.nitw.ac.in

B.L.Narasimharaju
Dept. of Electrical Engineering
NIT Warangal, India
blnraju@nitw.ac.in

Akshay Kumar Rathore
Dept. of Electrical Engineering
Concordia University, Montreal,Canada
akshay.rathore@concordia.ca

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***Abstract*—In this paper, new single-stage boost multilevel inverter (MLI) is presented. A proposed 5-level basic unit is proposed, which is utilized for the construction of generalized symmetrical and asymmetrical configurations.The proposed topology provides high boost factor with reduced capacitor count and size. The design of 11-level inverter is explained in detailed, and also, simulation results for steady-state and dynamic load conditions are portrayed. Additionally, a few key parameters of proposed topology are compared with recent existing MLIs and tabulated.**

***Index Terms*—Step-up inverters, multilevel inverters, switched capacitor, boost DC-link, cascaded multilevel inverters.**

I. Introduction

Recent times, the inverter topologies are drastically transforming in order to meet the requirements of different applications such as uninterruptible power supplies (UPS), photovoltaic grid connected system, electrical vehicles etc. thereby, the traditional two-level inverters with transformer are replaced by transformerless boost inverters. Generally, front-end dc-dc converter based two stage inverters like z-source [1], quasi-inverter [2] are capable of boost input DC voltage. But, these two-stgae transformerless inverters suffer from high voltage & current stresses and less efficiency. Also, recently evolved switched capacitor multilevel inverter (SCMLI) topologies [3]–[7] produce quality output with high boost factor and efficiencies. However, these SCMLI's operating techniques leads to increased capacitor count and size with increase in number of levels and output power requirements. Thus, in this paper a new single stage boost multilevel inverter is proposed with reduced capacitor count, size and improved boost factor. The design procedure for proposed 11-level inverter of 1kW and its simulation results are presented. The simulation analysis under steady-state and dynamic load conditions are discussed in detail.

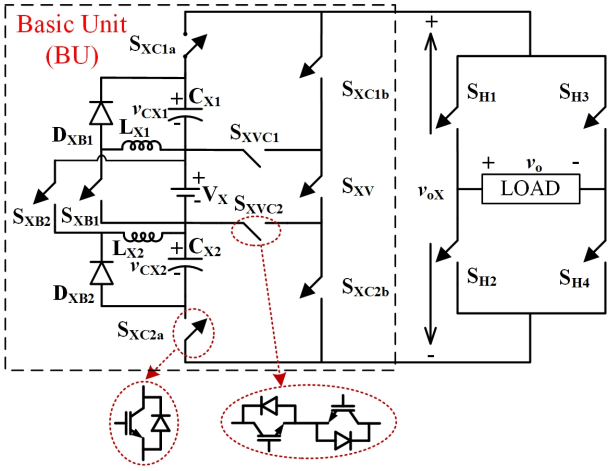

Fig. 1. Proposed Basic Unit of MLI.

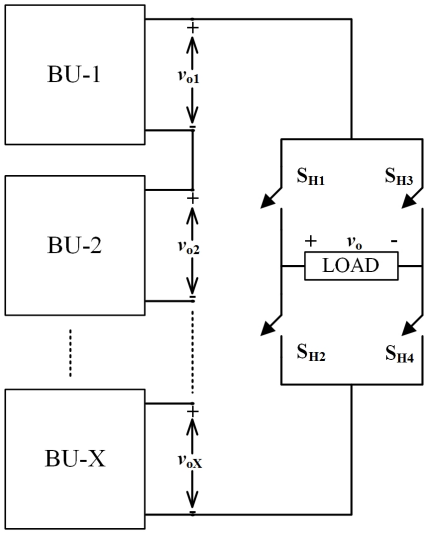

Fig. 2. Generalized circuit diagram of the proposed MLI

II. Proposed Multilevel Inverter

The proposed multilevel inverter is shown in the Fig. 1. The basic unit (BU) shown in Fig.1 consists a DC source V_X, two integrated buck-boost converters (BBC) and level selecting circuitry (LSC). Each BBC is constructed by using

an inductor L_{Xn}, capacitor C_{Xn}, boost switch S_{XBn} and boost diode D_{XBn} (where n=1 or 2). These BBC circuits help the capacitors to charge to the desired values v_{CX1} and v_{CX2}, which are x_{X1} and x_{X2} times of DC source magnitude V_X. The LSC is developed with the help of switches S_{XC1a}, S_{XC1b}, S_{XC2a}, S_{XC2b}, S_{XV}, S_{XVC1}, & S_{XVC2}. Either (x_{X1}=1 and x_{X2}=3) or (x_{X1}=3 and x_{X2}=1) is chosen in order get maximum levels (i.e.,5 levels) out of the proposed BU. The conducting semiconductor devices during respective output levels of BU are given in TABLE I. The generalized cascaded single-stage boost multilevel inverter is presented in Fig. 2, which consists cascaded connection of X number of BUs for level generation and H-bridge for inversion. The generalized topology can be operated either in symmetric or asymmetric mode and the maximum number of output levels in symmetric ($N_{symm,max}$) and asymmetric ($N_{asymm,max}$) are expressed as follows

$$N_{symm,max} = 10X + 1 \tag{1}$$

$$N_{asymm,max} = 2 * 6^X - 1 \tag{2}$$

where X is equals to the number of basic units.

With one BU i.e., X=1, the proposed inverter produces a 11-level output voltage waveform. The capacitor voltage ratios are taken as $x_{11} = 1$ and $x_{12} = 3$ that means $v_{C11} = V_1$ and $v_{C12} = 3V_1$. The duty cycle d_{1B1} & d_{1B2} of BBC converters are expressed as

$$d_{1B1} = \frac{x_{11}}{1 + x_{11}} \tag{3}$$

$$d_{1B2} = \frac{x_{12}}{1 + x_{12}} \tag{4}$$

The critical inductance and capacitance can be calculated from the following equations

$$L_{11,critical} = \frac{d_{1B1}^2 R}{2x_{11}(1 + x_{11} + x_{12})f_s} \tag{5}$$

$$L_{12,critical} = \frac{d_{1B2}^2 R}{2x_{12}(1 + x_{11} + x_{12})f_s} \tag{6}$$

$$C_{11,critical} = \frac{(1 + x_{11} + x_{12})d_{1B1}}{k_{11}x_{11}Rf_s} \tag{7}$$

$$C_{12,critical} = \frac{(1 + x_{11} + x_{12})d_{1B2}}{k_{12}x_{12}Rf_s} \tag{8}$$

where
R = load resistance
f_s=switching frequency of BBCs
k_{11}=capacitor C_{11} ripple voltage ratio
k_{12}=capacitor C_{12} ripple voltage ratio
The inductance values higher than above given boundary values will make the BBCs to operate in continuous current mode (CCM). Similarly lesser values will make them to operate in dis-continuous current mode (DCM).

III. Comparative Study

In this section, the various parameters like number of semi-conductor devices, passive components etc. used in proposed converter are compared with other recently evolved SCMLIs and the statistics are tabulated in TABLE II.

The proposed topology is providing a boost factor of 5, which is equals to [3] and higher than the [4] & [5] but, the proposed topology requires two capacitors only. Compared to all the remaining SCMLIs the proposed topology requires less size capacitor in terms of hundreds of micro farads where the remaining require in terms of milli farads.

TABLE I

SWITCHING STATES OF BASIC UNIT

On State Devices	Boost Converter		v_{0X}
	BBC-1	BBC-2	
$S_{XC1b}, S_{XV}, S_{XC2b}$	OFF	OFF	0
$S_{XC1b}, S_{XVC1}, S_{XVC2}, S_{XC2b}$			V_X
$S_{XC1a}, S_{XVC1}, S_{XV}, S_{XC2b}$			v_{CX1}
$S_{XC1b}, D_{XV}, S_{XVC2}, S_{XC2a}$			v_{CX2}
$S_{XC1a}, S_{XVC2}, S_{XC2b}$	ON	OFF	$V_{X1} + v_{CX1}$
$S_{XC1b}, S_{XVC1}, S_{XC2a}$	OFF	ON	$V_{X1} + v_{CX2}$
S_{XC1a}, S_{XC2a}	ON	ON	$V_{X1} + v_{CX1} + v_{CX2}$

TABLE II

COMPARISON BOOST MULTILEVEL INVERTER

Topology	[4]	[5]	[3]	Proposed
N_{IGBT}	10	16	12	15
N_{Diodes}	1	2	4	2
$N_{Sources}$	1	2	1	1
N_{Levels}	9	13	11	11
$N_{Capacitors}$	2	4	4	2
$N_{Inductors}$	-	-	-	2
$v_{0,peak}/\Sigma(V_{in})$	2	3	5	5

IV. Simulation Results

The proposed 11-level topology operation is verified using simulation studies in MATLAB/SIMULINK. A 1000 W, R-L load at 0.8 power factor with R = 30 Ω, L = 70 mH, V_1 = 60 V, V_0 = 215 V (RMS), L_{11} = 75 μH, L_{11} = 56.25 μH, C_{11} = 400 μF, C_{12} = 200 μF, f = 50 Hz & f_s = 10 kHz is simulated. Two PI controllers are implemented to control the BBC to maintain the capacitor voltages at desired values for dynamic load conditions. For the inverter switches stair-case PWM is applied. The steady state simulation results are presented in the Fig. 3. From Figs. 3d & 3e it can be observed that the capacitor C_{11} & C_{12} ripple voltages are 5.8 V (9.66%) & 10

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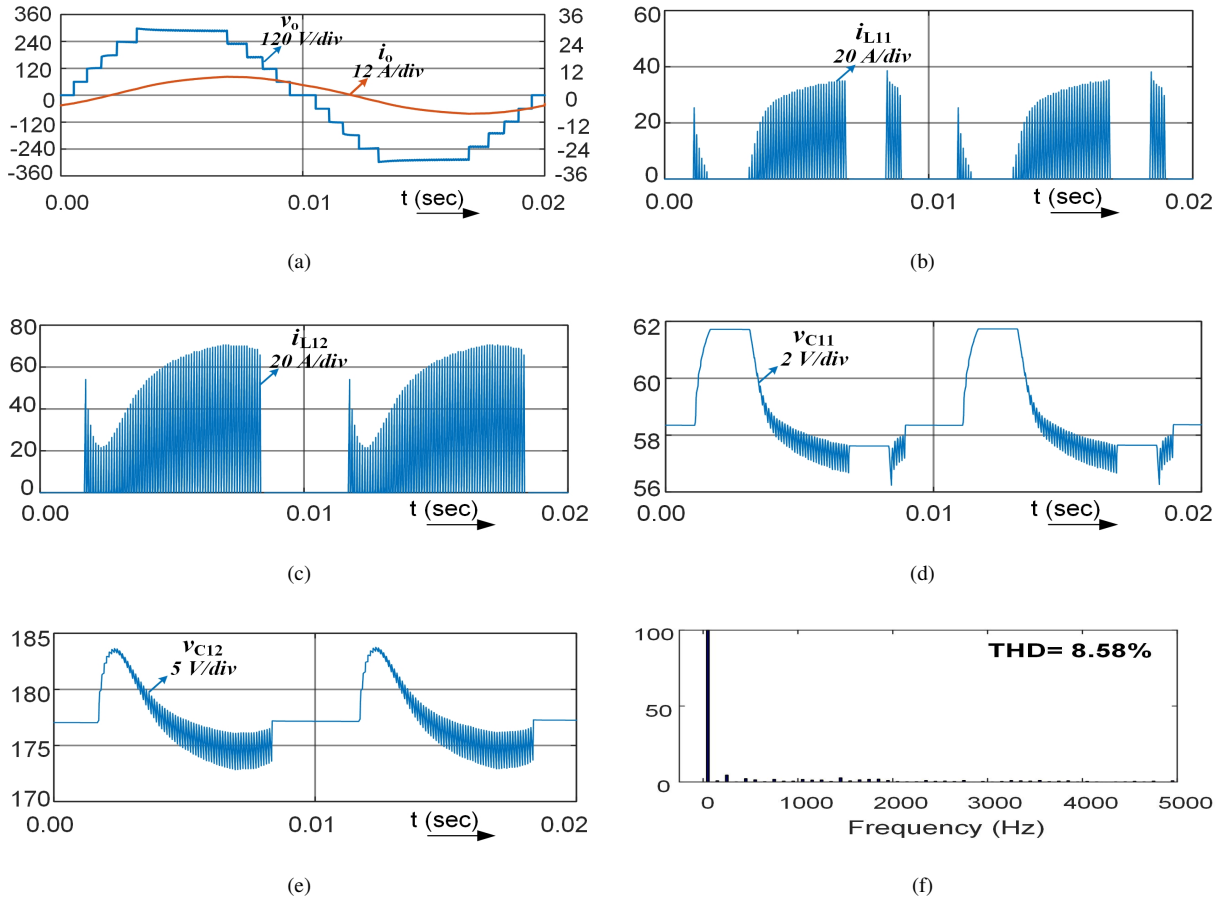

Fig. 3. Steady state simulation waveforms (a) load voltage v_0 (V) and current i_0 (A) (b) inductor L_{11} current iL_{11} (A) (c) inductor L_{12} current iL_{12} (A) (d) capacitor C_{11} voltage vC_{11} (V) (e) capacitor C_{12} voltage vC_{12} (V) (f) harmonic spectrum of load voltage (%)

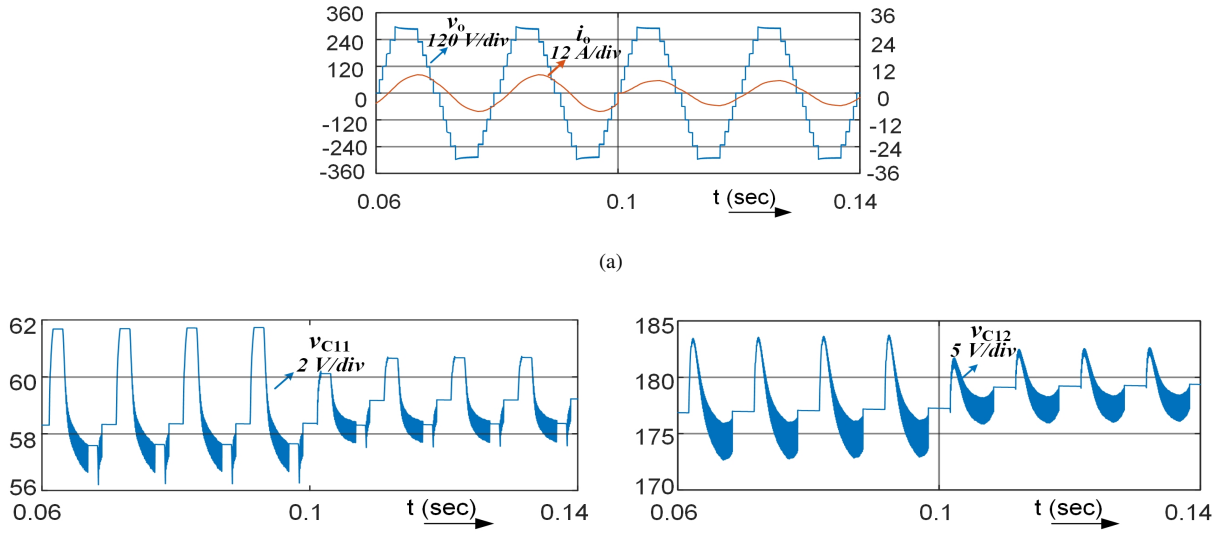

Fig. 4. Simulation waveforms during step change in R-L load (1000 W to 780 W) (a) load voltage v_0, load current i_0 (A) (b) capacitor C_{11} voltage vC_{11} (V) (c) capacitor C_{12} voltage vC_{12} (V)

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V (5.5%) respectively. The total harmonic distortion (THD) of load voltage is measured as 8.58% and its harmonic spectrum is depicted in Fig. 3f. To test the dynamic behaviour of the proposed MLI, a step change in R-L load (from 1000 W to 780 W) is applied at 0.1 seconds and the respective load voltage, load current & capacitor voltages are depicted in Fig. 4. From Fig. 4a it can be observed that the load voltage is constant even the load current is changed at 0.1 seconds.

V. Conclusion

In this paper, new single stage boost multilevel inverter is presented to overcome the drawbacks in the existing SCMLIs. The design procedure for 11-level inverter is given, from this it is evident the requirement of capacitance is less compared to its counterparts. Its operation is verified for R-L load using simulation analysis and the results are showcased. Output voltage of the proposed 11-level inverter without any filter is 8.58%.

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