Novel Non-Isolated Differential Buck-Boost Inverter with Single-Stage Conversion and Reduced Device Voltage Stress

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***Abstract*—Differential boost inverters (DBI) formed by differentially connected two dc-dc converters to produce single-phase AC voltage. DC-DC converters in DBIs are developing the voltage higher than peak of the output voltage waveform and experiencing higher voltage and current stresses. Thereby causing more power loss and lower efficiency issues. In this paper, new differential buck-boost inverter (DBBI) is presented to reduce the voltage stress of semiconductor devices and inductor currents. The detailed operation of the proposed inverter is explained. Also, simulation results and comprehensive comparative analysis are presented.**

***Index Terms*—Differential Inverter, Boost Inverter, Single Stage, Transformerless**

I. Introduction

In recent times, single stage transformerless inverters became popular in various applications like photovoltaic, electric vehicles, uninterrupted power supplies (UPS) and micro-grids etc. In conventional transformerless inverter, a front end DC-DC converter step-ups low voltage DC input and later inverter generates the AC waveform. This two stage conversion leads to low efficiency and high component count hence, raised attention towards single stage transformerless inverter topologies. Differential boost inverter proposed in [1]–[3] provided single stage power conversion from low voltage DC to high voltage AC by the differential connection of two DC-DC converters. DBI topologies produce good quality AC waveform with less filter components and its inherent L-C-L filter functionality is explained in [4]. Few control power decoupling techniques [4]–[8] are presented to reduce the input second harmonics and to control non-linear loads. Conventionally, DBI topologies use full cycle modulation (FCM) to generate two sinusoidal signals of 180 degrees phase shift. Here, both the converters are operating all the time causing high inductor currents and power loss. To reduce the inductor currents half cycle modulation (HCM) is proposed in [9], where one of DC-converter is OFF for one half of the output waveform cycle while the other is operated with modulation. Still there is passage of load current through the inductor during converter OFF period. Further, Improved DBI (IDBI) is proposed in by the incorporation of clamping switches in DBI to bypass the converter during OFF period. The DC-DC converters presented in existing DBI topologies generating voltage more than the peak of the output voltage waveform so, experiencing high blocking voltage across the semiconductor devices and capacitors. To address these issues a new differential buck-boost inverter is proposed. The proposed DBBI provides reduced voltage stress of switches and current stresses of the inductors.

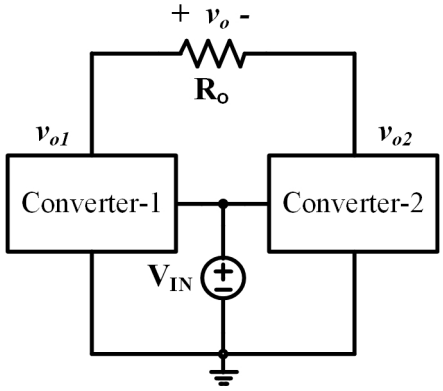

Fig. 1. Basic Structure of Differential Boost Inverter

II. Existing Differential Boost Inverters and Modulation Techniques

Generally, differential boost inverter is formed by differential connection of two boost or buck-boost converters [1]–

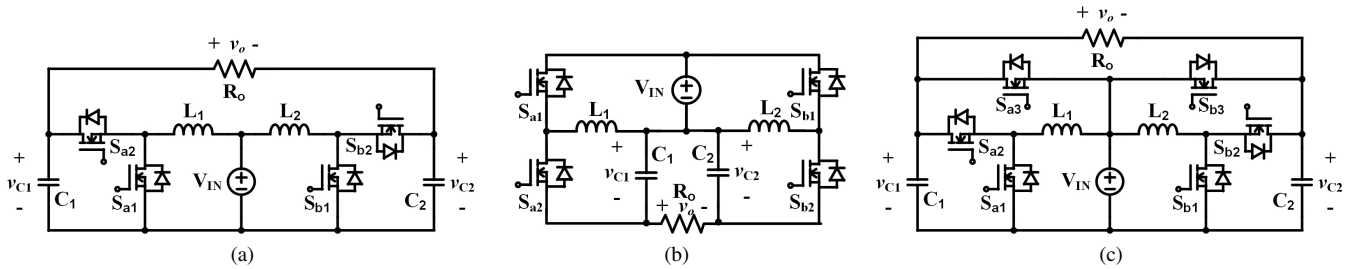

Fig. 2. Existing DBI Circuits: (a) Boost (b) Buck-Boost (c) Improved Boost

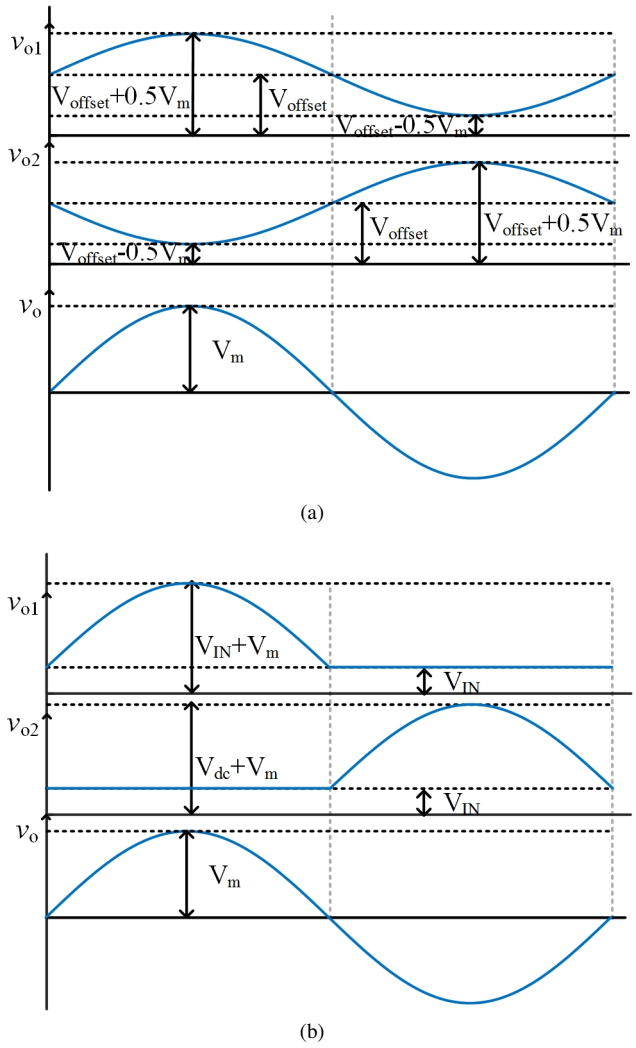

Fig. 3. Model Waveforms of DBI: (a) Conventional Full Cycle modulation (b) Half Cycle Modulation

[3] and its basic structure is depicted in Fig. 1. The output capacitor voltages of converter-1 and converter-2 are v_{o1} and v_{o2} respectively, which are connected differentially across the load to generate voltage v_o. With application of conventional full cycle modulation (FCM), these two converters generate sinusoidal waveforms of reference frequency with 180 degrees phase shift. Here, both converters operate all the time and the model waveforms for FCM are depicted in Fig. 3a. To reduce the switching losses half cycle modulation (HCM) [9] is applied to DBIs, where one of converter output voltage is clamped to input voltage V_{IN} and the converter is modulated to generate sinusoidal signal with offset voltage. Fig. 3b depicts the model waveforms for the HCM operation. In HCM operation, the inductor in clamped converter will carry the load current and causes more conduction losses. To reduce these conduction losses with HCM operation, by-pass switches are used in [9] as shown in Fig. 2c.

III. Proposed DBI Operation

The proposed differential buck-boost DBI (DBBI) with reduced switch voltage stresses is shown in Fig. 4. Converter-1 is formed by the switches S_{a1}, S_{a2} & S_{a3}, inductor L_1 and capacitor C_1. Similarly converter-2 is built by the switches S_{b1}, S_{b2} & S_{b3}, inductor L_2 and capacitor C_2. Both converters are energized by the input voltage source V_{IN} and their output voltages v_{o1} and v_{o2} are differentially connected across the load. Operation of the proposed DBBI is divided into four modes and are shown in Fig. 4b

A. Mode-a: ($0 < v_o < V_{IN}$)

In this mode, the IDBI's output voltage is accomplished by V_{IN} state and zero states. During V_{IN} state, switches S_{a1}, S_{a3}, S_{b2}, and S_{b3} are ON. Assuming negligible energy in inductors and capactiors make v_{o1} and v_{o2} to clamp at V_{IN} and zero potential respectively. The difference of these voltages makes output voltage equals to V_{IN}. For zero state operation, switches S_{a1}, S_{a3}, S_{b1}, and S_{b3} are ON and provide free wheeling path for load current. During this interval both v_{o1} and v_{o2} are equal to V_{IN} and hence, make output voltage as zero.

B. Mode-b: ($v_o > V_{IN}$)

During this mode, switches S_{a1}, S_{b2}, and S_{b3} are continuously ON while complementary switches S_{a2} and S_{a3} are operated with the modulated duty cycle to shape the capacitor voltage as sinusoidal. When S_{a2} is ON inductor L_1 will be energized and discharges when S_{a3} is ON. Turning ON of S_{b2}, and S_{b3} clamp the voltage v_{o2} to zero volts and S_{a1} conduction makes the v_{o1} to $V_{IN} + v_{c1}$ volts. Hence, the output voltage v_o will be $V_{IN} + v_{c1}$.

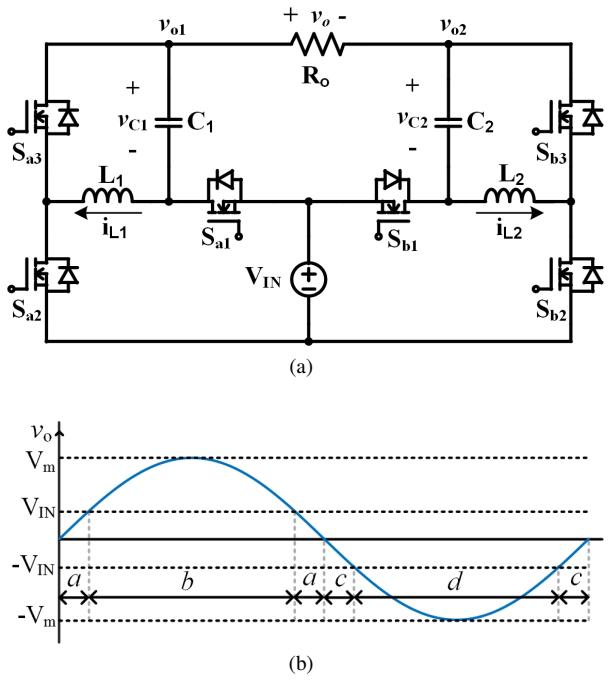

Fig. 4. Proposed IDBI (a) Schematic Diagram and (b) Key Operating Modes

C. Mode-c: ($-V_{IN} < v_o < 0$)

In this mode, the output voltage is obtained using $-V_{IN}$ state and zero states. For $-V_{IN}$ state switches switches S_{a2}, S_{a3}, S_{b1}, and S_{b3} are ON so, v_{o1} & v_{o2} clamps to zero and V_{IN} potential and generates $-V_{IN}$ at the output. Zero state operation is same as explained in Mode-a.

D. Mode-d: ($v_o < -V_{IN}$)

This mode of operation is similar to Mode-b. Here, Mode-b's converter-1 and converter-2 functionality interchanged to have zero and $(V_{IN} + v_{C2})$ volts as v_{o1} & v_{o2} voltages respectively. The difference of these voltages i.e., $-(V_{IN}+v_{C2})$ will be produced at the output.

Duty cycle of the proposed inverter for different modes are expressed as follows

For Mode-a & Mode-c: inverter operates as buck converter

$$d(t) = \frac{|v_o(t)|}{V_{IN}} \tag{1}$$

For Mode-b & Mode-d: inverter operates as boost converter

$$d(t) = 1 - \frac{V_{IN}}{|v_o(t)|} \tag{2}$$

IV. Simulation & Comparison Studies

A. Simulation

Operation of the proposed topology is examined through simulation analysis using PSIM software. A 500 W load with the following specifications: $V_{IN} = 100$ V, $V_o = 230$ V (RMS), $L_1 = L_2 = 400\mu H$, $C_1 = C_2 = 5\mu F$, $f_o = 50$ Hz, $f_{sw} = 50$ kHz is simulated. Fig. 5 depicts the load voltage, current and capacitor voltage waveforms. From these waveforms it can be noticed that the capacitor peak voltage is less than the output voltage peak. Inductor current waveforms shown in Fig. 6 confirms that their current is zero for half of the output cycle, which will reduce the inductor conduction losses. The voltage across the switches S_{a1}, S_{a2} and S_{a3} are presented in FIg. 7 where the S_{a1} blocking voltage equals to V_{IN} and remaining switches are blocking of V_m volts.

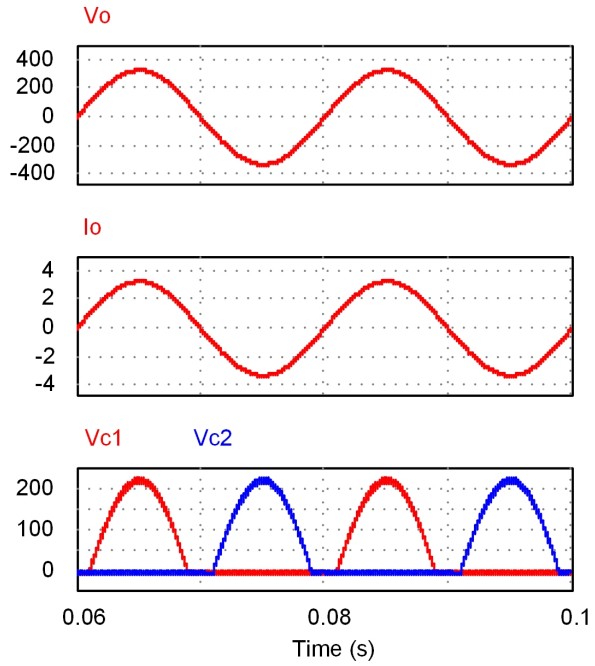

Fig. 5. Simulation results of output voltage v_o (V), output current i_o (A) and capacitor voltages v_{c1} (V) & v_{c2} (V).

TABLE I
COMPARISON OF SWITCH BLOCKING VOLTAGES

Switchies	DBI(FCM) [1]	DBI(HCM) [9]	IDBI(HCM) [9]	Proposed
S_{a1}	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	V_{IN}
S_{a2}	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	V_m
S_{a3}	—	—	V_m	V_m
S_{b1}	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	V_{IN}
S_{b2}	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	$(V_{IN}+V_m)$	V_m
S_{b3}	—	—	V_m	V_m
TSV	$(4V_{IN}+4V_m)$	$(4V_{IN}+4V_m)$	$(4V_{IN}+6V_m)$	$(2V_{IN}+4V_m)$

TABLE II
COMPARISON OF INDUCTOR CURRENTS

Switchies	DBI(FCM) [1]	DBI(HCM) [9]	IDBI(HCM) [9]	Proposed
$I_{L,Peak}$ (A)	15.80	15.9	16.69	12.41
$I_{L,RMS}$ (A)	6.94	6.59	6.30	4.62
$I_{L,Average}$ (A)	2.648	2.312	3.69	2.64

B. Comparison

To prove the improvements of proposed inverter over existing differential a comprehensive comparison is presented in

TABLE III
COST COMPARISON OF DIFFERENT DIFFERENTIAL BUCK-BOOST INVERTERS AT OUTPUT POWER (P_o)=500W, V_{IN}=100 V, V_m=325 V

Element	Part Number	Specifications	Price per Unit ($)	DBI(FCM) [1]	DBI(HCM) [9]	IDBI(HCM) [9]	Proposed
Mosfets	S1HP25N50E	500V, 26A	3.06	4	4	4	-
	S1HP25N40D	400V, 26A	2.92	-	-	2	4
	SQP25N1552	150V, 26A	1.95	-	-	-	2
Capacitors	MEP1847H55025	5uF, 500V	6.49	2	2	2	-
	C4GADUC4500AA	5uF, 250V	4.25	-	-	-	2
Inductors	AGP423474	470 uH, 12A	17	2	2	2	2
			Total Cost ($)	59.22	59.22	65.06	**58.08**

*Courtesy: www.mouser.com and prices are subject to market conditions

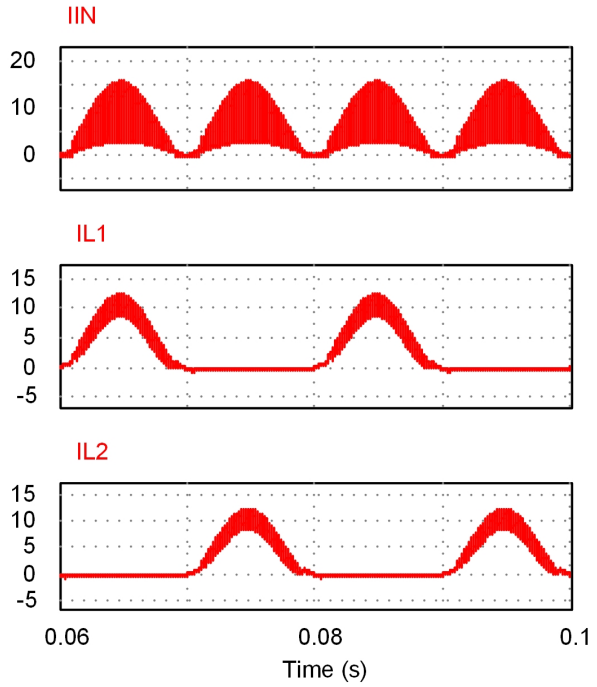

Fig. 6. Simulation results of input current i_{IN} (A) and inductor currents i_{L1} (A)& i_{L2} (A).

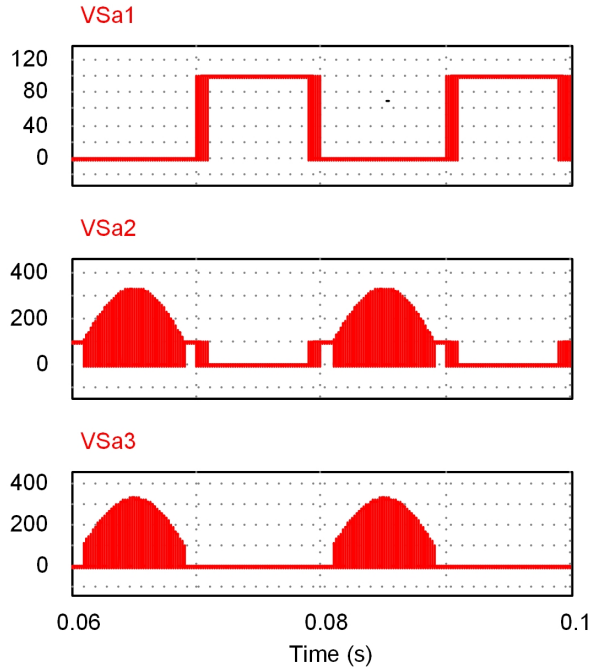

Fig. 7. Simulation results of the switch voltages v_{Sa1} (V), v_{Sa1} (V) & v_{Sa3} (V).

this section.

*1) **Switch Voltage Stresses**:* The blocking voltages of inverter switches are tabulated in the TABLE I. The proposed inverter possess lowest Total Switch Voltage (TSV) i.e., $(2V_{IN} + 4V_m)$, which helps to reduce switching losses and the switches cost.

*2) **Inductor RMS Current**:* Proposed and the remaining DBI topologies are simulated as per specification the given in earlier simulation section. The inductor currents values of each circuit are tabulated in TABLE II. Usually inductor power losses depends on their RMS current values. Here, the proposed inverter have lesser RMS inductor current compared to other topologies hence, efficiency will be improved.

*3) **Efficiency**:* Losses of proposed converter are evaluated by using PSIM thermal model and the loss distribution is presented in Fig. 8 The efficiency of the proposed topology

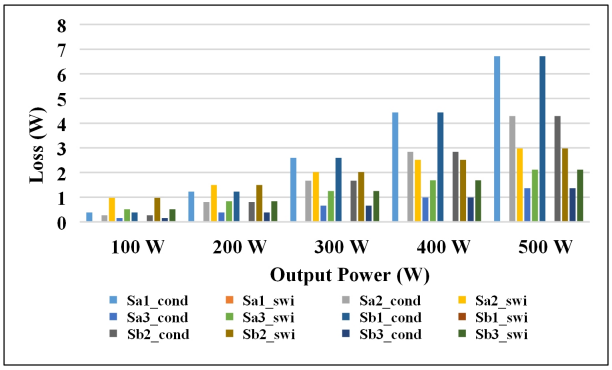

Fig. 8. Loss distribution of switches in the proposed topology with respect to the load

compared with the other BBIs and the respective graphs are

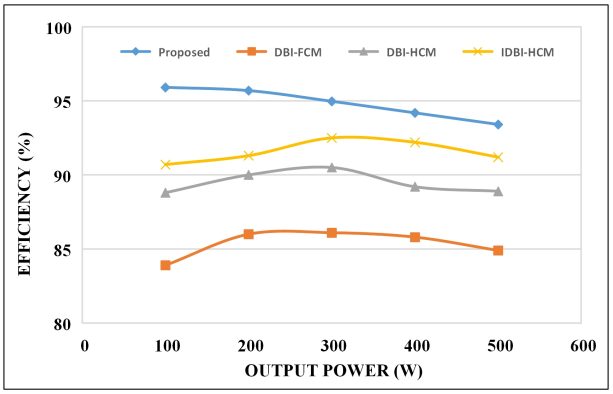

Fig. 9. Comparison of proposed topology efficiency with the other BBIs

plotted in Fig. 9, which confirms the improvement in efficiency with the proposed topology.

*4) **Capacitor Size & Cost**:* Generally, the cost and size of the capacitor depends upon its capacitance and voltage ratings. With the same capacitance value the proposed topology needs a lower voltage rating capacitor. So, the size and cost of the total inverter will be reduced.

The comprehensive cost comparison of the proposed topology with different buck-boost inverters is carried to show its cost effectiveness. The cost comparison data is furnished in TABLE III. which confirms that the proposed topology, even with six switches, is economical than the BBIs [1], [9] with four switches

V. Conclusion

In this paper, new cost effective differential buck-boost inverter is presented. Its detailed operation is explained and comprehensive comparative study with existing DBIs is presented. The proposed inverter provided less TSV, low inductor RMS currents, improved efficiency and utilized small size capacitors.

Acknowledgment

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