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Single-stage electrolytic capacitor less non-inverting buck-boost PFC based AC–DC ripple free LED driver

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Abstract: This study proposes electrolytic capacitor (EC) less power factor correction (PFC) light emitting diode (LED) driver with reduced current ripple. Generally PFC LED drivers need massive ECs to diminish output current ripple. The life-span of LED driver significantly reduces due to short life-span of ECs, and hence demands for EC-less LED drivers. The proposed LED driver is composed of non-inverting buck-boost PFC converter and bi-directional converter (BDC) for ripple current cancellation which replace the short-life ECs with long-life film capacitors. The PFC converter is designed with discontinuous conduction mode in order to ensure unity power factor operation. The role of BDC is to absorb second harmonic ac ripple current of PFC converter and allow the dc current to LED load. In addition, the desired BDC output voltage (v_{cbc}) is higher than the PFC output voltage (V_{LED}) irrespective of ac source voltage, hence, simplifies the control complexity. Theoretical analysis and predictions of the system have been validated using MATLAB/Simulink simulation, and experimentally validated with a prototype of 7 W. The results evident that PFC integrated BDC provide reduced ripple current with film capacitor as compared with EC counterpart and hence increase the life-span of LED driver.

1 Introduction

Globally one fifth consumption of electricity in lighting system demands for energy efficient lighting sources [1]. With rapid advancement in semiconductor technology, light emitting diodes (LEDs) are gaining more popular than conventional lighting systems. The advantages of LEDs over conventional lighting systems are high luminous efficacy, long-life, lesser power consumption, compact size and environmental friendly etc. [2, 3]. A direct ac-grid fed LED lighting system involves ac–dc power converter with power factor correction (PFC) to attain near unity power factor (UPF) with less total harmonic distortion (THD).

In literature several types of PFC based LED drivers such as single-stage, two-stage etc., are reported. Two stage PFC LED drivers are used for medium power applications. The first stage is to achieve UPF, whereas second stage is to maintain desired voltage regulation. However, two stage drivers suffers from several demerits such as bulky, lesser efficiency, high cost and require two control circuits [4]. These drawbacks can be overcome by use of single-stage drivers, where in which both PFC stage and dc–dc stage is merged into single stage to achieve compact size with desired power factor (PF). Further, single-stage PFC based LED drivers using various converter topologies have been addressed [5–8]. Among all topologies the buck converter is cheapest converter but it serves only when output voltage is less than ac source voltage. The negative input current would occur when the rectified input voltage is less than output voltage. This is not allowed because the rectifier will block negative current. As a result the input current is zero near zero crossing point of line voltage; it exhibits more distortions of ac source current and electromagnetic interference problems [5–8]. Therefore, this converter is not good for PFC applications. Although, the boost converter is a best choice for PFC applications due to its source side inductor, but still it suffers from higher device voltage stress for universal input applications. Moreover, as a consequence of higher boost voltage, more number of LEDs needs to be connected in series, which lead to higher driver cost [6]. Flyback converter is a good choice for low power applications due to its less component count and inherent device protection with isolation. However, transformer design is complex and its leakage inductance leads to ringing oscillation. Cuk, SEPIC and Zeta converters have more number of storage devices, which increases the size of driver [7]. A classical buck-boost converter works in step-up/step-down mode and capable of giving high PF is a better choice for low and medium power applications and hence, able to fulfil most of the LED driver specifications. However, it suffers from various drawbacks such as high switching stress due to inverted output, need of isolated gate driver circuit, independent grounding of source side and load side [8]. These drawbacks can be overcome by the proposed non-inverting buck-boost (NIBB) converter. Generally, LED driver requires bulky electrolytic capacitors (ECs) to balance the dc output power and instantaneous input power. The life-span of ECs ranges from 5000 to 10,000 hours (1/10th of LED life-span) and it leads to reduction in overall life-span of LED drivers [9, 10]. In order to improve the life-span of drivers, EC-less LED drivers are essential [11]. In consequence, several techniques to eliminate ECs are reported [12–22]. EC-less LED driver is implemented by replacing EC with magnetic storage device [12, 13]. However, the storage device is associated with various drawbacks such as less energy density, reduction in efficiency due to core and winding resistance loss [22]. Another method is by reducing the power imbalance to be handled by ECs between ac input and dc output [14]. Few authors have addressed third and fifth harmonic injecting techniques to eliminate ECs and minimise peak to average ratio [15–17]. However, by injecting third and fifth hormonics component into source current results in reduced PF and high THD and significant flickering effect in LED light due to second harmonic ripple [15, 16]. Moreover, the additional control circuit is required to generate third and fifth harmonics. Thus, it increases the overall driver cost and complexity of control circuit which needs to be further investigate. A pulsating current driver technique is presented to reduce the EC size [18]. However, all these methods eliminate ECs with the penalty of poor PF. In [19–21] the bi-directional converter (BDC) is connected in parallel with PFC converter to absorb the second harmonic ripple, whereas BDC is operated with feed forward closed loop control which increases the control complexity. This paper proposes ripple-free LED driver using EC-less NIBB PFC

integrated BDC. The proposed driver provides various advantages such as improved PF, lesser THD, ripple free LED current, compact size and increased life-span due to elimination of EC and simple BDC control because of its fixed duty operation. Section 2 presents operation and design of proposed converter with an introduction from Section 1. Section 3 presents operation and design of proposed EC-less LED driver. Finally, Section 4 presents simulation, result analysis and performance comparisons of various parameters of the proposed system.

2 Operation and design of NIBB PFC converter

In the operation and design of NIBB PFC converter, the circuit elements are considered as ideal.

2.1 Principle of operation

The PFC LED driver consists of uncontrolled rectifier followed by PFC converter. Figs. 1*a–c* illustrates the NIBB PFC converter, EC-less PFC integrated BDC for ripple cancellation and their theoretical waveforms, respectively. The PFC converter is designed with discontinuous conduction mode (DCM) to ensure UPF with low THD. When the switches ($Q_{\rm pfc}$ & $Q_{\rm pfc}$) are turned-ON simultaneously, the PFC inductor ($L_{\rm pfc}$) gets charged from the dc-link voltage ($v_{\rm in}$), while the charged capacitor ($C_{\rm o}$) alone supplies power to the LED load. When the switches ($Q_{\rm pfc}$ & $Q'_{\rm pfc}$) are turned-OFF, the diodes ($D_{\rm pfc}$ & $D_{\rm pfc}$) get forward biased and hence, the energy stored in $L_{\rm pfc}$ will helps to charge $C_{\rm o}$ and also, supplies power to the load. When $L_{\rm pfc}$ is completely demagnetised both the diodes get reverse biased, while $Q_{\rm pfc}$ & $Q'_{\rm pfc}$ are already in turn-OFF position and inductor voltage ($v_{L_{\rm pfc}}$) becomes zero and hence operates in DCM. During this DCM interval the charged $C_{\rm o}$ alone supplies power to LED load until next switching cycle begins. This topology is considered as indirect energy transfer converter because its source is not connecting directly to the load. Thus, it prevents the load from any source faults and vice-versa.

2.2 Design considerations for DCM

When both the switches are turned-ON for time DT, the change in inductor current is given by

$$\Delta i_{L(+)} = \frac{v_{\rm in}}{L_{\rm pfc}} DT \tag{1}$$

When the switches are turned-OFF at $t = DT$, diodes become forward bias for time duration of D_1T.

The change in inductor current is given by

$$\Delta i_{L(-)} = \frac{-V_{\rm LED}}{L_{\rm pfc}} D_1 T \tag{2}$$

At $t = D_1T$ inductor energy resets to zero and hence diodes become reverse bias. During the DCM interval of $(1 - D - D_1)T$, all the switching devices are turned-OFF, hence charged $C_{\rm o}$ alone will supply power to the load. The current through inductor during DCM operation is zero and is given by

$$\Delta i_{L(0)} = 0 \tag{3}$$

Under steady-state operation, net change in inductor current over a cycle period is zero and is given by

$$\frac{v_{\rm in}}{L_{\rm pfc}} DT + \frac{(-V_{\rm LED})}{L_{\rm pfc}} D_1 T + 0 = 0 \tag{4}$$

By solving (4), the dc gain of NIBB converter is obtained as

$$M = \frac{V_{\rm LED}}{v_{\rm in}} = \frac{D}{D_1} \tag{5}$$

From the $i_{\rm d}$ waveform shown in Fig. 1*c*, the average diode current is equal to average output current and is given by

$$I_{\rm LED} = \frac{V_{\rm LED}}{R} = \frac{1}{T}\left[\frac{i_{Lpk}}{2} D_1 T\right] \tag{6}$$

From (6), average load voltage is given by

$$V_{\rm LED} = \frac{v_{\rm in} D D_1 R}{2 L_{\rm pfc} f_{\rm spfc}} \tag{7}$$

By equating (5) and (7)

$$D_1 = \sqrt{\frac{2L_{\rm pfc}}{RT}} \tag{8}$$

where,

$$R = \frac{V_{\rm LED}}{I_{\rm LED}} \tag{9}$$

From the waveform shown in Fig. 1*c*, the maximum switch current ($i_{\rm swm}$) and maximum diode currents ($i_{\rm dm}$) can be calculated as follows

$$i_{\rm swm} = i_{Lpk} = \frac{v_{\rm in}}{L_{\rm pfc}} DT \tag{10}$$

$$i_{\rm dm} = i_{Lpk} = \frac{V_{\rm LED}}{L_{\rm pfc}} D_1 T \tag{11}$$

Assuming boundary condition, the critical inductor value is given by

$$L_{\rm pfc\,(crit)} = \frac{V_{\rm LED}(1 - D)}{2 f_{\rm spfc} I_{\rm LED}} \tag{12}$$

For DCM operation, the value of $L_{\rm pfc}$ must be less than the $L_{\rm pfc(crit)}$ value.

The output filter $C_{\rm o}$ value must be adequate enough to provide tolerable ripple output voltage and to supply continuous output load.

$$C_{\rm o} = \frac{I_{\rm LED} D}{\Delta v_{\rm co} f_{\rm spfc}} \tag{13}$$

where, $\Delta v_{\rm co}$ – output ripple voltage, $V_{\rm LED}$ – voltage across LED load, $f_{\rm spfc}$ – switching frequency of PFC converter, M – dc-gain of NIBB converter, $C_{\rm o}$ – output filter capacitor, $v_{\rm in}$ – dc-link voltage, i_{Lpk} – peak current of $L_{\rm pfc}$, and D – duty ratio of PFC converter. R – Equivalent output resistance of LED load. Filter capacitor ($C_{\rm o}$) is designed to achieve a ripple voltage $\Delta v_{\rm co}$ of 5% with a switching frequency of 20 kHz.

3 Operation and design of proposed EC-less LED driver

Fig. 1*b* illustrates the proposed EC-less LED driver schematic, which composed of NIBB PFC converter and BDC topology for ripple absorption. The inductor ($L_{\rm o}$) is to provide desired ripple free current to the load. In order to achieve ripple free output voltage, film capacitors are used instead of bulky ECs which results in increased life-span of PFC LED drivers. Fig. 2 depicts the key waveforms of proposed EC-less LED driver.

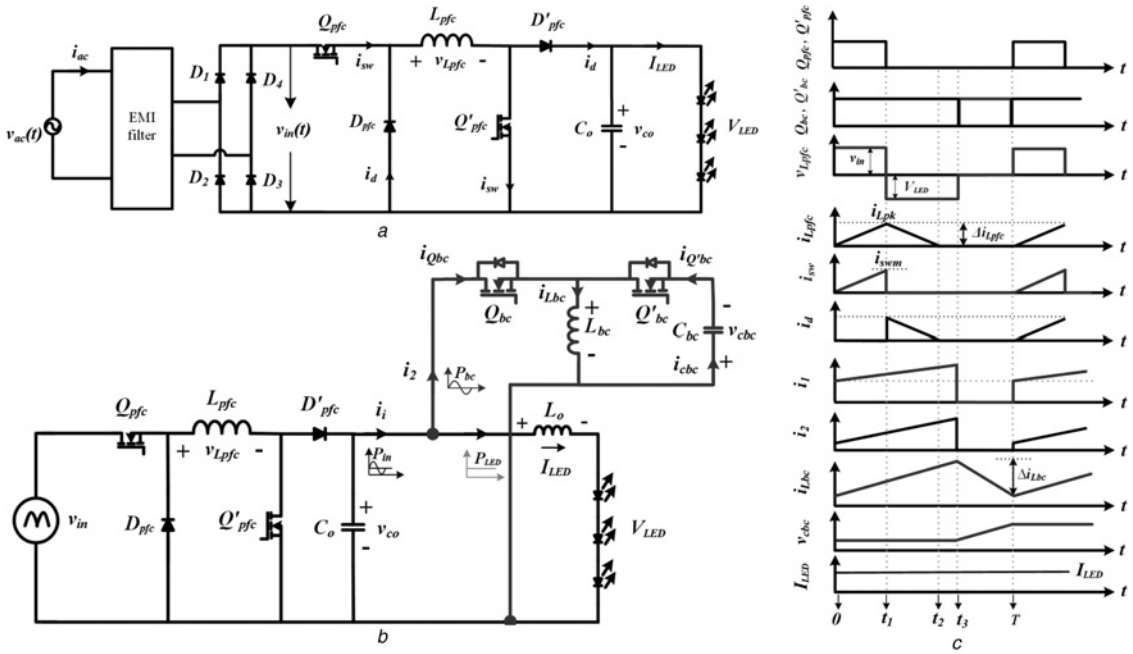

Fig. 1 *Proposed converter circuits*

a NIBB PFC converter
b PFC integrated BDC
c Theoretical waveforms

The instantaneous source voltage v_{ac} (t) and source current i_{ac} (t) are given by

$$v_{ac}(t) = V_m \sin \omega t \tag{14}$$

$$i_{ac}(t) = I_m \sin \omega t \tag{15}$$

For UPF operation, the source current is in-phase with source voltage. From (14) and (15), the instantaneous input power is represented by

$$p_{in}(t) = v_{ac}(t) i_{ac}(t) = P_{in} - P_{in} \cos 2\omega t \tag{16}$$

Assuming zero power loss in PFC converter, the average input power

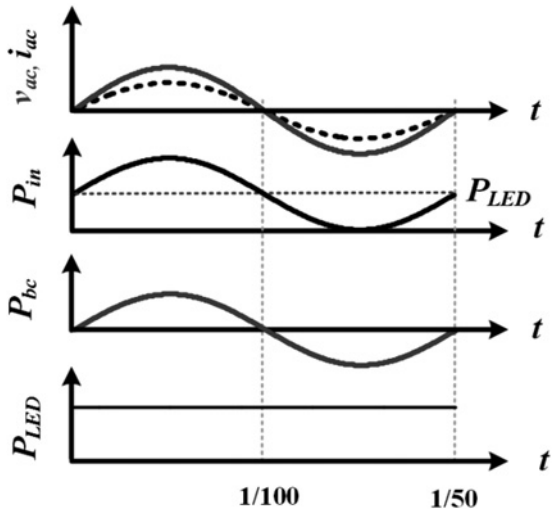

Fig. 2 *Key waveforms of proposed EC-less LED driver*

can be calculated as

$$P_{in} = \frac{V_m I_m}{2} = P_{LED} \tag{17}$$

where V_m – peak value of source voltage, I_m – peak value of source current, $p_{in}(t)$ – instantaneous input power, P_{in} – average input power, P_{LED} – output power and ω – angular frequency of input supply $\omega = 2\pi/T_{line}$. Assuming larger value of L_o, its current is considered as constant. This means the voltage across capacitor C_o is same as voltage across LED load. The instantaneous input power is same as output power.

$$i_1 = \frac{P_{LED}}{V_{LED}} = \frac{p_{in}(t)}{V_{LED}} = \frac{P_{in}}{V_{LED}} - \frac{P_{in}}{V_{LED}} \cos 2\omega t \tag{18}$$

The current i_1 has two components, one is ac component with twice the line frequency, and another one is dc component I_{LED} as illustrated in (18). The direct feeding of i_1 to LED load leads to flickering which reduces the efficacy and life-span of LED. The proposed BDC topology has been used to bypass the ac component with twice the line frequency from i_1 and hence eliminates the load flickering.

3.1 Operation of proposed LED driver

This section explains modes of operation of proposed LED driver. Fig. 3 shows the equivalent circuits of proposed LED driver in each mode of operation. From the theoretical waveforms shown in Fig. 1*c*, the operation of proposed driver is categorised into four modes under the condition $P_{in} > P_{LED}$. The operation under the condition $P_{in} < P_{LED}$ is similar to $P_{in} > P_{LED}$ except that the current $i_{L_{bc}}$ flows in reverse direction.

Mode-1: $[0 \simeq t_1]$

In mode-1 operation, switches Q_{pfc}, Q'_{pfc} and Q_{bc} are turned-ON at instant $t = 0$. The inductor L_{pfc} is energised from dc-link voltage,

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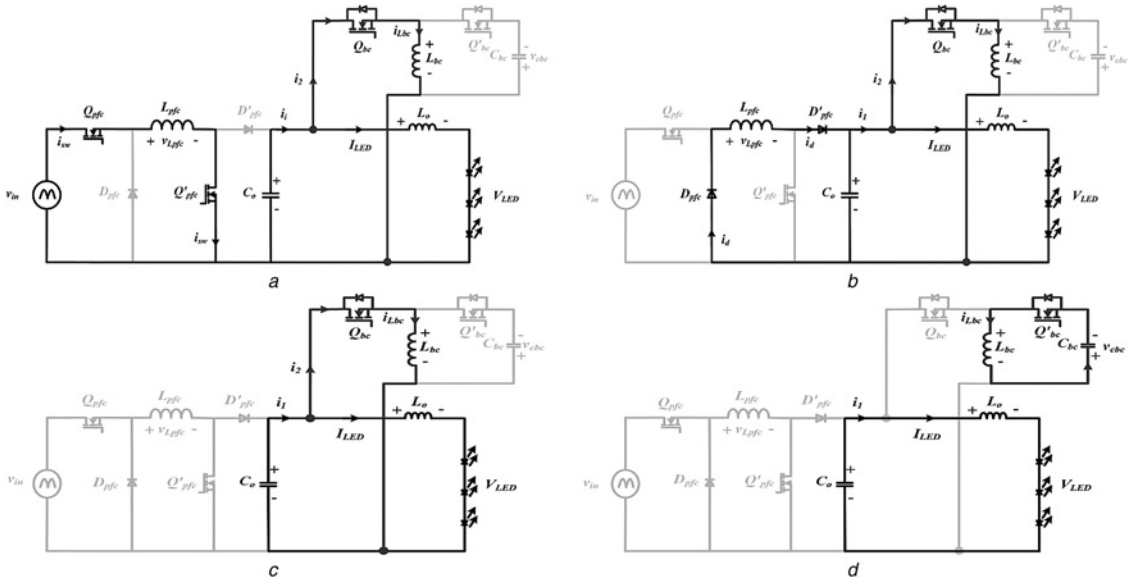

Fig. 3 *Equivalent circuits of different modes of proposed LED driver*

a Mode-1
b Mode-2
c Mode-3
d Mode-4

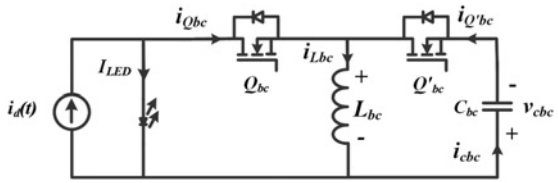

Fig. 4 *Equivalent circuit of BDC topology*

while C_o delivers energy to L_{bc} and LED load. This mode ends at $t = t_1$. The equivalent circuit of mode-1 is shown in Fig. 3*a*.

Mode-2: $[t_1 \simeq t_2]$

At the instant $t = t_1$, the switches (Q_{pfc}, Q'_{pfc}) OFF and the switch Q_{bc} remains ON and Q'_{bc} remains OFF, and diodes (D_{pfc}, D'_{pfc}) become forward biased. Stored energy in the L_{pfc} delivers to charge the capacitor C_o, energise the inductor L_{bc} and power the LED load. The mode-2 ends at the instant $t = t_2$ and the L_{pfc} is fully discharged. Fig. 3*b* depicts the equivalent circuit of mode-2.

Mode-3: $[t_2 \simeq t_3]$

Table 1 Specifications of proposed EC-less LED driver

Parameter description		Value/model no.
source voltage (v_{ac})		30–90 V_{rms}
supply frequency (f_{line})		50 Hz
output power (P_{LED})		7 W
output voltage (V_{LED})		40 V
output current (I_{LED})		175mA
rectifier diodes (D_1, D_2, D_3 & D_4)		MUR 160 (4)
MOSFETs	Q_{pfc}, Q'_{pfc}	IRFP264N, IRF540N
	Q_{bc}, Q'_{bc}	SiHG20N50C (2)
diodes (D_{pfc}, D'_{pfc})		BVY29 (2)
switching frequency	f_{spfc}	20 kHz
	f_{sbc}	58 kHz
inductors	L_{pfc}, L_{bc}	300 µH, 2.2 mH
	L_o (output filter)	2 mH
capacitors	C_o, C_{bc}	6.6 µF, 13.2 µF
pulse generation		TL 494 PWM IC FPGA processor
driver ICs		IR2110 (2)

The equivalent circuit of mode-3 is shown in Fig. 3*c*. In mode-3 operation, Q_{bc} is still remains ON and L_{pfc} is in zero energy state. The capacitor C_o supply energy to L_{bc} and LED load. The mode-3 operation ends at instant $t = t_3$ when Q_{bc} is turned-OFF and Q'_{bc} is turned-ON.

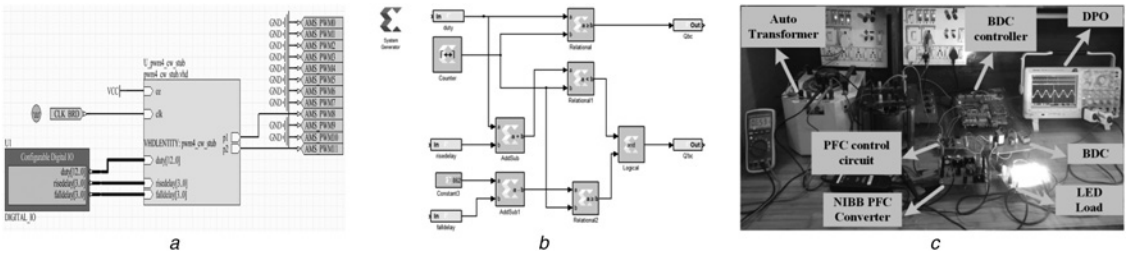

Fig. 5 *BDC control circuit implementation*

a Altium designer schematic view
b Control logic using XILINK blocksets in MATLAB
c Experimental setup of proposed LED driver

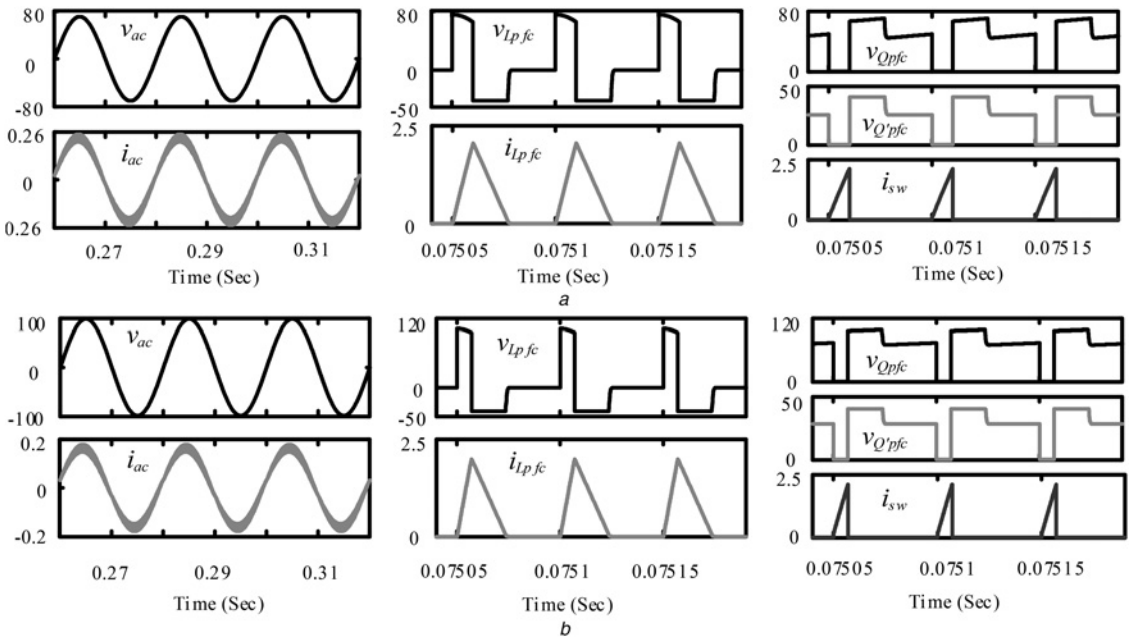

Fig. 6 *Simulation waveforms of PFC converter at ac source voltage of*

a $V = 50\ V_{rms}$
b $V = 70\ V_{rms}$

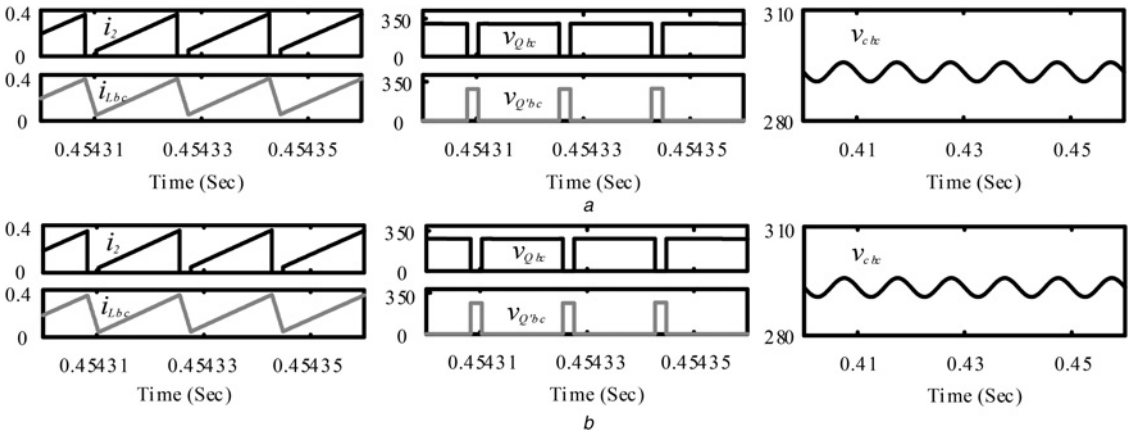

Fig. 7 *Simulation waveforms of BDC at ac source voltage of*

a $V = 50\ V_{rms}$
b $V = 70\ V_{rms}$

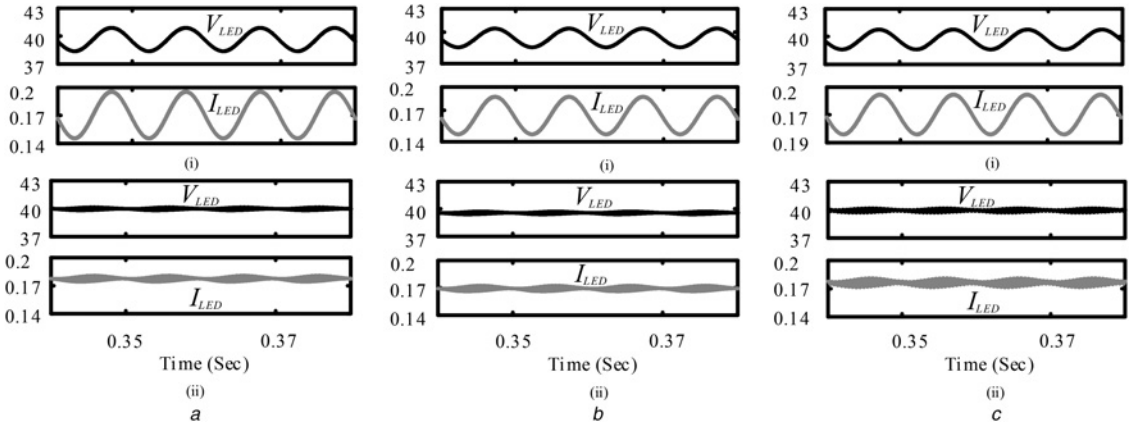

Fig. 8 *Simulation waveforms of V_{LED}, I_{LED} of PFC converter (i) without BDC and (ii) with BDC topology at v_{ac} of*

a $V = 50\ V_{rms}$
b $V = 70\ V_{rms}$
c $V = 110\ V_{rms}$

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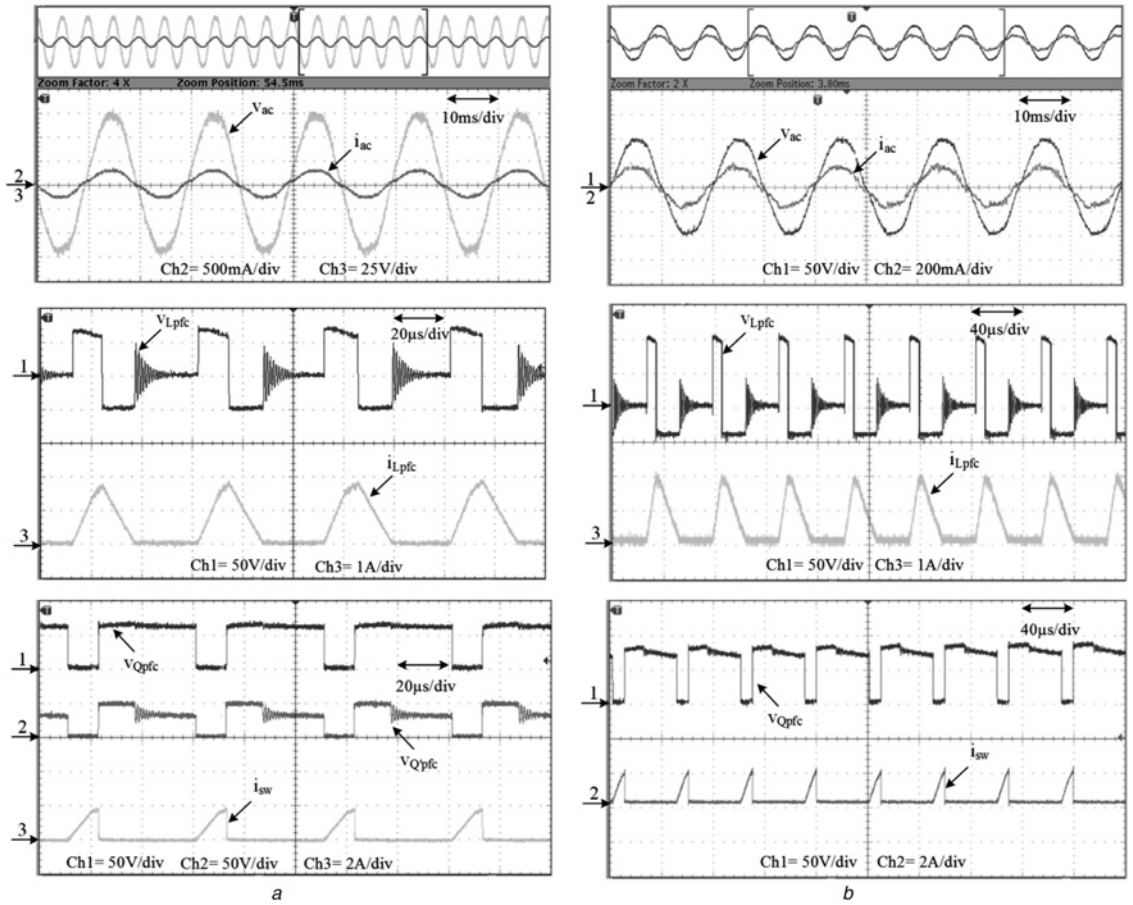

Fig. 9 *Experimental waveforms of PFC converter*

a $V = 50\ V_{rms}$
b $V = 70\ V_{rms}$

Mode-4: $[t_3 \simeq T]$

The equivalent circuit of mode-4 is shown in Fig. 3*d*. Mode-4 starts at instant $t = t_3$ by turning-OFF Q_{bc} and turning-ON Q'_{bc}. Energy stored in L_{bc} will be discharged to C_{bc}, while C_o alone supplies power to LED load. The mode-4 operation ends by turning-OFF Q'_{bc} at time $t = T$ and next switching cycle begins with mode-1 operation.

3.2 Design of BDC topology

The steady-state analysis of BDC has been made by neglecting dc component. Whereas, filter components L_o and C_o are considered as short circuit and open circuit, respectively. Fig. 4 shows the equivalent circuit of BDC.

Due to the role of PFC, the double line frequency ac component of diode current i_d (t) can be expressed as follows

$$i_d(t) = I_{LED} \sin(2wt) \tag{19}$$

The current i_d will flow only through the switch Q_{bc} by deviating the path from LED load. Consequently, current ripple component with twice the line frequency is absorbed by BDC topology. The switch current $i_{Q_{bc}}$ and $i_{Q'_{bc}}$ can be expressed as

$$i_{Q_{bc}} = i_d(t) = D_{bc} i_{L_{bc}} = I_{LED} \sin(2\omega t) \tag{20}$$

$$i_{Q'_{bc}} = (1 - D_{bc}) i_{L_{bc}} \tag{21}$$

From (20) $i_{L_{bc}}$ can be written as

$$i_{L_{bc}} = \frac{1}{D_{bc}} I_{LED} \sin(2\omega t) \tag{22}$$

From (21)

$$i_{Q'_{bc}} = \frac{1 - D_{bc}}{D_{bc}} I_{LED} \sin(2\omega t) \tag{23}$$

The voltage across C_{bc} is expressed as follows

$$\begin{aligned} v_{cbc}(t) &= \frac{1}{C_{bc}} \int_{t=0}^{t=T} i_{cbc}(t)\, dt \\ &= \frac{1}{2\omega C_{bc}} \frac{1 - D_{bc}}{D_{bc}} I_{LED}(-\cos(2\omega t)) \end{aligned} \tag{24}$$

The current flowing through L_{bc} can be derived as follows.

$$\begin{aligned} i_{L_{bc}}(t) &= \frac{1}{L_{bc}} \int_{0}^{t=T} v_{L_{bc}}\, dt \\ &= \frac{1}{4\omega^2 L_{bc} C_{bc}} \frac{(1 - D_{bc})^2}{D_{bc}} \sin(2\omega t) \end{aligned} \tag{25}$$

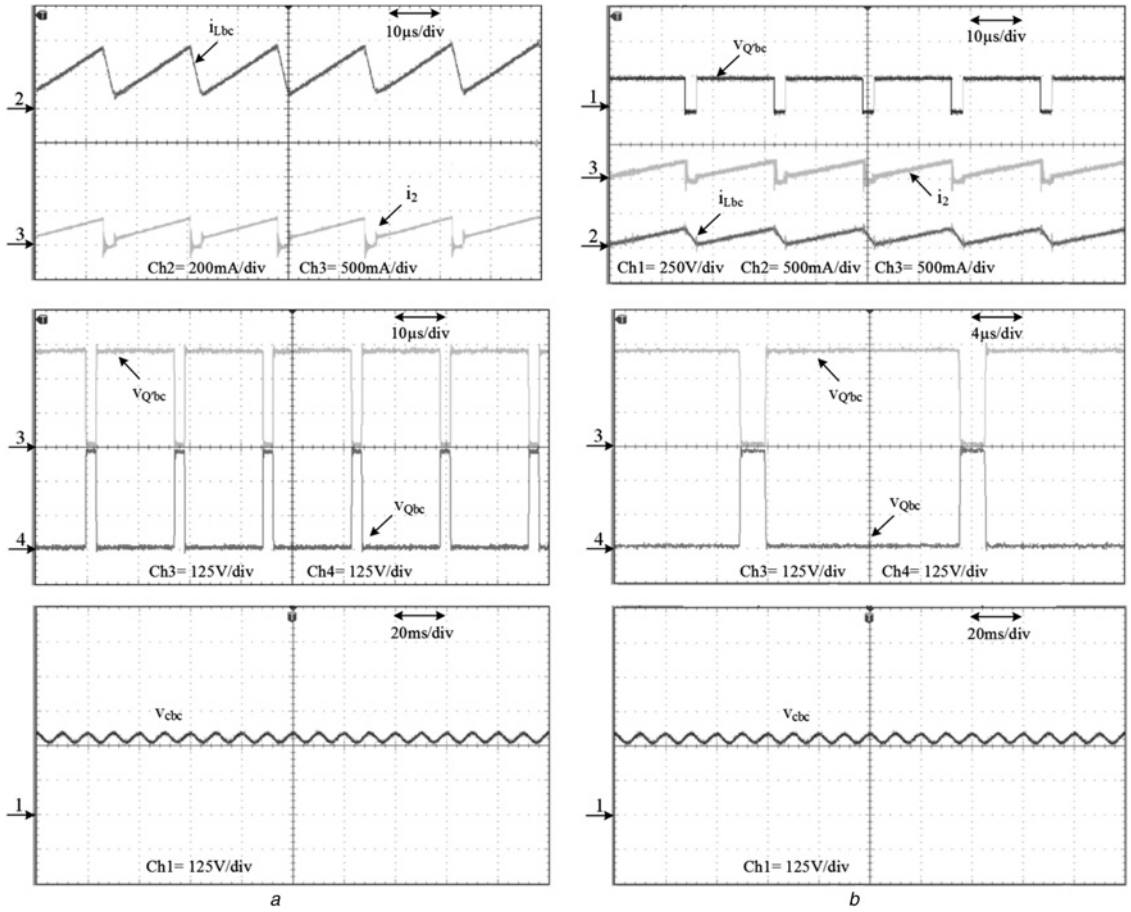

Fig. 10 *Experimental waveforms of BDC at ac source voltage of*
a $V = 50\ V_{rms}$
b $V = 70\ V_{rms}$

By solving (22) and (25), the duty ratio D_{bc} is given by

$$(1 - D_{bc})^2 = 4\omega^2 L_{bc} C_{bc}$$
$$D_{bc} = 1 - 2\omega\sqrt{L_{bc} C_{bc}} \tag{26}$$

where, D_{bc} is duty cycle of BDC.

The inductor L_{bc} is designed for CCM operation with a switching frequency of 58 kHz. The dc-gain of BDC converter can also be expressed as,

$$v_{cbc} = \frac{-D_{bc}}{1 - D_{bc}} v_{co} \Rightarrow D_{bc} = \frac{v_{cbc}}{v_{cbc} - v_{co}} \tag{27}$$

where, v_{cbc} – output voltage of BDC, and v_{co} – input voltage of BDC.

When switch Q_{bc} is turned-ON and Q_{bc} is turned-OFF, voltage across the inductor L_{bc} is given by

$$v_{L_{bc}} = L_{bc} \frac{di_{L_{bc}}}{dt} = v_{co} \tag{28}$$

By solving (27) and (28), the L_{bc} can be obtained as

$$L_{bc} = \frac{v_{co} v_{cbc} T_{sbc}}{\Delta i_{L_{bc}} (v_{cbc} - v_{co})} = \frac{v_{co} v_{cbc}}{\Delta i_{L_{bc}} (v_{cbc} - v_{co}) f_{sbc}} \tag{29}$$

where, $f_{sbc} = 1/T_{sbc}$ is switching frequency of BDC converter.

The BDC control technique is implemented using Altium Nanoboard with FPGA Spartan 3AN. Altium designer software is used to build control logic and interface between PC and board as shown in Fig. 5*a*. Fig. 5*b* depicts the schematic of control circuit developed using XILINK blocksets in MATLAB to realise the BDC pulses. The experimental setup of proposed LED drivers is depicted in Fig. 5*c*.

4 Simulation and results analysis of proposed system

The proposed EC-less LED driver has been simulated and validated experimentally. Table 1 describe the major specifications used in prototype of proposed EC-less LED driver.

4.1 Simulation results

Performance analysis of proposed LED driver has been made with EC and without EC using Matlab/Simulink simulation. The operation of NIBB PFC is studied and analysed. Figs. 6*a* and *b* shows the simulation waveforms of PFC converters (source voltage (v_{ac}), source current (i_{ac}), inductor voltage ($v_{L_{pfc}}$), inductor current ($i_{L_{pfc}}$), switch voltages ($v_{Q_{pfc}}$, $v_{Q'_{pfc}}$), switch current (i_{sw}) at input source voltage of 50 and 70 V, respectively. It can be observed from Fig. 6, that the current i_{ac} is sinusoidal with a PF of 0.998 and THD of 3.74%. The simulation waveforms ($v_{L_{pfc}}$, $i_{L_{pfc}}$) shown in Fig. 6 evident that the desired DCM operation of PFC converter. Figs. 7*a* and *b* depicts the simulation waveforms of BDC with source voltages of 50 and 70 V, respectively. Figs. 8*a*–*c* illustrates the output load waveforms (V_{LED} & I_{LED}) of PFC converter without BDC and with BDC for source voltages of 50, 70 and 110 V, respectively.

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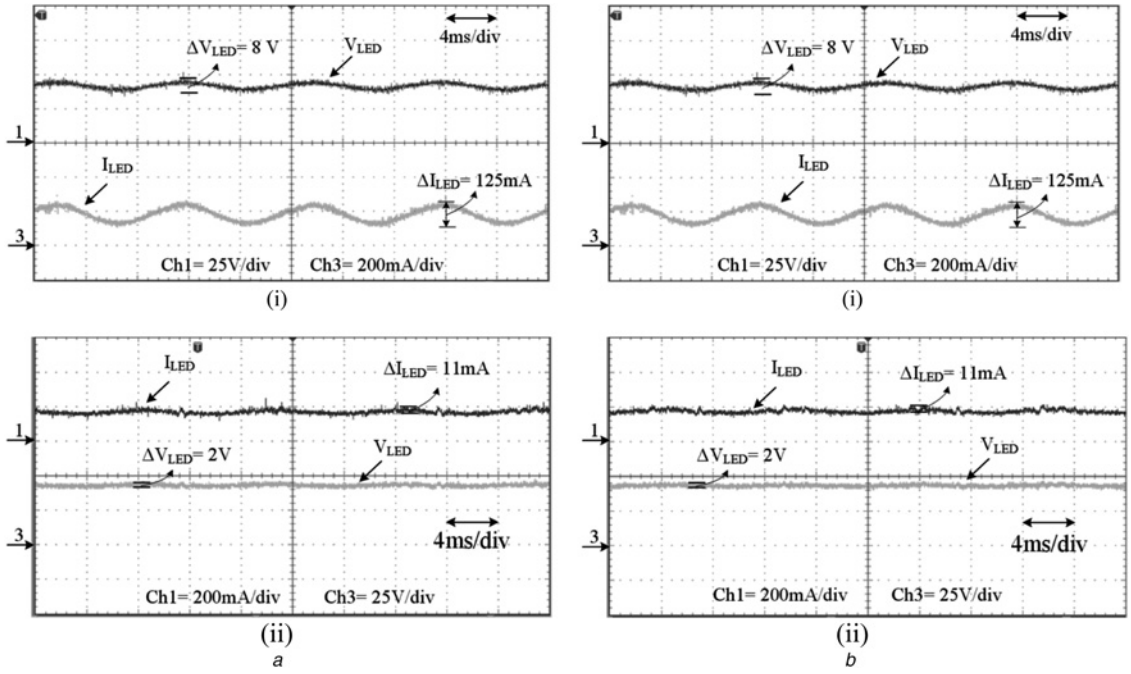

Fig. 11 *Experimental waveforms of V_{LED}, I_{LED} of PFC converter (i) without BDC and (ii) with BDC topology at v_{ac} of*

a $V = 50\ V_{rms}$
b $V = 70\ V_{rms}$

4.2 Experimental results

To validate the theoretical design and analysis predictions, a prototype of proposed LED driver is built and tested. The circuit components used for hardware implementation is provided in Table 1. The low-cost analogue IC TL494 is used to generate switching pulses for hardware implementation of PFC converter. The PWM switching pulses are realised by using FPGA processor for hardware implementation of BDC. The converter is designed for an output power of 7 W with load voltage of 40 V and current of 175 mA.

Figs. 9–11 illustrates the experimental results of various parameters for ac source voltages of 50 and 70 V. Figs. 9*a* and *b* shows the experimental waveforms of PFC converters v_{ac}, i_{ac}, $v_{L_{pfc}}$, $i_{L_{pfc}}$, $v_{Q_{pfc}}$, $v_{Q'_{pfc}}$, and i_{sw} at ac source voltage of 50 and 70 V, respectively. It can be observed from Fig. 9, that the source current is sinusoidal with a PF of 0.989. The waveforms ($v_{L_{pfc}}$, $i_{L_{pfc}}$) shown in Fig. 9

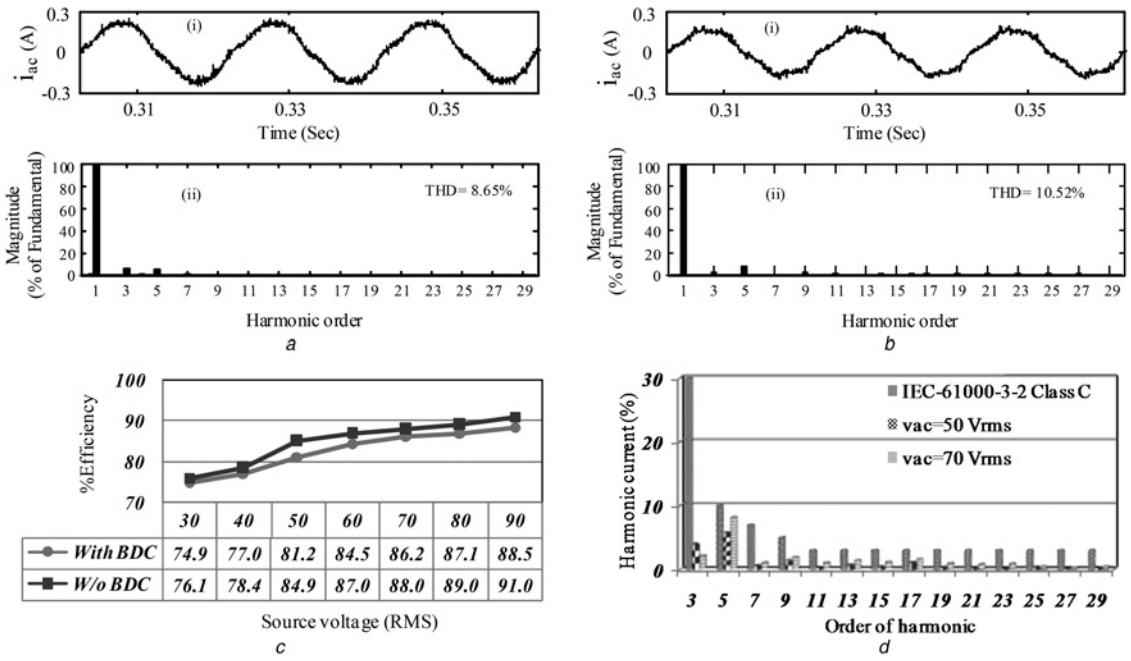

Fig. 12 *Experimental waveform of i_{ac} and its harmonic spectrum analysis at ac source voltage of*

a $V = 50\ V_{rms}$
b $V = 70\ V_{rms}$
c Efficiency against source voltage
d Measured input current harmonics

evident that the desired DCM operation of PFC converter. Figs. 10*a* and *b* depicts the waveforms of BDC converter at ac source voltages of 50 and 70 V, respectively. Figs. 11*a* and *b* illustrate the output load waveforms (V_{LED} & I_{LED}) of PFC converter without BDC and EC-less PFC integrated BDC at ac source voltage of 50 and 70 V, respectively. It can be observed from Fig. 11, that the ripple voltage and current of PFC converter without BDC is 8 V and 125 mA, respectively. Moreover, from Fig. 11 it can be clearly seen that the ripple frequency of V_{LED} and I_{LED} of PFC converter without BDC is twice the line frequency. In consequence, the waveforms shown in Fig. 11 evident that the significant reduction in ripple current and ripple voltage with the proposed EC-less BDC ripple absorption concept. Moreover, from the waveforms shown in Fig. 11, it can be observed that the effective absorption of the 100 Hz ac ripple component by the BDC topology. The measured ripple current and ripple voltage from Fig. 11 is 11 mA and 2 V, respectively. In addition, replacement of EC with the film capacitor results in significant size reduction (i.e. both in volume and its value) and hence increased life-span of the LED driver. Therefore, as compared with the benefits claimed in [15, 16], the proposed LED driver results in additional benefits such as; reduced ripple output voltage and current, high PF, less THD and reduced LED flickering effect. It is evident from the analysis that both simulation and prototype result are in close agreement with each other.

Figs. 12*a* and *b* depicts the experimental waveforms and THD spectrums of i_{ac} at 50 and 70 V_{rms}, respectively. It is evident from Figs. 12*a* and *b* that the source current THD is well below the IEC-61000 class C limits. Fig. 12*c* demonstrates the efficiency of PFC converter without BDC and EC-less PFC integrated BDC LED driver as a function of ac source voltage. It can be observed from Fig. 12*c*, that the efficiency of NIBB PFC based LED driver without BDC is 88% and proposed EC-less PFC based LED driver with BDC is 86.20% at v_{ac} of 70 V. Fig. 12*d* shows the comparison of measured harmonic spectrum of proposed system with IEC-61000 class C limits. From Fig. 12*d*, it confirms that the source current harmonics of proposed LED driver is well below IEC-61000 class C limits.

5 Conclusion

In this paper, EC-less LED driver is designed and analysed in detail. A prototype of EC-less PFC based LED driver with BDC integrated is built and practical results are validated with simulation counterparts. The proposed LED driver is able to absorb the ripple current of twice line frequency and allow ripple free current to the load without using ECs which simplifies control complexity. The results show that the reduction in output current ripple from 125 to 11 mA using proposed ripple absorbing BDC topology. In addition, PF of 0.989 is achieved with DCM operation of NIBB PFC converter. The efficiency of EC-less ripple absorbing BDC topology with ac source voltage of 70 V is 86.20% and THD is 10.52% which satisfies the IEC 61000 class C limits. The result analysis demonstrates the effectiveness of proposed LED driver that provides significant reduction in output ripple current and voltage, and increased life-span of LED driver using film capacitor instead of larger size ECs.

6 References

1 Jane, G.-C., Lin, Y.-L., Chiu, H.-J., *et al.*: 'Dimmable light-emitting diode driver with cascaded current regulator and voltage source', *IET Power Electron.*, 2015, **8**, (7), pp. 1305–1311

2 Luo, Q., Zhao, B., Zou, C., *et al.*: 'Analysis and design of a multi-channel constant current light-emitting diode driver based on high-frequency AC bus', *IET Power Electron.*, 2013, **6**, (9), pp. 1803–1811

3 Chen, C.-L., Liao, T.-J., Hung, C.-C.: 'Source switching circuit with low-gate-driving loss in high-voltage buck light emitting diode driver', *IET Power Electron.*, 2013, **6**, (4), pp. 663–671

4 Cheng, H.-L., Cheng, C.-A., Ku, C.-W., *et al.*: 'Single-stage driver for supplying high-power light-emitting-diodes with universal utility-line input voltages', *IET Power Electron.*, 2012, **5**, (9), pp. 1614–1623

5 Wei, H.W.H., Batarseh, I.: 'Comparison of basic converter topologies for power factor correction'. Proc. IEEE Southeastcon 1998 'Engineering for a New Era', 1998, pp. 348–353

6 Shrivastava, A., Singh, B., Pal, S.: 'A novel wall-switched step-dimming concept in LED lighting systems using PFC zeta converter', *IEEE Trans. Ind. Electron.*, 2015, **62**, (10), pp. 6272–6283

7 Shen, C.L., Wu, Y.E., Tsai, C.T.: 'Coupled-inductor Sepic-type PFC with soft-switching feature for LED lighting applications'. Proc. of the 2011 6th IEEE Conf. on Industrial Electronics and Applications, ICIEA 2011, 2011, pp. 2384–2389

8 Ramanjaneya Reddy, U., Narasimharaju, B.L.: 'Unity power factor buck-boost LED driver for wide range of input voltage application'. 2015 Annual IEEE India Conf. (INDICON), 2015, pp. 1–6

9 Almeida, P.S., Camponogara, D., Dalla Costa, M., *et al.*: 'Matching LED and driver life spans: a review of different techniques', *IEEE Ind. Electron. Mag.*, 2015, **9**, (2), pp. 36–47

10 Gu, B., Feng, Q., Lai, J.-S., *et al.*: 'Bridgeless electrolytic capacitor-less valley-fill AC/DC converter for offline Twin-Bus light-emitting diode lighting application', *IET Power Electron.*, 2013, **6**, (6), pp. 1132–1141

11 Camponogara, D., Vargas, D.R., Costa, M.A.D., *et al.*: 'Capacitance reduction with an optimized converter connection applied to LED drivers', *IEEE Trans. Ind. Electron.*, 2015, **62**, (1), pp. 184–192

12 Pinto, R.A., Cosetin, M.R., Campos, A., *et al.*: 'Compact emergency lamp using power LEDs', *IEEE Trans. Ind. Electron.*, 2012, **59**, (4), pp. 1728–1738

13 Lam, J., Jain, P.K.: 'A new high power factor, soft-switched LED driver without electrolytic capacitors'. 2013 IEEE Energy Conversion Congress and Exposition, ECCE 2013, 2013, pp. 823–828

14 Zhang, F., Ni, J., Yu, Y.: 'High power factor AC–DC LED driver with film capacitors', *IEEE Trans. Power Electron.*, 2013, **28**, (10), pp. 4831–4840

15 Wang, B., Ruan, X., Yao, K., *et al.*: 'A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers', *IEEE Trans. Power Electron.*, 2010, **25**, (3), pp. 592–601

16 Ruan, X., Wang, B., Yao, K., *et al.*: 'Optimum injected current harmonics to minimize peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers', *IEEE Trans. Power Electron.*, 2011, **26**, (7), pp. 1820–1825

17 Yoo, J., Jung, K., Jeon, I., *et al.*: 'Third harmonic injection circuit to eliminate electrolytic capacitors in light-emitting diode drivers', *J. Electr. Eng. Technol.*, 2012, **7**, (3), pp. 358–365

18 Lam, J., Jain, P.K.: 'A high power factor, electrolytic capacitor-less AC-input LED driver topology with high frequency pulsating output current', *IEEE Trans. Power Electron.*, 2015, **30**, (2), pp. 943–955

19 Wang, R., Wang, F., Lai, R., *et al.*: 'Study of energy storage capacitor reduction for single phase PWM rectifier'. Conf. Proc. – IEEE Applied Power Electronics Conf. and Exposition – APEC, 2009, pp. 1177–1183

20 Wang, S., Ruan, X., Yao, K., *et al.*: 'A flicker-free electrolytic capacitor-less AC–DC LED driver', *IEEE Trans. Power Electron.*, 2012, **27**, (11), pp. 4540–4548

21 Yang, Y., Ruan, X., Zhang, L., *et al.*: 'Feed-forward scheme for an electrolytic capacitor-less AC/DC LED driver to reduce output current ripple', *IEEE Trans. Power Electron.*, 2014, **29**, (10), pp. 5508–5517

22 Narasimharaju, B.L., Dubey, S.P., Singh, S.P.: 'Design and analysis of coupled inductor bidirectional DC–DC convertor for high-voltage diversity applications', *IET Power Electron.*, 2012, **5**, (7), pp. 998–1007