A ZVS Series Resonant Current-Fed PWM Controlled DC-DC Converter

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***Abstract*-. This paper investigates a series LC resonance based current-fed DC-DC converter to enable wide-range zero voltage switching (ZVS) of the semiconductor devices for high-voltage gain applications. A series resonant tank allows natural commutation of the semiconductor devices and improved transformer utilization owing to the sinusoidal current through the transformer primary by operating the converter near the resonant frequency of the LC tank. ZVS of the active devices minimizes the switching losses, duty cycle loss and also limits the peak and circulating current allowing the use of lower rated components. Furthermore, proposed converter employs a simple duty cycle control with an interleaved boost derived structure and voltage-doubler to meet the desired output voltage levels. The operational principles, detailed mathematical analysis and simulation results are presented to verify the feasibility of the proposed idea.**

Key words: Current-fed converter, boost-derived, series resonance, Zero Voltage switching

I. INTRODUCTION

Rapid integration of alternative energy sources driven by factors like increased environmental concern, climate chnage and massive carbon emssions is shaping the future for sustainable, secure and affordable energy system. Clean distributed generation or dc microgrid system utilizing energy sources like solar/fuel-cell are growing quickly owing to the reduced conversion stages, power scalability, high efficiency and better controllability to support loads like modern data center, energy storage, UPS as well as applications like EV interfacing to DC microgrid [1]. Despite several advantages, these alternative sources exhibit huge variation in their output voltage and sluggish response to load variations due to their inherent operational characteristics. Therefore, power electronics converter becomes an essential link to handle the variable nature of loads and must posses greater flexibility to provide regulated output voltage at all times to accommodate huge source-side variability and uncertainty inherent to PV/fuel-cells [2][3][4].

In addition to the DC microgrid applicatios, multi-stage topologies like solar/fuel-cell inverters also utilize front-end high frequency (HF) transformer isolated dc/dc converter in conjunction with a PWM inverter for the inter-connection to an AC system. Therefore, for the energy-efficient operation and to improve the fuel utilization, DC-DC converters with high boosting capability, low input ripple current, unidirectional power flow and galvanic isolation have become ubiquitous for interfacing low-voltage clean energy sources like PV/fuel-cell to a high-voltage ac or dc bus. Traditionaly, voltage-fed dc-dc converters were dominant, but due to their inherent buck characteristics the desired voltage boosting action can only be achieved through the high turns ratio of HF transformer. As a result, the leakage inductance will be large resulting in overvoltage spikes on the semiconductor devices. They also exhibit high current ripple and duty-cycle loss, necessitating huge input filter capacitor making them inefficient for low voltage high curent applications. Therefore, to meet the aforementioned desired features, current-fed topology is a promising alternative as compared to the voltage-fed toplogy for low-voltage high current applications [5]. However, current-fed topology also suffers from large turn-off voltage overshoot across the semiconductor devices owing to the energy stored in the leakage inductance. Moreover, hard-switched semiconductor devices limits converter operation at high frequency, considerably impacting the size of magnetics and EMI filters, and therefore results in less efficient and bulky system [6][7].

In order to overcome these challenges, various soft-switching techniques are reported to operate the converter at high frequency with improved conversion efficiency. Initially, passive snubber circuits have been utilized to limit the turn-off voltage spike across the semiconductor devices by redirecting the leakage energy to the passive components while compromising on the conversion efficiency [8][9]. Alternatively, active-clamping was intoduced to enable soft–switching of the semiconductor devices with improved efficiency. However, it reduces converter's boost capacity and introduces circuit complexity on account of additional floating active devices and HF capacitor [10],[11]-[15][16][17]. Furthermore, concept of secondary modulation was introduced for current-fed dual active bridge topologies in [18][19]. Zero current switching (ZCS) and natural device voltage clamping has been achieved by modulating the load side active devices. Such converters offer wide range ZCS and low voltage stress while increasing the cost and complexity of the converter. Moreover, these converters are limited to bidirectional applications only. To reduce the component count and turn-off loss, soft-switching converters engaging resonance characteristics were introduced. Resonant converters are broadly classified as PWM controlled or frequency controlled. These converters eliminate the need for additional snubber circuitary and utlizes circuit paracitics to enable natural commutationof the semiconductor devices [20][21]-[24]. In

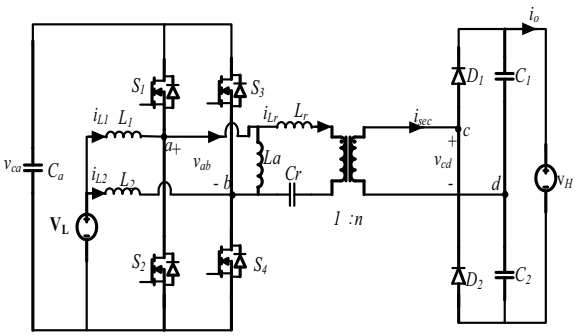

Fig. 1. Proposed series-LC resonant current-fed dc-dc converter topology.

[25], bidirectional resonant converters are reported. However, in comparison to the bi-directional resonant converters, it is much easier to design and operate a unidirectional resonant converter owing to simple control and less components. Unlike the conventional resonant converters, soft-switching quasi-resonant converters were also reported to provide reduced circulating and peak currents [26],[27]. However, they necessitate complicated variable frequency control to maintain soft-switching for wide variations in source voltage and load. In addition, these converters result in complex magnetic design owing to the wide switching frequency range.

This paper proposes a series resonant current-fed PWM controlled DC-DC converter topology to achieve ZVS of the semiconductor devices for wide variability in load and source voltage. The proposed converter exploits interleaved boost-derived characteristics with a voltage doubler circuit at the output stage to fulfill the high-voltage gain requirement as shown in Fig. 1. A simple PWM control is implemented to achieve wide range ZVS and output voltage regulation for all operating conditions. In addition, the switching frequency of converter is fixed at resonant frequency resulting in better transformer utilization and also simplifies the magnetic design and filter requirement. The performance of the proposed topology is evaluated for the given specifications. The paper is organized as follows; Section II describes the proposed converter and its steady state analysis, section III covers the detailed design aspects of the converter, Section IV presents detailed simulation results, and Section V concludes the paper.

II. Proposed Converter Topology And Its Steady State Analysis

The steady-state operation and analysis of the proposed series resonant current-fed converter is explained in this section. The proposed converter has boost derived primary, a series resonant tank, HF transformer and voltage doubler at the secondary. A simple duty control is used to achieve following objectives: 1) to transfer active power from source to load 2) to maintain regulated output voltage for wide range of source voltage and 3) to zero-voltage-switching (ZVS) of all the semiconductor switches. The following assumptions are made to understand the operation and analysis of the converter:

1. Input boost inductors L are large enough to maintain the constant current through it.

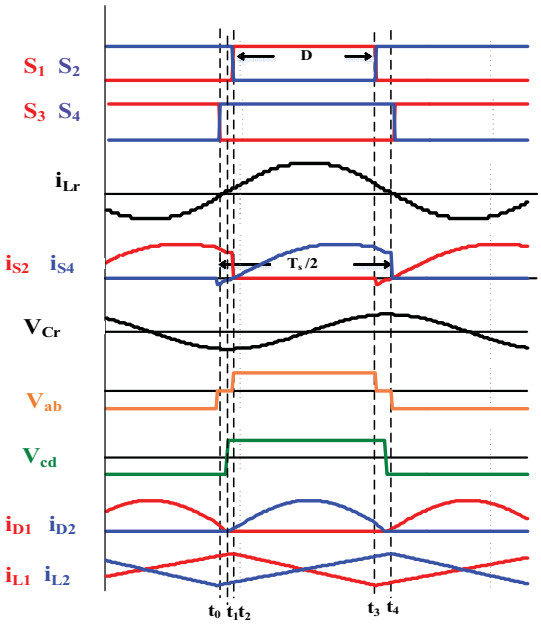

Fig. 2. Steady state operating waveforms of the converter for D<0.5.

2. Output capacitors C_a are large to maintain regulated voltage at the output.
3. All semiconductor components including mosfets and diodes are considered ideal.
4. Switching frequency is considered fixed at resonant frequency.
5. For this design, large value of L_m is considered in order to have reduced circulating currents.

Fig. 2 shows the operating waveforms of the converter for D < 0.5. Switches in the same leg have complementary gating signals while the top switches (S_1 S_3) with duty D and bottom switches (S_2 S_4) are 180 shifted from one another. Duty is kept constant at 0.5 for source voltage of 50V and can be lower to higher depending upon the corresponding source voltage. However, current through the transformer primary remains absoultely sinusoidal for D=0.5 but changes slightly for values other than D=0.5.

Interval (t_0-t_1): *In* Fig. 3(a) at instant t_1, S_4 is turned-on and switches S_2 is already conducting resulting in zero voltage at the bridge output V_{ab}=0. Diode D2 is conducting due to the negative voltage at the secondary of the transformer. The input current is shared between switch S_2 and S_4 while current through auxiliary inductor L_a (i_{La}) freewheels through switch S_2 and S_4. From the equivalent circuit it is possible to obtain:

$$V_{ab} = 0 \ and \ V_{cd} = -\frac{V_H}{2} \quad (1)$$

$$V_L = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \quad (2)$$

$$i_{L1} = i_{L2} = \frac{I_{in}}{2} \quad (3)$$

Interval (t_1- t_2): *In* Fig. 3(b) at instant t_1, both switch S_2 and S_4 remains ON. Also the body diode of switch S_1 starts conducting before S_1 turns ON. The bridge output voltage

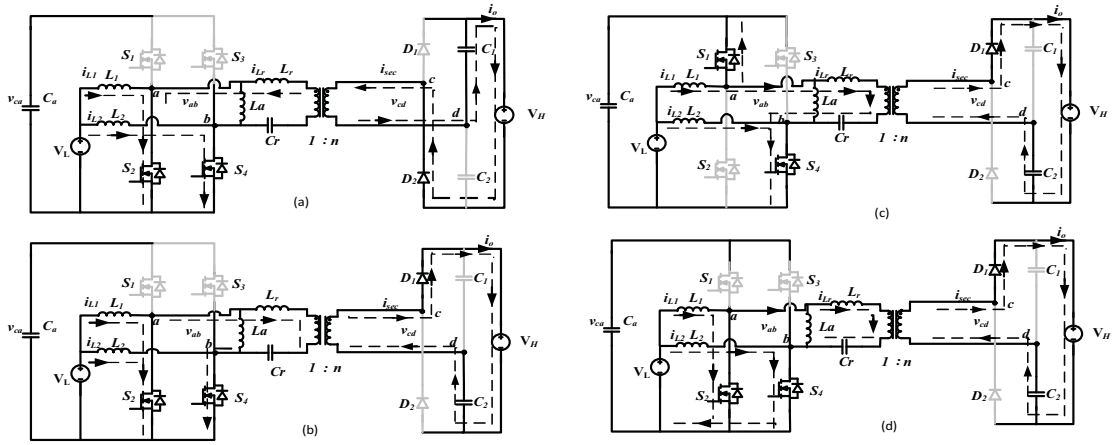

Fig. 3. Equivalent circuit of the proposed converter during different intervals of operation in half switching cycle.

becomes positive and a positive current flows through the transformer primary. Diode D_1 of the voltage doubler circuit gets forward. During this overlap interval, inductors L_1 and L_2 are charged by input voltage V_L and L_r resonates with C_r and resonant energy is transferred to the secondary.

$$V_{ab} = V_{ca} = \frac{V_L}{D} \text{ and } V_{cd} = \frac{V_H}{2n} \quad (4)$$

During this mode, current through L_1 starts decreasing and current through L_2 starts increasing linearly as indicated by.

$$\frac{di_{L1}}{dt} = \frac{V_L - V_{ca}}{L_1} \quad (5)$$

$$\frac{di_{L2}}{dt} = \frac{V_L}{L_2} \quad (6)$$

From the equivalent circuit, during this mode

$$V_{ab} - L_r \frac{di_{Lr}}{dt} - V_{cr}(t) - \frac{V_H}{2n} = 0 \quad (7)$$

$$i_{Lr(t)} = C_r \frac{dV_{cr}(t)}{dt} \quad (8)$$

Differential equation (13) and (14) can be solved to obtain $i_{Lr}(t)$ and $V_{cr}(t)$ assuming $i_{Lr(t_1)} = 0$ and $V_{cr}(t_1) = V_0$ can be expressed as

$$i_{Lr}(t) = \frac{1}{Z_r}\left(V_{ca} - V_o - \frac{V_H}{2n}\right) sin\omega_o(t - t_1) \quad (9)$$

$$i_{Lr}(t) = I_{Lr\_peak}\, sin\omega_o(t - t_1) \quad (10)$$

$$V_{cr}(t) = V_{ca} - \frac{V_H}{2n} + \left(V_o - V_{ca} + \frac{V_H}{2n}\right) cos\omega_o(t - t_1) \quad (11)$$

Where,

$\omega_o = \frac{1}{\sqrt{L_r C_r}}$ is the resonant frequency.

and $Z_r = \sqrt{\frac{L_r}{C_r}}$ is the characteristics impedance.

Interval (t_2- t_3): In Fig. 3(c) at instant t_2, S_2 turns-off while switch S_1 turns on at zero voltage as its body diode starts conducting due to positive I_{L1}. This allows zero voltage turn on of switch S_1.The bridge output voltage becomes positive and current through L_1 starts decreasing and current through L_2 starts increasing linearly.

$$V_{ab} = 0 \text{ and } V_{cd} = \frac{V_H}{2n} \quad (12)$$

$$i_{Lr}(t) = i_{Lr}(t_2) cos\omega_o(t - t_2) - \frac{1}{Z_r}\left(V_{cr}(t_2) + \frac{V_H}{2n}\right) sin\omega_o(t - t_2) \quad (13)$$

$$V_{cr}(t) = -\frac{V_H}{2n} + i_{Lr}(t_2)\, Z_r sin\omega_o(t - t_2) + \left(V_{cr}(t_2) + \frac{V_H}{2n}\right) cos\omega_o(t - t_2) \quad (14)$$

Interval (t_3- t_4):In Fig. 3(d) at instant t_3, S_1 turns off while S_4 is still conducting. Due to positive current through transformer primary, diode across S_2 starts conducting which allows zero voltage turn-on of S_2. The bridge output voltage again commutes to zero but secondary voltage remains positive and current i_{Lr} starts decreasing linearly and transfers power to the secondary through diode D_1.

A similar operation works for the rest of the stages after t_4 in another half of the switching period. Also, the time intervals t_1, t_2, t_3 and t_4 can be expressed in terms of duty cycle D as:

$$t_0 = 0$$

$$t_1 = \frac{1 - 2D}{4}\ T_s$$

$$t_2 = \frac{1 + 2D}{4}\ T_s$$

$$t_3 = \frac{T_s}{2}$$

where T_s is the switching interval of the converter.

III. DESIGN CONSIDERATIONS

The proposed converter is designed to achieve the set objectives. Therefore, a detailed design approach to allow optimal selection of various converter parameters has been discussed in this section.

A. Voltage gain of the proposed converter

The overall converter voltage gain can be expressed as:

$$G_{conv} = G_{interleaved\_boost} * G_{LC_{resonant}} * n * G_{rectifier}$$

$$G_{conv} = \frac{V_H}{V_L} \quad (15)$$

$$G_{interleave\ boost} = \frac{V_{ca}}{V_L} = \frac{1}{1 - D} \quad (16)$$

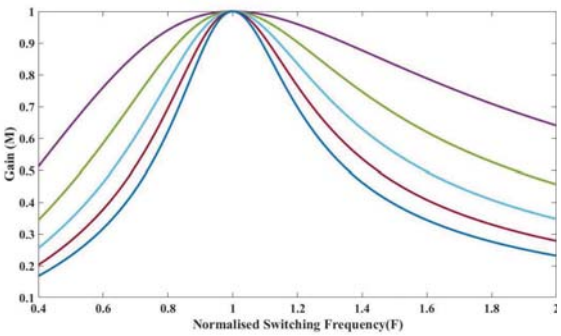

Fig. 4. Proposed series-LC resonant current- dc-dc converter topology.

$$G_{rectifier} = 2 \tag{17}$$

In order to estimate resonant tank gain, voltage gain expression for the tank can be derived as follows:

The fundamental rms for the bridge voltage output V_{ab} and voltage doubler input voltage V_{cd} can be expressed as

$$V_{ab} = \frac{2\sqrt{2} * V_{ca}}{\pi} \tag{18}$$

$$V_{cd} = \frac{4 * {V_H}/{2n}}{\pi} = \frac{2 * V_H}{n\,\pi} \tag{19}$$

By applying Laplace transformation, equivalent impedance of the resonant network can be obtained as

$$Z_r = \frac{V_{ab}}{I_{Lr}} = R_o \sqrt{1 + \left(Q\left(F - \frac{1}{F}\right)\right)^2} \tag{20}$$

where

$Q = \frac{\omega_r L_r}{R_o}$, $F = \frac{\omega_s}{\omega_r} = \frac{F_s}{F_r}$, $\omega_r = \frac{1}{\sqrt{L_r C_r}}$, $R_o = \frac{2R_L}{\pi^2 n^2}$ and

n is the HF transformer turns ratio.

From (20), resonant tank gain can be expressed as

$$\frac{V_{cd}}{V_{ab}} = \frac{1}{\sqrt{1 + \left(Q\left(F - \frac{1}{F}\right)\right)^2}} \tag{21}$$

Resonant tank gain can be plotted against normalized frequency as shown in Fig. 4. It should be observed that the gain is maximum when switching frequency is equal to resonant frequency. And for this design, switching frequency is kept constant at resonant frequency i.e at 100kHz.

$$G_{LC_{resonant}} = 1$$

B. ZCS condition

The proposed converter has to satisfy following conditions to confirm ZCS under wide operating range. Resonant current i_{Lr} and voltage V_{Cr} at different time instants can be derived to obtain ZVS condition. ZVS for the primary switches can be achieved if the body diode conducts before the corresponding switch. Therefore, ZVS of the switches can analyzed by the following equations:

ZVS of switch S_1 and S_2:

$$i_{L1}(t_2) > i_{Lr}(t_2) + i_{La}(t_2) \tag{22}$$

ZVS of switch S_3 and S_4:

$$i_{L1}(t_3) < i_{Lr}(t_3) + i_{La}(t_3) \tag{23}$$

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ZVS of switch S_1 and S_2:

$$i_{L1}(t_1) > i_{Lr}(t_1) + i_{La}(t_1) \tag{24}$$

ZVS of switch S_3 and S_4:

$$i_{L1}(t_2) < i_{Lr}(t_2) + i_{La}(t_2) \tag{25}$$

$$i_{La}(t_2) = \frac{V_{ca}}{2L_a} DT_s \tag{26}$$

$$i_{L1}(t_2) = \frac{P_{in}}{2\ V_L} - \frac{V_L(1-D)T_s}{2L_1} \tag{27}$$

$$i_{Lr}(t_2) = \frac{1}{Z_r}\left(V_{ca} - V_o - \frac{V_H}{2n}\right)\sin(2\pi D) \tag{28}$$

From Fig. 2 the average resonant current during half-switching cycle can be obtained from

$$I_{Lr} = \frac{1}{T_S}\int_{t_1}^{t_4} i_{Lr}(t) \tag{29}$$

$$= \frac{1}{T_S}\int_{t_1}^{t_4} I_{Lr\_peak}\ sin\omega_o(t - t_1) \tag{30}$$

$$= \frac{1}{T_S}\frac{I_{Lr\_peak}}{\omega_o}\left(1 - \cos(2\pi D)\right) \tag{31}$$

$$I_{Lr\_peak} = \frac{n\ I_o\ T_S\ \omega_o}{1 - \cos(2\pi D)} \tag{32}$$

Therefore, peak of the resonant tank can be limited by carefully selecting the resonant tank parameters while maintaining the ZVS of the active switches.

C. Design of resonant tank parameters

The resonant tank parameters L_r and C_r are computed by making the resonant frequency equal to the switching frequency of the converter. Whereas, according to (9), (13) and (28), it should be noted that the resonant current is inversely proportional to the impedance Z_r of the resonant tank. However a large value of impedance would lead to large inductor which directly decides the size of the tank network thereby affecting the converter power density. Therefore an appropriate value of Z_r is selected in order to limit the peak resonant current as well as inductor size for a chosen capacitor value.

D. Turns Ratio

Selction of turns ratio of the HF transformer should be such that the output voltage remains regulated at 400 V for the entire range of source voltage. Also, it is suggested that the turns ratio of the HF transformer is selected for the duty cycle D=0.5 when the voltage is at its midpoint of the entire voltage range.

Therefore, the turns ratio of the transformer is chosen as n=2 for the input side voltage being the nominal voltage at 50 V and considering unity gain of the LC tank, by using below expression.

$$n = \frac{V_H}{2\,V_{ca}} = \frac{V_0(1-D)}{2\,V_L} \tag{33}$$

E. Component stresses

The maximum voltage stress across the primary side MOSFET can be expressed as:

$$V_{DS1-4} = \frac{V_L}{1-D} \tag{34}$$

The rectifier diode voltages are clamped at Vo due to the capacitive output filter.

$$V_{D1-2} = V_H \tag{35}$$

F. Boost inductor calculation

Design of boost inductor is decided by the allowable ripple in the input current. In this case, ripple content depends on the duty cycle. The expression for input boost inductor is shown below:

For D = 0.5

$$L_1 = L_2 = \frac{V_L D\,T_S}{\Delta I_{in}} \tag{36}$$

However for D < 0.5 or D > 0.5, boost inductor current I_{L1} and I_{L2} are no longer 180º phase shifted resulting in the following expression for obtaining accurate ripple at the input side.

$$L_1 = L_2 = \frac{V_L(2D-1)\,T_S}{\Delta I_{in}} \tag{37}$$

IV. Results and Discussion

The proposed converter has been simulated using PSIM software to verify the desired operation and analysis. Open-loop control has been employed to evaluate the steady state performance of the proposed converter for the given converter specifications and design parameters.

Following are the converter specifications rated for 400W power: input voltage V_L= 40-60V with V_{nom}=50V, high side voltage V_H=400V, switching frequency, *fs* =100kHz. Design parameters include, L_r=57μH, C_r=47nF, $L_1 = L_2$=400μH, output capacitor C_1= C_2=100μF and n=2. Simulation results in Fig. 5(a) depicts the zero voltage switching of devices S_2 and S_4 for V_L= 50V at D=0.5. It can be observed that the switch current goes negative at turn-on implying anti-parallel diode conduction before the switch turns on. Fig. 5(b) illustrates ZVS of devices S_2 and S_4 for V_L= 40V with D>0.5. It can also be observed from Fig. 5 that the resonant current I_{Lr} is sinusoidal which is in agreement with the theoretical analysis.

Fig.6 depicts average output voltage and current waveforms for V_L=50V (D=0.5) and V_L=40V (D<0.5). Fig. 6(a) and 6(b) validate that the output voltage is maintained nearly constant at 400V for D=0.5 and D<0.5 scenarios respectively. A simple PWM control is implemented to achieve soft commutation of the active devices and output volatge regulation for wide range of source voltage.

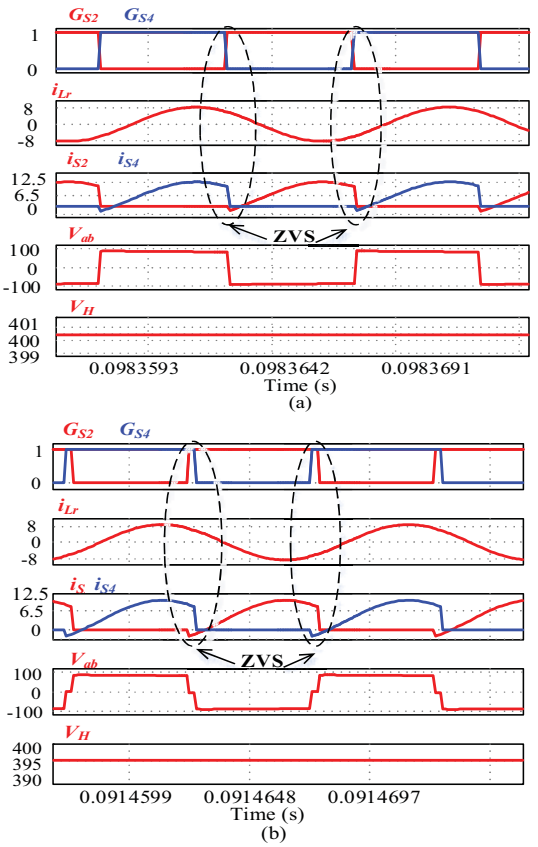

Fig. 5. Simulated waveforms for (a) V_L= 50V at D=0.5 and (b) V_L= 45V at D=0.45 at rated load condition.

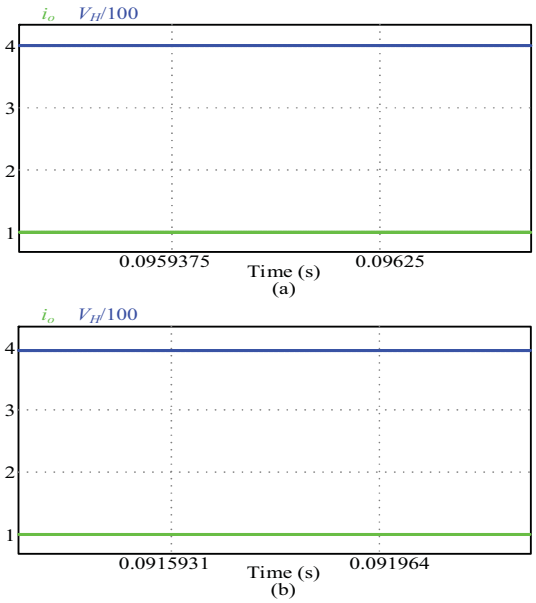

Fig. 6. Simulated waveforms for high side volatge and current for (a) V_L= 50V and (b) V_L= 45V at rated load.

V. CONCLUSION

A current-fed PWM controlled DC-DC converter utilizing series LC resonance to achieve ZVS of the semiconductor devices has been analysed. The key objectives of the proposed converter are to maintain regulated output volatge and ZVS of the primary switches for wide range of source voltage. Soft commutation employing series LC resonant has resulted in reduced circulating and peak current along with improved current quality owing to the sinusoidal nature of resonant current. Therefore, switching and conduction losses are significantly reduced. It also allows use of low rating devices and results in higher conversion efficiency over wide range of operation. Simulation results rated at 400W are presented to validate the performance of the proposed converter. Boost structure and voltage doubler makes the topology feasible for high voltage gain applications like solar to battery charging, data centers, EV interfacing to DC microgrid etc.

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