

A Cost-Effective Zero-Voltage Switching Dual-Output LED Driver

Ramanjaneya Reddy U and Narasimharaju B. L, *Senior Member, IEEE*

Abstract—Coupled-inductor (CI) converters are widely used in the light-emitting diode (LED) lighting applications due to several advantages, such as high step-down conversion, reduced switch/diode stress as compared to conventional buck converters. However, the main drawback of CI buck converter is high-voltage spikes during turn-OFF instant due to the leakage inductance of a CI, which leads to switching device failure. Passive clamp circuits are used to overcome the leakage inductance problem, but these clamp circuit's results in reduced efficiency and increased cost. This paper proposes a high step-down zero-voltage switching dual-output coupled-inductor buck (ZVS-DOCIB) LED driver with dimming control. The proposed LED driver provides various advantages like high step-down conversion, effective recovery of leakage energy, elimination of voltage spikes, reduced switching loss due to ZVS operation of both the switching devices, and less switching device count, particularly for multioutput drivers. Also, ZVS operation provides a significant reduction in switching losses, which results in high efficiency. Furthermore, dimming control is studied to regulate the average output currents. This paper presents design and analysis of the proposed ZVS-DOCIB converter. A prototype of the converter has developed and validated experimentally with simulation counterparts.

Index Terms—Buck converter, coupled inductor (CI), efficiency, LED, zero-voltage switching (ZVS).

I. INTRODUCTION

GLOBALLY one-fourth of an electrical power contributes to lighting applications, which demand energy saving and reliable lighting systems [1]. Solid-state lighting technology is growing enormously due to its significant advantages like high brightness, longevity, absence of toxic gas, energy efficient, and compact size [2]. Due to durability and energy efficient, LEDs are used in various applications, such as household, street, transportation, indoor lighting systems, and LCD panels, etc. When a LED driver utilizes an ac source as an input, usually the conventional two-stage LED driver, as shown in Fig. 1(a), is adopted. This two-stage structure is composed of power factor correction (PFC) regulator followed by a dc–dc converter. Thus, a two-stage PFC technique needs more components, which increases converter size and control complexity significantly. Fig. 1(b)

Manuscript received May 27, 2016; revised August 17, 2016 and October 22, 2016; accepted November 29, 2016. Date of publication December 6, 2016; date of current version May 9, 2017. Recommended for publication by Associate Editor L. Huber.

The authors are with the Department of Electrical Engineering, National Institute of Technology, Warangal 506004, India (e-mail: ureddy89@gmail.com; bnlraju@nitw.ac.in).

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Digital Object Identifier 10.1109/TPEL.2016.2636244

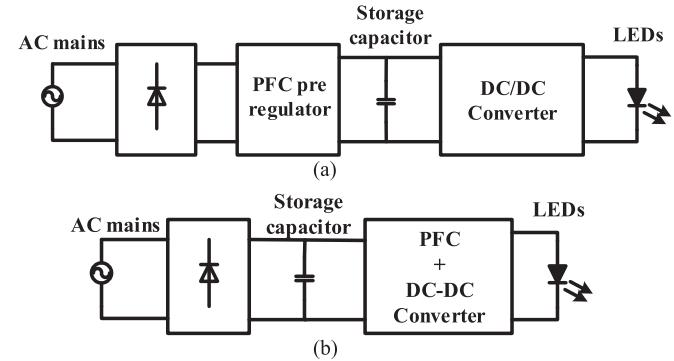


Fig. 1. (a) Classical two-stage LED driver. (b) Single-stage LED driver.

shows the single-stage PFC circuit that provides both PFC operation and regulated dc voltage. Since, the cost is a significant aspect, single-stage PFC-based LED drivers with simple control technique leads to compact size, high efficiency, and hence, it is an attractive choice for lighting applications [3], [4]. The buck converter is an attractive solution for LED lighting applications due to its simplicity and less component count. However, the efficiency decreases when the high step-down conversion is desired due to the fact that poor utilization of the switch (less duty ratio) at the peak value of input voltage [5].

A few coupled-inductor buck (CIB) topologies reported in the literature has high step-down conversion ratio with increased duty cycle. However, the coupled-inductor (CI) topologies cause high-voltage spikes during turn-OFF instant due to the leakage inductance of CI, which leads to subsequent failure of switching devices [6], [7]. Furthermore, passive clamp techniques are used to minimize/eliminate the switching transients but with increased cost and complexity [5], [7]. Several authors have proposed CI topologies with leakage energy recycling with soft-switching techniques to reduce conduction losses and to improve the efficiency. In [8], a converter is introduced with switched capacitor and CI to accomplish the high step-down conversion, but in this topology, all the power switches are floating which needs an extra isolated gate driver, and, hence, increases the gate driver complexity. Moreover, the converter is suitable only for single output. In [9], a high step-down converter with a resonant voltage divider (RVD) is addressed. However, the RVD has the major drawback of large surge currents at startup, which results in component failure. In [10]–[15], soft-switching converters with CI are presented. In [10], zero-voltage switching (ZVS) synchronous buck converter is proposed for single output with the

low step-down ratio. The method presented in [11] is a ZVS synchronous buck CI converter which requires more components for a single output. In [12], introduced a zero-current switching (ZCS) turn-ON and ZVS turn-OFF by adding CI and diode to a conventional buck converter with poor switch utilization. The method proposed in [13] introduced a ZCS-ZVS bidirectional dc–dc converter which requires more components for a single output. Thus, it increases the size and cost. In [14], a nonisolated ultrahigh step-down converter for recycling leakage energy using a capacitor between dc bus and CI is proposed. A nonisolated CI high step-down converter with zero dc-magnetizing inductor current and with ZVS operation provides improved efficiency [15]. However, converter size becomes bulky and also has high cost due to more component count.

For high-power LED lighting applications, usually number of LEDs connected in series, in parallel, and in a series–parallel combination. The LEDs of series-connected string generate similar light output, but this type of arrangement is not reliable because a whole string of LEDs will fail even if anyone LED of the string is damaged. The major issue in the paralleling of LED strings is unequal sharing of forward currents. Linear and switched-mode current regulators are connected in each string to drive the parallel strings with an equal current sharing, but using a linear regulator for equal current sharing will result in reduced efficiency. In contrast, switched-mode current regulator can overcome the drawbacks of the linear current regulator, but it requires more components, and, hence, high cost. For aforementioned reasons, the switched-mode regulator-based multioutput LED drivers with dimming control may be a preferred choice. In [16]–[19], multioutput converters are proposed. In [16], a dual-output bridgeless single-ended primary inductance converter (SEPIC) is proposed, in which two SEPIC converters connected in parallel to drive two loads. This converter uses more component count and operating with hard switching which leads to high cost and less efficiency. A multioutput buck converter provides two different voltages, but the step-down voltage gain is low, and also, the efficiency is less due to hard switching [17]. A wide range high step-down multioutput converter is proposed in [18], but it requires four power switches for two outputs. In [19], proposed hard-switching step-down multioutput current autobalancing LED driver has less efficiency and no illumination control. This apt review motivates to design and develop a high-efficient multioutput converter for enhancing step-down conversion, increasing the conversion efficiency and possessing multiple outputs with different voltage levels. Therefore, this study proposes a zero-voltage switching dual-output coupled-inductor buck (ZVS-DOCIB) converter to achieve high step-down voltage ratio, high-power conversion efficiency, and with two different voltage levels. Furthermore, dimming control is studied to regulate the average output currents. Thus, the proposed ZVS-DOCIB converter provides various advantages, such as high step-down conversion, effective recovery of leakage inductance, reduced switching loss, increased efficiency, compact size, and low cost. Therefore, it makes an attractive choice for multioutput LED drivers with common input dc link and only one switch per output with illumination control of each load. The main idea of the proposed study is to achieve high

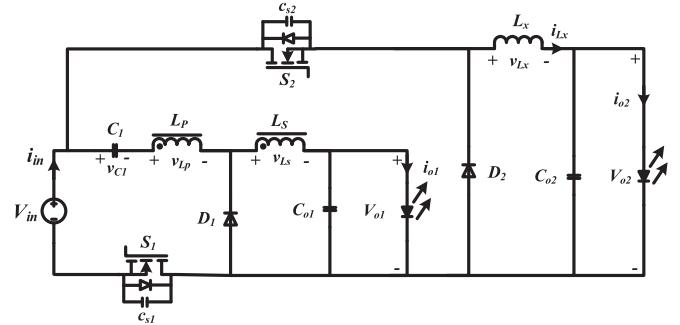


Fig. 2. System configuration of the proposed high step-down ZVS-DOCIB LED driver.

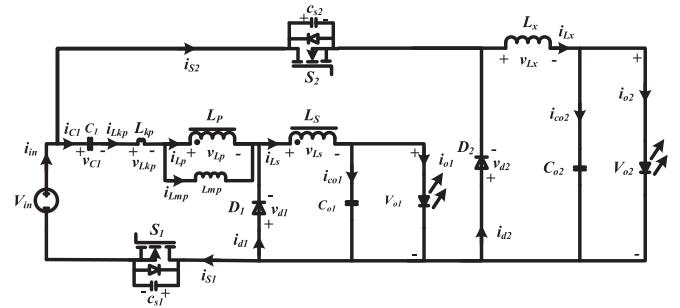


Fig. 3. Equivalent circuit of the proposed high step-down ZVS-DOCIB LED driver.

efficiency of dc–dc postregulator as the second stage of conventional two-stage solution (PFC + postregulator). The proposed solution is cost effective as compared with the three-stage solutions. Furthermore, the two independent output performances are the consequence of providing no overvoltage at the main switch of the CIB and also to drive the additional load.

II. PROPOSED CONVERTER AND DESIGN ANALYSIS

Fig. 2 depicts the proposed high step-down ZVS-DOCIB converter, which contains main switch (S_1), auxiliary switch (S_2), diodes (D_1 and D_2), and energy recycling capacitor (C_1), one CI composed of primary inductance (L_P) and secondary inductance (L_S), auxiliary inductor (L_x), and output capacitors (C_{o1} and C_{o2}). Also, the input voltage/current is represented by V_{in}/i_{in} , the output voltage/current of load-1 is represented by V_{o1}/i_{o1} , and load-2 is represented by V_{o2}/i_{o2} . The equivalent representation of LED loads is denoted by R_{o1} and R_{o2} . Fig. 3 illustrates the equivalent circuit of the proposed ZVS-DOCIB converter with voltage polarities and current directions. The various circuit variables are defined as follows: i_{C1} and v_{C1} are energy recycling capacitor current and voltage, respectively, i_{Lkp} and v_{Lkp} are leakage inductor current and voltage, respectively, i_{Lp} and v_{Lp} are primary winding current and voltage, respectively, i_{ls} and v_{ls} are secondary winding current and voltage, respectively, i_{Lx} and v_{Lx} are auxiliary inductor current and voltage, respectively, i_{d1} and v_{d1} are current and voltage of diode D_1 , and i_{d2} and v_{d2} are current and voltage of diode D_2 .

The CI in Fig. 3 is a replica of an ideal transformer with magnetizing inductance L_{mp} and leakage inductance of L_{kp}

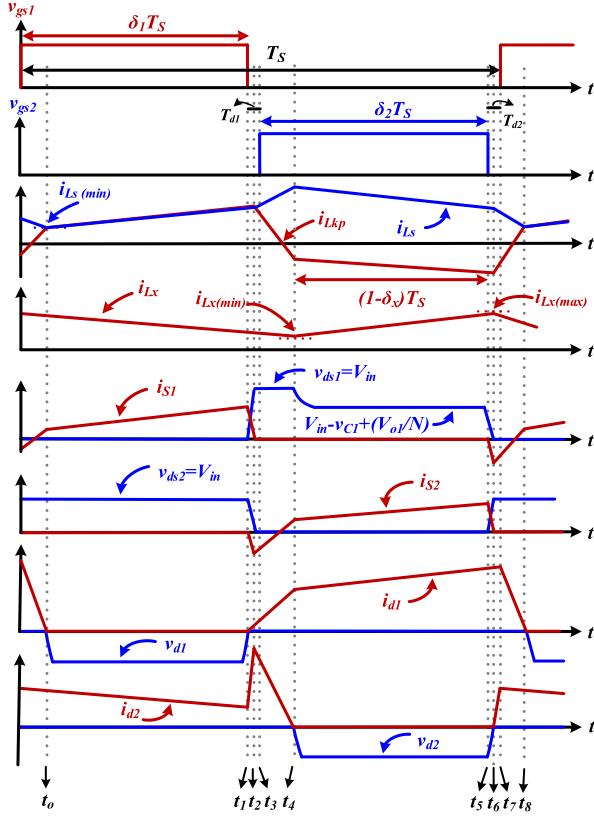


Fig. 4. Idealized waveforms of the proposed ZVS-DOCIB LED driver.

[6]. The turn's ratio (N) and coupling coefficient's (k_p and k_s) of an ideal transformer are defined as follows:

$$N = N_S / N_P \quad (1)$$

$$k_p = L_{mp} / (L_{mp} + L_{kp}) = L_{mp} / L_P$$

$$k_s = L_{ms} / (L_{ms} + L_{ks}) = L_{ms} / L_S \quad (2)$$

where N_P and N_S represent the number of turns in the primary and secondary winding of CI, respectively. The L_{kp} and L_{ks} represent the leakage inductance/s of L_P and L_S , respectively. L_{mp} and L_{ms} represent the magnetizing inductance/s of L_P and L_S , respectively. To make $L_{mp} = L_P$ and $L_{ms} = L_S$ from (2), the coefficient of coupling simply set to 1. Assuming 100% of coupling (i.e., $k_p = 1$), the mutual inductance (M) can be calculated as $M = \sqrt{L_P L_S} = N L_P$.

Fig. 4 depicts the idealized waveforms of the proposed ZVS-DOCIB converter. The gating signals for the main switch (V_{gs1}) and auxiliary switch (V_{gs2}) are a compliment to each other. The duty cycle of the main switch (S_1) and auxiliary switch (S_2) are defined as δ_1 and δ_2 , respectively. Moreover, T_S represents the switching period of power switches S_1 and S_2 . In order to make analysis of the proposed converter simple, the following assumptions has been made.

- 1) All the power switches and diodes are ideal.
- 2) In order to maintain the constant output voltage, the output capacitors assumed to be higher values.

A. Modes of Operation

The working principle of the ZVS-DOCIB is described in eight operating modes over a switching period (T_S). Each mode of operation with equivalent circuits are illustrated as shown in Fig. 5 and explained as follows:

1) Mode-1: ($t_o - t_1$) [see Fig. 5(a)]: At $t = t_0$ the switch S_1 is in conduction, while switch S_2 is in OFF state. The difference between input voltage V_{in} and output voltage V_{o1} is impressed across the string of capacitor C_1 and the CI. Therefore, the currents i_{Lkp} , i_{Lp} , and i_{Ls} increase slowly. The current i_{Lkp} is same as the current i_{S1} which flows through input source and capacitor C_1 . Also, the energy in L_x will discharge through D_2 . At $t = t_1$, mode-1 ends when S_1 is turned-OFF and D_1 gets forward biased. According to Kirchhoff current law (KCL) and Kirchhoff voltage law (KVL), the key current and voltage equations are given by

$$\left. \begin{aligned} i_{S1}(t) &= i_{C1}(t) = i_{Lkp}(t) = i_{Ls}(t) \\ i_{Lx}(t) &= i_{d2}(t) \end{aligned} \right\} \quad (3)$$

$$V_{in} = v_{C1} + v_{Lkp} + v_{Lp} + v_{Ls} + V_{o1} \quad (4)$$

$$v_{Lx} = L_x \frac{di_{Lx}}{dt} = -V_{o2}. \quad (5)$$

By using $v_{Lkp} = v_{Lp}(1 - k_p)/k_p$ and $v_{Lp} = v_{Ls}/N$, (4) can be rearranged as follows:

$$\begin{aligned} V_{in} &= v_{C1} + v_{Ls}(1 - k_p)/Nk_p + v_{Ls}/N + v_{Ls} + V_{o1} \\ &= v_{C1} + v_{Ls}/Nk_p + v_{Ls} + V_{o1}. \end{aligned} \quad (6)$$

From (6), the voltage v_{Ls} can be obtained as

$$\begin{aligned} v_{Ls} &= \frac{Nk_p (V_{in} - v_{C1} - V_{o1})}{(1 + Nk_p)} \\ &= \left(\frac{N_2 k_p}{N_1 + N_2 k_p} \right) (V_{in} - v_{C1} - V_{o1}). \end{aligned} \quad (7)$$

The voltage across the primary inductor is v_{Ls}/N and the voltage across the auxiliary inductor is $-V_{o2}$. Therefore, the current i_{Lp} and i_{Lx} can be obtained as follows:

$$\begin{aligned} i_{Lkp}(t) &= i_{Ls}(t) = i_{Ls(min)} + \frac{1}{L_P} \int_{t_o}^t \frac{v_{Ls}}{N} dt \\ &= i_{Ls(min)} + \frac{v_{Ls}}{NL_P} (t - t_o) \end{aligned} \quad (8)$$

$$\begin{aligned} i_{Lx}(t) &= i_{Lx}(t_o) + \frac{1}{L_x} \int_{t_o}^t (-V_{o2}) dt \\ &= i_{Lx}(t_o) - \frac{V_{o2}}{L_x} (t - t_o) \end{aligned} \quad (9)$$

where the $i_{Ls(min)}$ is the minimum currents of CI. The switch S_1 , capacitor C_1 , and CI are in series, hence all the currents are same as given in (3). Furthermore, the energy in L_x will discharge through D_2 . Thus, the current i_{d2} is same as i_{Lx} as given in (3).

2) Mode-2: ($t_1 - t_2$) [see Fig. 5(b)]: At $t = t_1$, switch S_1 is turned-OFF and S_2 remains in the OFF state, so the converter enters the transition time (T_{d1}) interval. During the interval

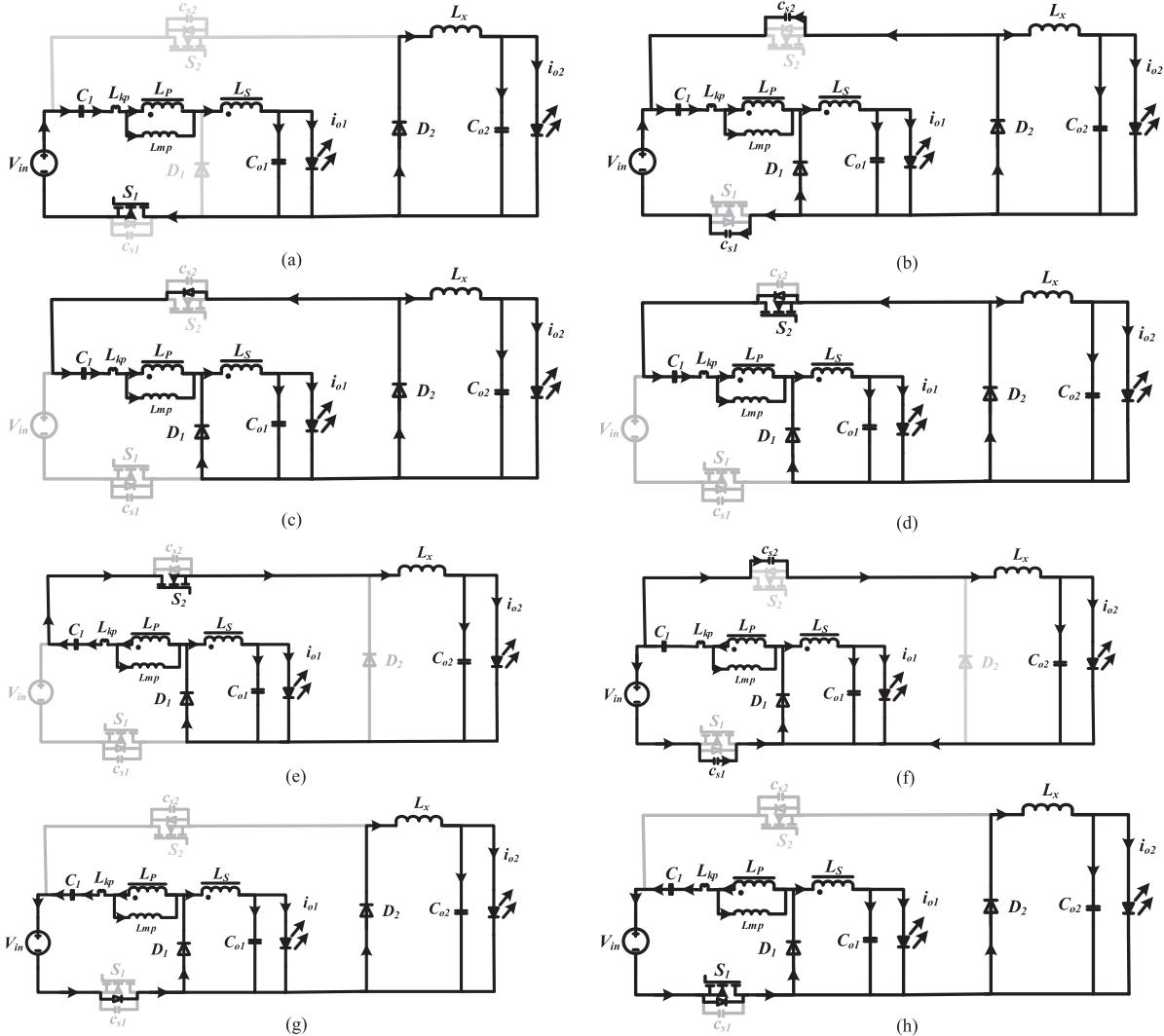


Fig. 5. Equivalent modes of the proposed LED driver: (a) Mode-1 [$t_0 - t_1$]; (b) mode-2 [$t_1 - t_2$]; (c) mode-3 [$t_2 - t_3$]; (d) mode-4 [$t_3 - t_4$]; (e) mode-5 [$t_4 - t_5$]; (f) mode-6 [$t_5 - t_6$]; (g) mode-7 [$t_6 - t_7$]; and (h) mode-8 [$t_7 - t_8$].

$t_1 - t_2$, junction capacitance (c_{s1}) charges from 0 V to V_{in} and junction capacitance (c_{s2}) discharges from V_{in} to 0 V. This mode ends when the charging and discharging of c_{s1} and c_{s2} are finished

$$c_{s1} = c_{s2} = \frac{(i_{L_{kp}} * t_{d1})}{(2 * V_{in})} = 437.5 \text{ pF.} \quad (10)$$

Since the time T_{d1} is very short, the current $i_{L_{kp}}$ during the period T_{d1} is assumed to be constant. In order to ensure ZVS junction capacitances, c_{s1} and c_{s2} should be less than the value obtained from (10).

3) Mode-3: ($t_2 - t_3$) [see Fig. 5(c)]: At $t = t_2$, the voltage across S_2 becomes zero, and the body diode of S_2 starts conduct to release the stored energy of L_{kp} , and, hence, the current $i_{L_{kp}}$ decreases while the current i_{L_S} continues to power the load-1 through D_1 . Also, the energy in the inductor L_x is continuously powering the load-2 through D_2 .

4) Mode-4: ($t_3 - t_4$) [see Fig. 5(d)]: This mode starts at $t = t_3$ by turning-ON the auxiliary switch S_2 . The conduction of body diode of S_2 in the previous mode ensures the ZVS turn-

ON of S_2 . During this mode, the energy of L_S powering load-1 through D_1 , while the energy in L_x is powering load-2 through D_2 . Since the voltage across inductors L_S and L_P are $-V_{o1}$ and $-v_{C1}$, respectively, the voltage across inductor L_x is $-V_{o2}$. From Fig. 4, it can be observed that the current i_{L_S} is increasing from $t_2 - t_4$ and the current i_{L_P} and i_{L_x} are decreasing from $t_2 - t_4$. Therefore, during the time interval t_2 to t_4 , currents i_{L_P} , i_{L_S} , and i_{L_x} can be obtained as follows:

$$i_{L_P}(t) = i_{L_P}(t_2) + \frac{1}{L_P} \int_{t_2}^t (-v_{C1}) dt \\ = i_{L_P}(t_2) - \frac{v_{C1}}{L_P} (t - t_2) \quad (11)$$

$$i_{L_S}(t) = i_{L_S}(t_2) + \frac{1}{L_S} \int_{t_2}^t (-V_{o1}) dt \\ = i_{L_S}(t_2) - \frac{V_{o1}}{L_S} (t - t_2) \quad (12)$$

$$\begin{aligned} i_{Lx}(t) &= i_{Lx}(t_2) + \frac{1}{L_x} \int_{t_2}^t (-V_{o2}) dt \\ &= i_{Lx}(t_2) - \frac{V_{o2}}{L_x} (t - t_2). \end{aligned} \quad (13)$$

The currents obtained in (11)–(13) are also applicable for mode-3, because the nature of currents i_{Lx} and i_{Lp} are decreasing from $t_2 - t_4$ and the nature of current i_{Ls} is increasing from $t_2 - t_4$.

5) *Mode-5: ($t_4 - t_5$) [see Fig. 5(e)]*: This mode begins when the L_x completely demagnetized and D_2 becomes reverse biased. Since S_2 is in ON-state, the L_x gets energized by i_{Lkp} and powering the load-2, while load-1 is powering by the freewheeling energy of L_S through D_1 . According to KVL, the voltage equation is given by

$$v_{Lx} = L_x \frac{di_{Lx}}{dt} = v_{C1} + v_{Lkp} + v_{Lp} - V_{o2}. \quad (14)$$

By assuming coupling coefficient as 1, the i_{Lx} can be derived from (14) as follows:

$$\begin{aligned} i_{Lx}(t) &= i_{Lx}(\text{min}) + \frac{1}{L_x} \int_{t_4}^t (v_{C1} + v_{Lp} - V_{o2}) dt \\ &= i_{Lx}(\text{min}) + \frac{(v_{C1} + v_{Lp} - V_{o2})}{L_x} (t - t_4). \end{aligned} \quad (15)$$

The voltage across v_{Ls} is $-V_{o1}$, thus the current i_{Ls} can be obtained as

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(t_4) + \frac{1}{L_S} \int_{t_4}^t (-V_{o1}) dt \\ &= i_{Ls}(t_4) - \frac{V_{o1}}{L_S} (t - t_4). \end{aligned} \quad (16)$$

6) *Mode-6: ($t_5 - t_6$) [see Fig. 5(f)]*: At $t = t_5$, switch S_2 is turned-OFF and S_1 remains in the OFF state, so the converter enters the transition time (T_{d2}) interval. During the interval $t_5 - t_6$, junction capacitance (c_{s2}) charges from 0 V to V_{in} and junction capacitance (c_{s1}) discharges from $(V_{in} - v_{C1} - V_{o1}/N)$ to 0 V. This mode ends when the charging and discharging of c_{s1} and c_{s2} are finished

$$c_{s1} = c_{s2} = \frac{(i_{Lkp} * t_{d2})}{(2 * V_{in})} = 625 \text{ pF}. \quad (17)$$

Since the time T_{d2} is very short, the current i_{Lkp} during the period T_{d2} is assumed to be constant. In order to ensure ZVS junction capacitances, c_{s1} and c_{s2} should be less than the value obtained from (17). The optimal value of junction capacitors c_{s1} and c_{s2} are selected from (10) and (17) in order to ensure ZVS. The switching devices used in this study is IRF 640-N, the junction capacitance of IRF640-N is 185 pF which is below the calculated values from (10) and (17), hence ensures the ZVS operation of both the switches.

7) *Mode-7: ($t_6 - t_7$) [see Fig. 5(g)]*: At $t = t_6$, the voltage across S_1 becomes zero and the body diode of S_1 conduct to carry i_{Lkp} . During this mode-7, the current i_{Ls} continuous to supply the load-1 through diode D_1 , while the energy in inductor L_x is powering to load-2 through diode D_2 .

8) *Mode-8: ($t_7 - t_8$) [see Fig. 5(h)]*: This mode starts at $t = t_7$ by turning-ON the auxiliary switch S_1 . The conduction of body diode of S_1 in the previous mode ensures the ZVS turn-ON of S_1 . During $t_7 - t_8$, the voltage across v_{Lp} and v_{Ls} are $V_{in} - v_{C1}$ and $-V_{o1}$, respectively. Furthermore, the energy in L_x will discharge through diode D_2 . Thus, the current i_{Lx} is same as i_{d2} . At $t = t_8$, the diode D_1 becomes reverse biased, thus completes the mode-8 and next cycle begins with switching period (T_S)

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(t_6) + \frac{1}{L_S} \int_{t_6}^t (-V_{o1}) dt \\ &= i_{Ls}(t_6) - \frac{V_{o1}}{L_S} (t - t_6) \end{aligned} \quad (18)$$

$$\begin{aligned} i_{Lp}(t) &= i_{Lp}(t_6) + \frac{1}{L_P} \int_{t_6}^t (V_{in} - v_{C1}) dt \\ &= i_{Lp}(t_6) + \frac{(V_{in} - v_{C1})}{L_S} (t - t_6) \end{aligned} \quad (19)$$

$$\begin{aligned} i_{Lx}(t) &= i_{Lx}(t_6) + \frac{1}{L_x} \int_{t_6}^t (-V_{o2}) dt \\ &= i_{Lx}(t_6) - \frac{V_{o2}}{L_x} (t - t_6). \end{aligned} \quad (20)$$

The current i_{Ls} is decreasing and i_{Lp} increasing during the time intervals $[t_6 - t_8]$, hence expression is given in (18) and (19) are valid. The current i_{Lx} is decreasing linearly during the time intervals $[t_6 - t_8]$, hence expression is given in (20) is valid.

In order to get the voltage gains of a ZVS-DOCIB converter the mode-1, mode-4, and mode-5 are considered by neglecting the delay time and leakage energy. The duty cycle of S_1 and S_2 are defined as δ_1 and δ_2 , respectively. In order to make analysis simple, the δ_1 is approximately equal to $(1 - \delta_2)$ by neglecting the delay time. The capacitor C_1 is selected [20] for recycling of the CI leakage energy so that to eliminate the switching spikes. By using volt-second balance of secondary winding, voltage gain ($G_{V_{o1}}$) from output terminal V_{o1} to input V_{in} can be obtained as follows:

$$\frac{k_p N (V_{in} - v_{C1} - V_{o1})}{(1 + k_p N)} \delta_1 T_S + (-V_{o1}) (1 - \delta_1) T_S = 0. \quad (21)$$

By assuming coupling coefficient as 1 (i.e., $k_p = 1$) and solving (21), the gain $G_{V_{o1}}$ is obtained as

$$G_{V_{o1}} = \frac{V_{o1}}{V_{in}} = \frac{N \delta_1}{(1 - \delta_1) + (1 + N)} = \frac{\left(\frac{N_2}{N_1}\right) \delta_1}{(1 - \delta_1) + \left(1 + \frac{N_2}{N_1}\right)}. \quad (22)$$

By assuming coupling coefficient as 1 and neglecting leakage inductance (i.e., $k_p = 1$), by solving (5) and (14), the demagnetizing duty cycle (δ_x) of an auxiliary inductor is calculated by using volt-second balance across L_x

$$(-V_{o2}) \delta_x T_S + (v_{LP} + v_{C1} - V_{o2})(1 - \delta_x) T_S = 0. \quad (23)$$

By solving (23), the voltage gain ($G_{V_{o2}}$) from output terminal V_{o2} to input V_{in} is obtained as

$$G_{V_{o2}} = \frac{V_{o2}}{V_{in}} = \frac{1 - \delta_x}{6}. \quad (24)$$

When switch S_2 is turned OFF, the voltage across auxiliary inductor is given by

$$v_{Lx} = V_{02} \quad (25)$$

$$\Delta i_{Lx} = \frac{V_{02}}{L_x} \delta_x T_S. \quad (26)$$

The minimum current of an auxiliary inductor is represented as

$$i_{Lx(\min)} = i_{Lx(\text{avg})} - \frac{\Delta i_{Lx}}{2} = \frac{V_{o2}}{R_{o2}} - \frac{V_{o2}}{2L_x} \delta_x T_S. \quad (27)$$

The L_x is designed by using (26), where Δi_{Lx} is the ripple current of the auxiliary inductor. By considering $V_{o2} = 7.2$ V, $T_S = 10 \mu\text{s}$, $\delta_x = 0.72$, and Δi_{Lx} is 7.5% of a load current (i_{o2}), from (26), the calculated value of auxiliary inductor is 1 mH.

The minimum current of a secondary winding is represented as

$$i_{Ls(\min)} = i_{Ls(\text{avg})} - \frac{\Delta i_{Ls}}{2} \quad (28)$$

where $i_{Ls(\text{avg})}$ and Δi_{Ls} are average and ripple value of secondary winding of CI, respectively. The average value of $i_{Ls(\text{avg})}$ and Δi_{Ls} can be calculated as follows:

$$i_{Ls(\text{avg})} = V_{o1}/R_{o1} \quad (29)$$

$$\Delta i_{Ls} = \frac{V_{o1}}{L_S} (1 - \delta_1) T_S. \quad (30)$$

Substituting (29) and (30) into (28), $i_{Ls(\min)}$ can be obtained as

$$i_{Ls(\min)} = \frac{V_{o1}}{R_{o1}} - \frac{V_{o1}}{2L_S} (1 - \delta_1) T_S. \quad (31)$$

By considering boundary-conduction mode, $i_{Ls(\min)} = 0$. The minimum value of L_S for continuous-conduction mode (CCM) can be obtained as follows:

$$L_S(\min) \geq \frac{R_{o1} (1 - \delta_1) T_S}{2}. \quad (32)$$

For a ZVS-DOCIB converter, the CI should be selected based on $L_S(\min)$ in order to ensure CCM operation. From (32), the value of L_S is selected as 1 mH and then, primary inductance is calculated by using a relation $N = \sqrt{(L_S/L_P)}$ and L_P is obtained to be 445 μH .

B. Design Considerations

To validate the proposed high step-down ZVS-DOCIB LED driver with load-1 of 25 W and load-2 of 5 W is designed and developed. A 150-V dc source is utilized for input supply to imitate the ac grid (V_{ac} of 110-V_{rms}) fed rectifier output. The output terminal voltage/current (V_{o1}/i_{o1}) of load-1 is set to 36 V/0.7 A. The load-1 modeled with ten LEDs connected in series, and each LED is impressed by 3.6 V and carry a current of 0.7 A. The output terminal voltage/current (V_{o2}/i_{o2})

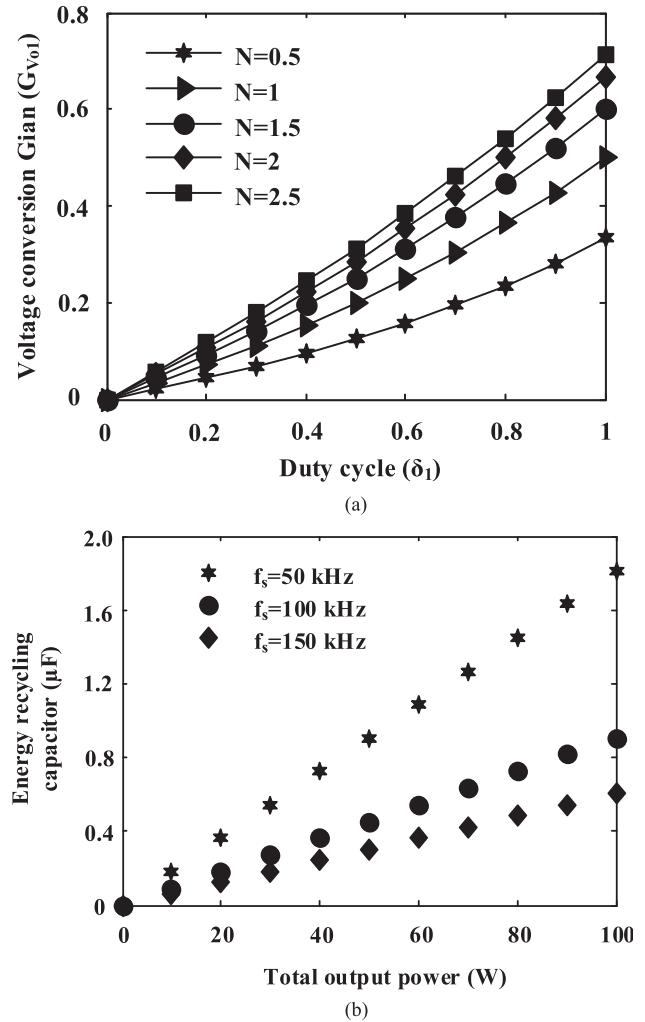


Fig. 6. (a) Voltage gain ($G_{V_{o1}}$) versus duty cycle. (b) Capacitor C_1 versus total output power.

of load-2 is set to 7.2 V/0.7 A. The load-2 modeled with two LEDs connected in series, and each LED is impressed by 3.6 V and carry a current of 0.7 A. Furthermore, the proposed ZVS-DOCIB converter is operated with a switching frequency 100 kHz, and coupling coefficient is considered to be 1 ($k_p = 1$) by assuming that the proposed topology has good leakage energy recycling effect. Fig. 6(a) illustrates the characteristic curves of voltage gain $G_{V_{o1}}$ on δ_1 for different values of N . From Fig. 6(a), the turns ratio (N) of CI selected as $N = 1.5$ with operating parameters of $V_{in} = 150$ V and $V_{o1} = 36$ V. According to (24), the demagnetizing duty cycle (δ_x) of L_x can be calculated as $\delta_x = 0.72$ for $V_{in} = 150$ V and $V_{o2} = 7.2$ V.

C. Switching Device Selection

The idealized waveforms as depicted in Fig. 4 would confirm that the switch S_1 and auxiliary switch S_2 are complimentary to each other with a small delay time between them. The maximum voltage across S_1 and S_2 can be represented as

$$v_{ds1(\max)} = V_{in} = 150 \text{ V} \text{ and } v_{ds2(\max)} = V_{in} = 150 \text{ V}. \quad (33)$$

From (33), the maximum voltage across the main switch S_1 and auxiliary switch S_2 are not a function of δ_1 and δ_2 , if the input voltage V_{in} and turns ratio N fixed. The devices (S_1 and S_2) must be selected higher than that of the theoretical values of voltage ratings. Hence, two IRF640-N MOSFETs with a voltage rating of 200 V are used as switching devices.

D. Energy Recycling Capacitor

The capacitor C_1 is connected between the input source and CI to transfer the energy from source to output along with the CI leakage energy [20]. Thus, capacitance C_1 can be calculated as

$$C_1 \geq \frac{2P_{o1,\text{rated}}}{(v_{C1})^2 f_s} = \frac{2 * 25.2}{(47)^2 * 100 * 10^3} = 0.228 \mu\text{F}. \quad (34)$$

The value of C_1 should be large enough to avoid the resonance with the leakage inductor. Hence, the C_1 value of 1 μF is used which is approximately five times higher than the designed value. Fig. 6(b) depicts the characteristic curves of C_1 versus output power for different switching frequencies. It can be noticed from Fig. 6(b), that the size of C_1 decreases significantly even for the increased output power rating of a converter at higher switching frequencies.

E. Output Capacitors Design

In the proposed ZVS-DOCIB converter, the charge variation (ΔQ_{o1}) of the capacitor (C_{o1}) in load-1 is represented as follows:

$$\Delta Q_{o1} = C_{o1} \Delta V_{co1} = (V_{o1} / R_{o1}) (1 - \delta_1) (T_S) \quad (35)$$

$$C_{o1} = (1 - \delta_1) (V_{o1}) / (R_{o1} f_s \Delta V_{co1}). \quad (36)$$

By substituting the values $\delta_1 = 0.475$, $R_{o1} = 51.4 \Omega$, $V_{o1} = 36$, $\Delta V_{co1} = 1\%$, and $f_s = 100 \text{ kHz}$ in (36), the value of C_{o1} is obtained to be 10 μF .

The load-2 output capacitor (C_{o2}) design is mainly on the basis of auxiliary inductor ripple current (Δi_{Lx}) and output capacitor voltage ripple (ΔV_{co2}), which is expressed as follows:

$$C_{o2} = \frac{\Delta i_{Lx} T_s}{8 \Delta V_{co2}}. \quad (37)$$

By considering $\Delta V_{co2} = 1\%$ of V_{o2} , $\Delta i_{Lx} = 52.5 \text{ mA}$, and $f_s = 100 \text{ kHz}$, from (37), the value of C_{o2} is obtained to be 1 μF .

The total efficiency (η) of the proposed converter is defined as the ratio of the output power to input power.

$$\eta = \frac{V_{o1} i_{o1} + V_{o2} i_{o2}}{V_{in} i_{in}} = \frac{P_{o1} + P_{o2}}{P_{in}} \quad (38)$$

where $P_{o1} = V_{o1} i_{o1}$ and $P_{o2} = V_{o2} i_{o2}$ are output power of load-1 and load-2, respectively.

III. DIMMING CONTROL

The dimming control is often needed to control the illumination level of LED light for the human need to create a comfortable environment. Moreover, dimming operation results in reduced power consumption and produces less heat, hence

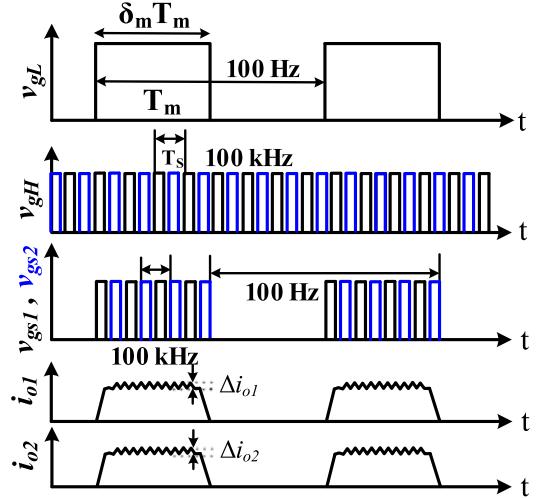


Fig. 7. DPWM control scheme.

increases the LED life span and optimizes the running cost. Therefore, dimming control is essential in LED lighting application. The illumination of LED is directly related to its average current. Amplitude modulation (AM) and pulse width modulation (PWM) methods are used to control the illumination of LED [21]–[26]. AM dimming can be realized by adjusting the duty cycle of the PWM signal, but it leads to color discrepancy due to LED current variation at different illumination levels [21]–[23]. Therefore, AM dimming control is not appropriate for the application wherein constant color stability is an essential requirement. A low-frequency PWM dimming control can be used to prevent color instability of LED light [24]–[26].

In this proposed study, a double pulse width modulation (DPWM) dimming control technique is adopted to control the illumination level of LED light, as illustrated in Fig. 7. With DPWM control, when low-frequency pulse signal (v_{gL}) is high, the switches S_1 and S_2 are triggered with a high-frequency pulse. Consequently, when v_{gL} is low, the switches S_1 and S_2 are turned-OFF for a long duration, where in Fig. 7, T_m and δ_m are switching period and duty cycle of low-frequency dimming signal, respectively. By varying the δ_m from 35% to 100%, the ZVS operation is achieved and also, illumination of LED light is adjusted by controlling the average output current. According to Energy Star Program Requirements Product Specifications for Luminaires (Light Fixtures) Version 1.0 (Effective date: Oct. 1, 2011), the preferable dimming level is from (35% to 100%) [27].

IV. IMPLEMENTATION AND RESULT DISCUSSION

A. Simulation Results and Analysis

Simulation and detailed analysis of the proposed ZVS-DOCIB converter in Fig. 3 is performed using the MATLAB/Simulink software. Table I describes the specifications and design parameters used for simulation analysis. Figs. 8 and 9 illustrate the steady-state simulation waveforms of the ZVS-DOCIB LED driver. From Fig. 8(a) and (b), it can be noticed that the turn-OFF switching spikes across the main switch

TABLE I
PARAMETERS USED IN SIMULATION OF THE PROPOSED
ZVS-DOCIB LED DRIVER

Parameter	V_{in}	f_s	C_1	P_o	L_P	L_S	L_x	C_{o1}	C_{o2}
Value	150 V	100 kHz	1 μ F	30 W	445 μ H	1 mH	1 mH	10 μ F	1 μ F

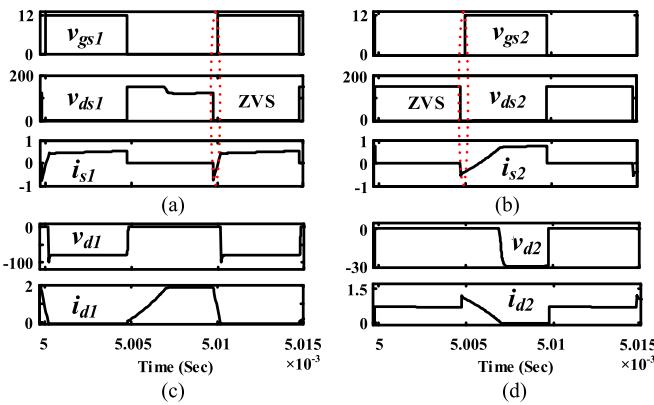


Fig. 8. Simulation waveforms of switching devices: (a) v_{gs1} , v_{ds1} , and i_{s1} ; (b) v_{gs2} , v_{ds2} , and i_{s2} ; (c) v_{d1} and i_{d1} ; and (d) v_{d2} and i_{d2} .

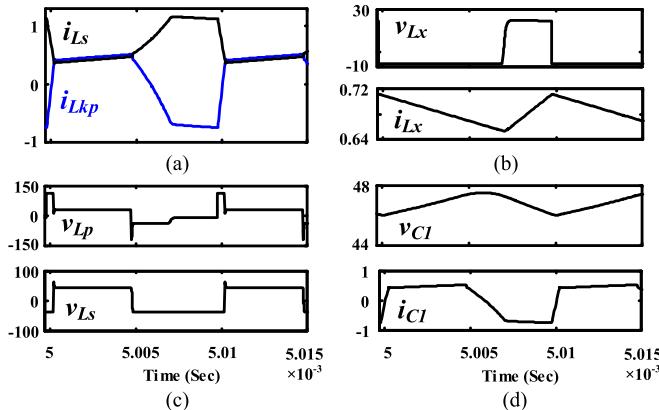


Fig. 9. Simulation waveforms of CI , L_x , and C_1 : (a) i_{Lkp} and i_{Ls} ; (b) v_{Lx} and i_{Lx} ; (c) v_{Lp} and v_{Ls} ; and (d) v_{C1} and i_{C1} .

(S_1) and auxiliary switch (S_2) are effectively eliminated and operating with ZVS which results in reduced device voltage ratings and switching losses, respectively. Fig. 8(c) and (d) illustrates the v_{d1} , i_{d1} of diode D_1 and v_{d2} , i_{d2} of diode D_2 , respectively. Fig. 9(a)–(d) shows the steady-state waveforms of leakage current/secondary current (i_{Lkp} / i_{Ls}), auxiliary inductor voltage/current (v_{Lx} / i_{Lx}), primary voltage/secondary voltage (v_{Lp} / v_{Ls}), and energy recycling capacitor voltage/current (v_{C1} / i_{C1}), respectively. Fig. 10(a) and (b) depicts output voltages/currents (V_{o1} / i_{o1}) of load-1 and (V_{o2} / i_{o2}) of load-2 at 100% of dimming. Likewise Fig. 11(a) and (b) depicts output voltages/currents (V_{o1} / i_{o1}) of load-1 and (V_{o2} / i_{o2}) of load-2 at 80% of dimming. From Fig. 11(a) and (b), it is evident that the average output of each load is controlled by varying the duty ratio of v_{gL} .

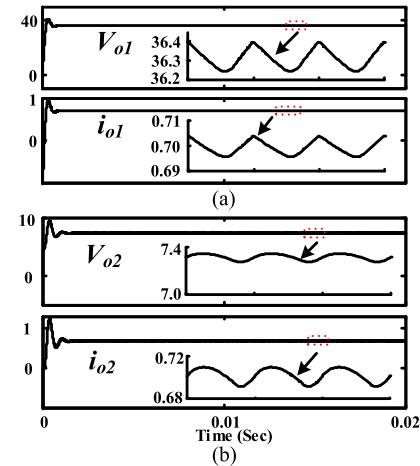


Fig. 10. Simulation waveforms of output voltages/currents at 100% dimming: (a) V_{o1} and i_{o1} . (b) V_{o2} and i_{o2} .

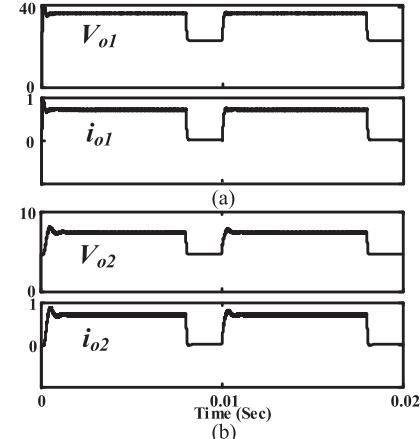


Fig. 11. Simulation waveforms of output voltages/currents at 80% dimming: (a) V_{o1} and i_{o1} . (b) V_{o2} and i_{o2} .

B. Experimental Results and Analysis

In order to validate simulation and analysis of the ZVS-DOCIB LED driver, a 30 W ($P_{o1} = 25$ W and $P_{o2} = 5$ W) prototype is developed and tested experimentally. The specification and designed parameters used for experimental setup are listed as follows.

- 1) Input voltage source: $V_{in} = 150$ V.
- 2) Switching frequency: $f_s = 100$ kHz.
- 3) Load-1 output voltage: $V_{o1} = 36$ V.
- 4) Load-2 output voltage: $V_{o2} = 7.2$ V.
- 5) CI: $L_P = 447 \mu$ H; $R_P = 17 \text{ m}\Omega$; $L_S = 1.01$ mH; $R_S = 56 \text{ m}\Omega$; $N = 1.5$; PQ32/30 core.
- 6) Auxiliary inductor: $L_x = 1$ mH, $R_x = 55 \text{ m}\Omega$; PQ26/20 core.
- 7) Energy transferring capacitor: $C_1 = 1 - \mu$ F/450 – V film capacitor.
- 8) Switching devices: S_1, S_2 – IRF640-N (200 V/18 A, $R_{ds(on)} = 150 \text{ m}\Omega$), D_1, D_2 : BVY29 (500 V/9 A, $V_F = 0.9$ V).
- 9) Output capacitors: $C_{o1} = 10 \mu$ F/50 V, $C_{o2} = 1 \mu$ F/25 V.

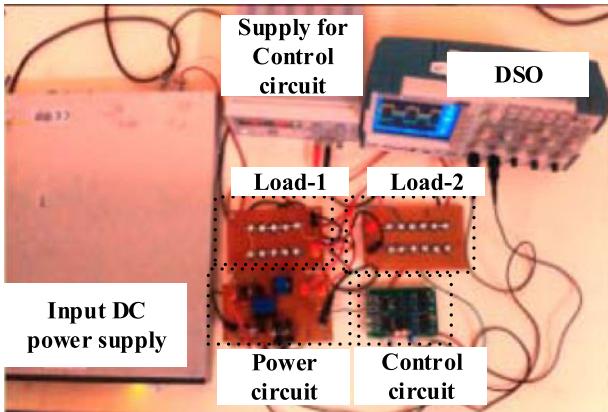


Fig. 12. Experimental setup of the proposed ZVS-DOCIB LED driver.

The CI and auxiliary inductor of the converter are made with PQ 32/30 and PQ 26/20 ferrite cores, respectively. The primary winding (L_P) of CI is made with 14 turns (SWG-30 wire, four parallel wires) and secondary winding (L_S) of CI is made with 21 turns (SWG-30 wire, eight parallel wires). The auxiliary inductor is made with 20 turns (SWG-30 wire, four parallel wires). Fig. 12 shows the experimental prototype of the proposed LED driver. The experimental circuit consists of MOSFETs with part number IRF640-N in the power circuit used as switching devices. A programmable dc power supply is used as an input dc power source to feed LED driver. The two outputs of a converter are connected to LED load, in which load-1 is configured by connecting ten LEDs in series, and load-2 is configured by connecting two LEDs in series, respectively. The high-frequency (100 kHz) switching pulses for the proposed ZVS-DOCIB LED driver is generated by using the phase-shift resonant controller IC UC3875. The low-frequency (100 Hz) pulse is generated by using SG3525 PWM IC. Driver IR2110 is used for driving switching devices. All experimental waveforms are captured by using Tektronix DPO 3034.

Figs. 13–16 illustrate experimental waveforms of various voltages and currents of the ZVS-DOCIB LED driver with rated specifications. Fig. 13(a) and (b) depicts the gating signals, voltage, and current waveforms of main switch S_1 and auxiliary switch S_2 , respectively. It can be noticed from Fig. 13(a) and (b) that the maximum voltage stress on switch S_1 and auxiliary switch S_2 is clamped to input voltage (i.e., $v_{ds1(\max)} = v_{ds2(\max)} = V_{in} = 150$ V). Fig. 13(c) and (d) depicts the voltage and current waveforms of diodes D_1 and D_2 , respectively. As can be observed from experimental results, the voltage spikes and oscillation in waveforms are mainly caused due to resonance between stray inductance and parasitic capacitance of switching devices. Fig. 14(a) shows current $i_{L_{kp}}$ and current i_{L_s} waveforms of CI. Fig. 14(b) depicts the current i_{L_x} and voltage v_{L_x} waveforms of an auxiliary inductor L_x . Fig. 14(c) shows the voltage waveforms of primary and secondary windings of CI. Fig. 14(d) shows the voltage and current waveforms of capacitor C_1 . It can be observed from Fig. 14(a) and (d), that the current through C_1 is same as current $i_{L_{kp}}$ since C_1 and leakage inductance L_{kp} are in series. Fig. 15(a)

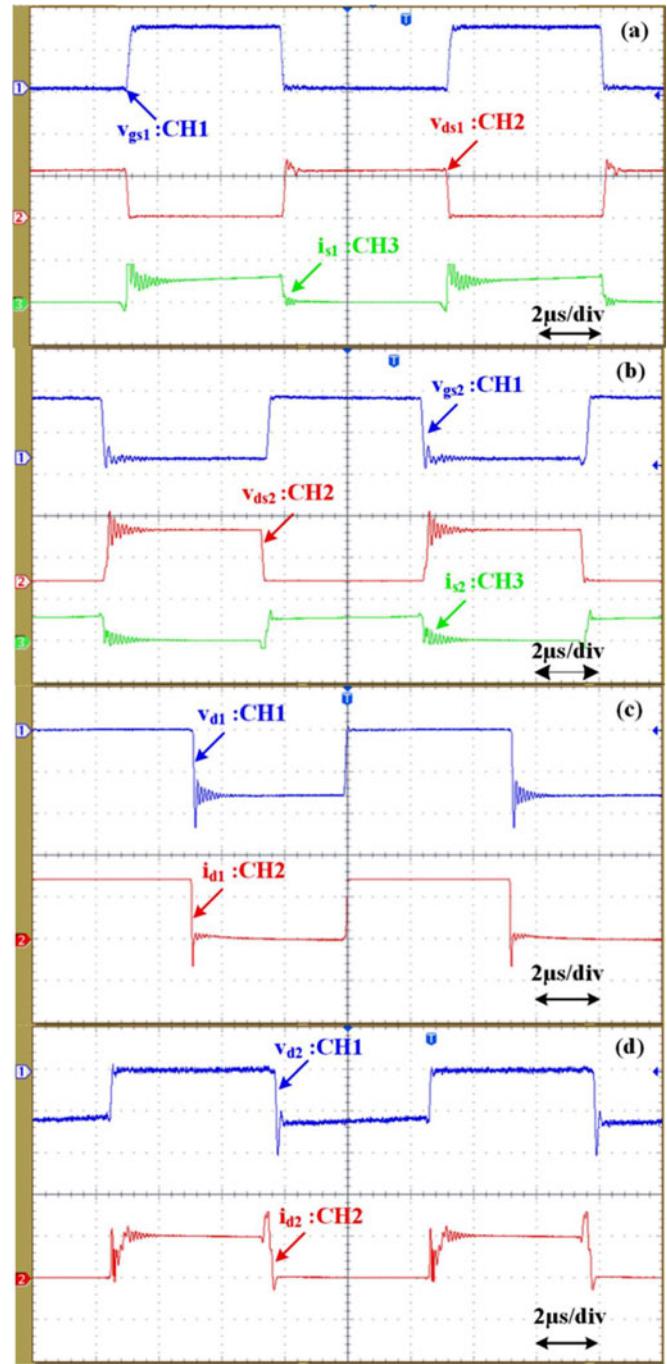


Fig. 13. Experimental waveforms of switching devices: (a) v_{gs1} [10 V/div], v_{ds1} [125 V/div] and i_{S1} [1 A/div]; (b) v_{gs2} [10 V/div], v_{ds2} [125 V/div] and i_{S2} [1 A/div]; (c) v_{d1} [50 V/div] and i_{d1} [500 mA/div]; and (d) v_{d2} [12.5 V/div] and i_{d2} [500 mA/div].

and (b) depicts the output voltage and current waveforms of load-1 and load-2, respectively, with 100% dimming. The enlarged waveforms of gating signals and voltages of the switch (S_1) and switch (S_2) are shown in Fig. 16(a) and (b), respectively. From Fig. 16(a) and (b), it is clearly shown that the ZVS operation of the main switch (S_1) and auxiliary switch (S_2). As a result of zero voltage turn-ON of S_1 and S_2 , switching transient voltage spikes are effectively eliminated. Also, a significant

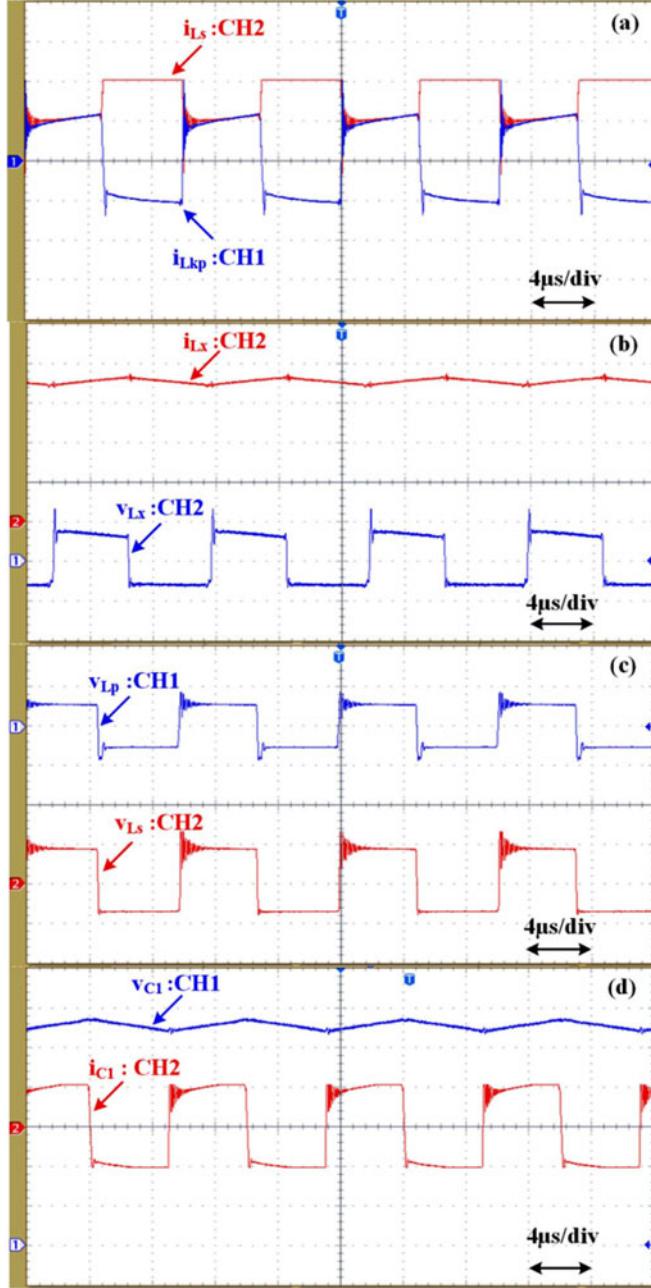


Fig. 14. Experimental waveforms of CI, L_x and C_1 : (a) i_{Lkp} [500 mA/div] and i_{Ls} [500 mA/div]; (b) v_{Lx} [12.5 V/div] and i_{Lx} [200 mA/div]; (c) v_{Lp} [50 V/div] and v_{Ls} [50 V/div]; and (d) v_{C1} [7.5 V/div] and i_{C1} [500 mA/div].

reduction in switching loss, and, hence, increases the converter efficiency. The experimental results show close agreement with theoretical/simulation counterparts.

Fig. 17(a) and (b) depicts the experimental waveforms of low-frequency signal (100 Hz), high-frequency signals (100 kHz), and combination of low- and high-frequency signals at 50% and 80% of dimming, respectively. Figs. 18 and 19 illustrate the output load voltage and current waveforms when DPWM drives LED lamp at 50% and 80% of rated output current. When low-frequency dimming signal v_{gL} is high, the proposed ZVS-DOCIB converter operates with high frequency and regulates

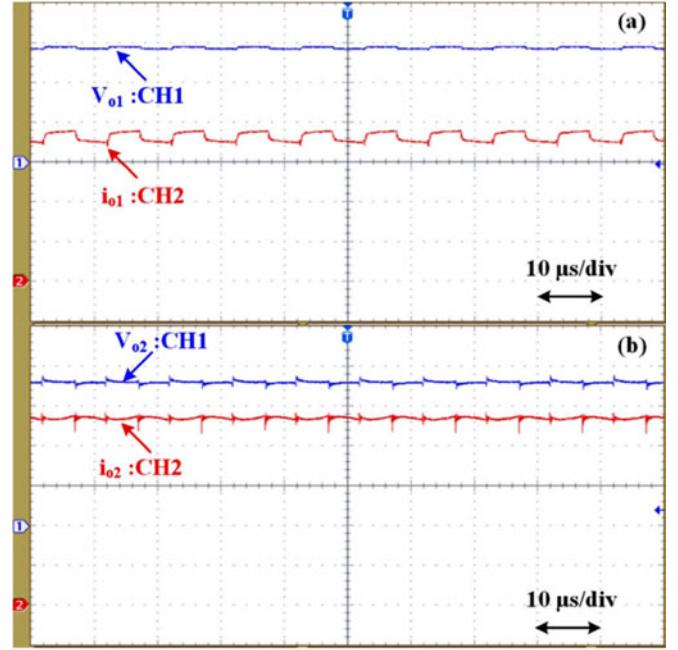


Fig. 15. Experimental waveforms of output voltages/currents at 100% dimming: (a) V_{01} [12.5 V/div] and i_{01} [200 mA/div], (b) V_{02} [2 V/div] and i_{02} [150 mA/div].

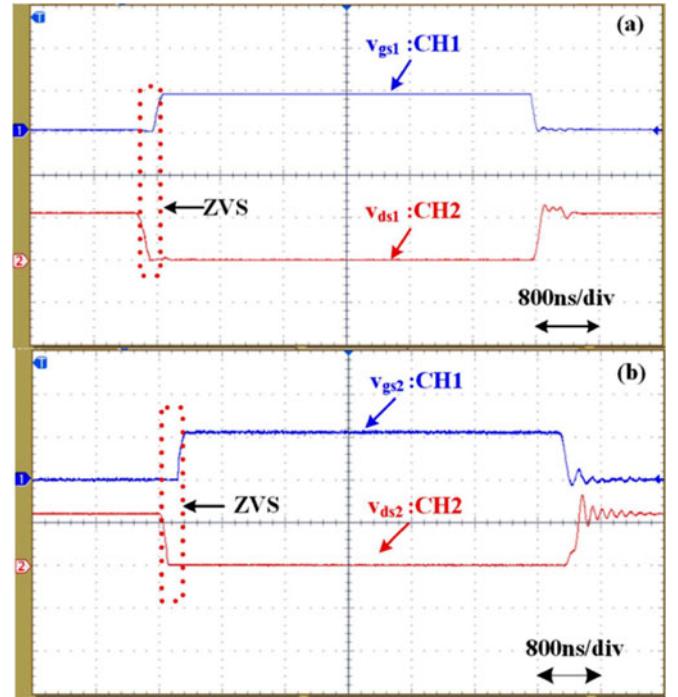


Fig. 16. Experimental enlarged waveforms of switch S_1 , S_2 : (a) V_{gs1} [12.5 V/div], V_{ds1} [125 V/div]. (b) V_{gs2} [12.5 V/div], V_{ds2} [125 V/div].

the output current. When v_{gL} is low, the ZVS-DOCIB converter is disconnected from an input source and lamp currents of load-1 and load-2 falls to zero, and, hence, output capacitors C_{o1} and C_{o2} discharged to 23 and 4.6 V, respectively. Further from Figs. 18 and 19, it can be observed that the oscillations occurred in load voltages and currents of both the loads at every instant

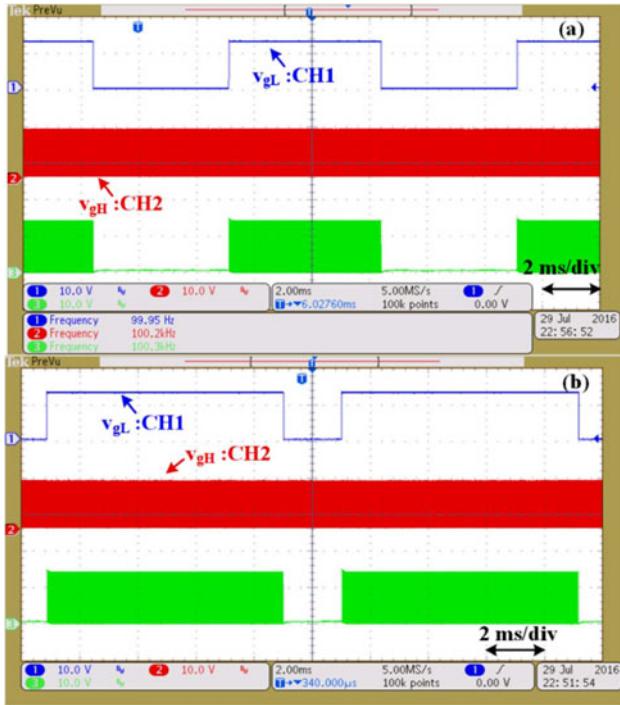


Fig. 17. Experimental switching pulses: (a) 50% dimming and (b) 80% dimming.

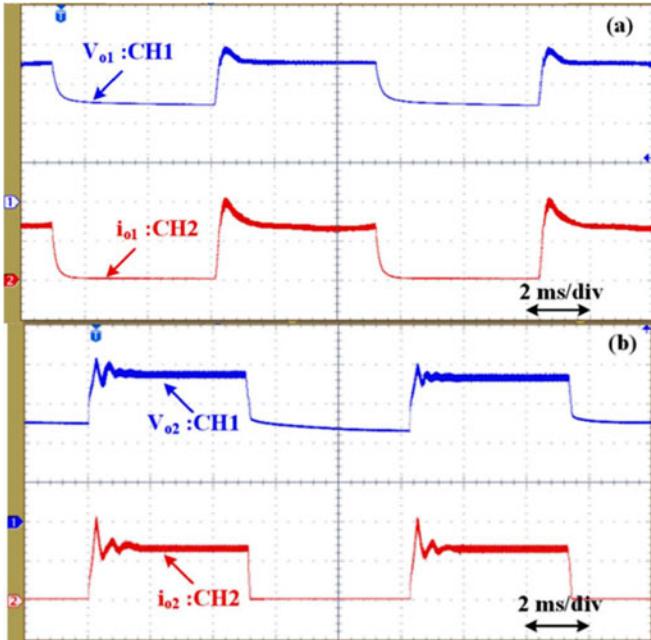


Fig. 18. Experimental waveforms of output voltages/currents at 50% dimming: (a) V_{o1} [10 V/div] and i_{o1} [500 mA/div]. (b) V_{o2} [2 V/div] and i_{o2} [500 mA/div].

of dimming due to LC filter at load side. However, this can be overcome by reducing the inductance value, but it may lead to high ripple in load currents.

Fig. 20 demonstrates the efficiency comparison of the proposed ZVS-DOCIB converter over a converter reported in [19]. The efficiency of the proposed converter at rated load condition

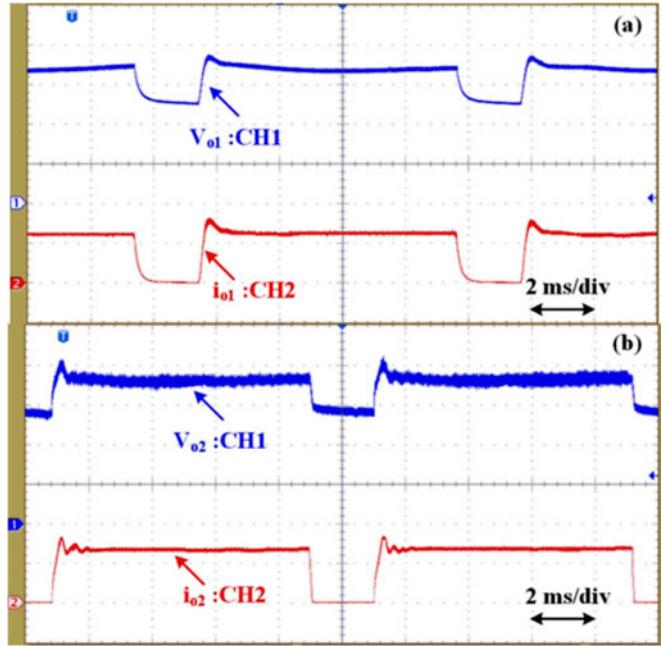


Fig. 19. Experimental waveforms of output voltages/currents at 80% dimming: (a) V_{o1} [10 V/div] and i_{o1} [500 mA/div]. (b) V_{o2} [2 V/div] and i_{o2} [500 mA/div].

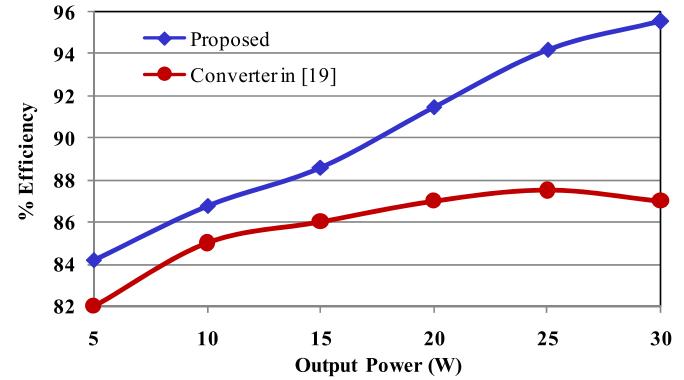


Fig. 20. Measured efficiency versus load power.

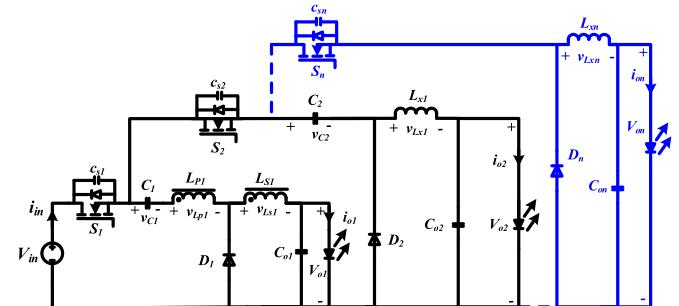


Fig. 21. Extended configuration of the proposed converter for multiple loads.

is 95.5%, whereas the converter in [19], the maximum efficiency at rated load condition is 87.5%. The major advantages of the proposed converter are: achieves high step-down ratio, effective recycling of leakage energy, ZVS operation of both the

TABLE II
COMPARATIVE STUDY OF ZVS-DOCIB CONVERTER WITH OTHER WORKS IN THE LITERATURE

	Narasimharaju <i>et al.</i> [6]	Hwu and Yau [9]	Hwu <i>et al.</i> [14]	Hwu <i>et al.</i> [15]	Huang <i>et al.</i> [17]	Wu <i>et al.</i> [18]	Luo <i>et al.</i> [19]	Proposed
Method of switching	Hard switching	Soft switching	Soft switching	Soft switching	Hard switching	Hard switching	Hard switching	Soft switching
MOSFETs	2	4	3	3	2	10	3	2
Diodes	0	1	0	0	2	0	3	2
Inductors	0	1	0	1	1	1	3	1
ClIs	1	0	1	1	0	1	0	1
Capacitors	2	3	2	3	2	4	2	3
Component count	5	9	6	8	7	16	11	9
Input Voltage	$V_{in} = 200 \text{ V}$	$V_{in} = 24 \text{ V}$	$V_{in} = 48 \text{ V}$	$V_{in} = 48 \text{ V}$	$V_{in} = 5 \text{ V}$	$V_{in} = 48\text{--}85 \text{ V}$	$V_{in} = 400 \text{ V}$	$V_{in} = 150 \text{ V}$
Output voltages	$V_{o1} = 24$	$V_{o1} = 12$	$V_{o1} = 3.3$	$V_{o1} = 3.3$	$V_{o1} = 1.8; V_{o2} = 3.3$	$V_{o1} = 10 \text{ V}; V_{o2} = 5 \text{ V}; V_{o3} = 3.3 \text{ V}$	$V_{o1} = 28.57 \text{ V}; V_{o2} = 28.57 \text{ V}; V_{o3} = 28.57 \text{ V}$	$V_{o1} = 36 \text{ V}; V_{o2} = 7.2$
Output ports	1	1	1	1	2	3	3	2
Output power	400 W	120 W	49.5 W	33 W	1.56 W	96.6 W	$3 \times 10 = 30 \text{ W}$	30 W
%Efficiency	93.3	93.25	90.2	92.2	—	91.8	87	95.5

switching devices, reduction in switching losses, and increased efficiency.

The proposed topology can be extended for multiple loads as illustrated in Fig. 21. When all the switches of multiload converter operated with equal duty cycle, the input voltage of each cell is balanced, and the output current is identical. However, practically it is not exactly possible to turn-ON and turn-OFF these switches with equal duty because that may lead to uneven voltage stress. Also, unbalanced sharing of load current that makes the design of loop compensation difficult. Therefore, the reliability of the proposed circuit may be reduced by extending the circuit topology from two-channel output to multiple outputs. Furthermore, the driver complexity will increase due to a floating switch for each stage particularly in the case of more than two loads. Fig. 21 illustrates the extended configuration of the proposed converter for multiple loads.

A comparative study of the ZVS-DOCIB converter with similar researchers is summarized in Table II. It can be noticed from Table II that the ZVS-DOCIB converter requires less switching devices to drive multiloads, and, hence, it can be extended to any number of loads. Also, ZVS-DOCIB utilizes ClIs instead of using two separate inductors that result in several advantages, such as provide high step-down conversion, reduction in device rating, compact size, cost effective, and increased overall efficiency. Thus, the ZVS-DOCIB converter would be an ideal choice for multiload applications.

V. CONCLUSION

This study proposes a high step-down ZVS-DOCIB converter for LED lighting loads. In this paper, the detailed operating modes, design guidelines, the simulation analysis, and experimental results are provided to verify the effectiveness of the proposed converter. Also, an apt comparative study of the proposed converter over other converters reported is provided to confirm and justify the benefits of the ZVS-DOCIB converter. Experimental results show close agreement with the simulation

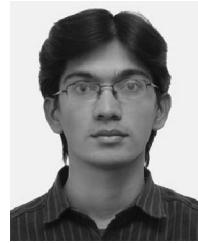
counterparts. The various benefits of the proposed ZVS-DOCIB converter are described as follows.

- 1) The step-down conversion ratio is extended by using CI.
- 2) Energy transferring capacitor to utilize the leakage energy of the CI and to reduce turn-OFF switching voltage spikes.
- 3) It requires only two switches to drive two loads, and both the switches are operating with ZVS property.
- 4) Reduced switching losses and increased efficiency due to ZVS operation.
- 5) The efficiency of the proposed converter is 95.5% at rated load.
- 6) Regulation of average output current by using dimming control.
- 7) Proposed converter can be extended to multiple loads of different voltage levels with less switch count, hence compact size and cost effective for multiload applications.

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Ramanjaneya Reddy U received the B.Tech. degree in electrical and electronics engineering from Raja Mahendra College Of Engineering, Hyderabad, India, in 2009, and the M.E. degree from the University Visvesvaraya College of Engineering, Bangalore, India, in 2012. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering, National Institute of Technology, Warangal, India.

His research interests include power electronic converters and its applications.



Narasimharaju B. L (S'10–M'12–SM'16) received the B.E. and M.E. degrees in electrical engineering from the University Visvesvaraya College of Engineering, Bangalore, India, in 1999 and 2002, respectively, and the Ph.D. degree from IIT Roorkee, Roorkee, India, in 2012.

He worked as a Project Trainee with ABB Bangalore from March 2001 to August 2001 and from 2001 to March 2002 with LRDE, India. He was a Teaching Assistant with UVCE, Bangalore, from April 2002 to August 2003. From August 2003 to May 2012, he was with the Faculty of Electrical Engineering, MIT Manipal University, India. He is currently a Faculty of Electrical Engineering, National Institute of Technology, Warangal, India. His research interest includes power electronics and its applications.