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A Wide Range Soft Switched Interleaved Boost Integrated L-L Type Full-Bridge DC-DC Converter

V.K. Satyakar Veeramallu
Department of Electrical Engineering
NIT Warangal
Warangal, India
vvk.satyakar@gmail.com

Porpandiselvi S
Department of Electrical Engineering
NIT Warangal
Warangal, India
selvi@nitw.ac.in

K. Ashok Kumar
Department of Electrical Engineering
NIT Warangal
Warangal, India
akk0107_jrf@nitw.ac.in

Narasimharaju B.L.
Department of Electrical Engineering
NIT Warangal
Warangal, India
blnraju@nitw.ac.in

***Abstract*—A new wide range soft switched interleaved boost integrated full-bridge DC-DC converter for PV and fuel cell applications is proposed in this paper. Fixed frequency PWM control is employed for output regulation. The proposed configuration has advantages such as soft switching across devices, wide ZVS range and very low input current ripple. The proposed configuration is simulated and corresponding results are discussed for a load of 200 W for 100% and 10% full-load conditions with input voltages of 22 V and 41 V.**

***Index Terms*—High-frequency isolated DC-DC converter, ZVS, Fixed frequency PWM control, Fuel cells converters, PV systems**

I. Introduction

Nowadays, fuel cell and photo-voltaic (PV) fed DC-DC converters are gaining importance due to their enormous advantages and requirement. Isolated DC-DC converters are mostly used for these applications [1]. To make the converters compact in size, these converters are operated with high switching frequency. Thus, makes soft switching an essential requirement to reduce switching losses and cooling arrangement. For applications with fuel cells or PV input, there is a requirement of wide soft switching as the input voltage varies widely. Several authors proposed wide gain soft switched converters for these types of applications [2]–[5]. However, they have limitations like more switch count, complex control, etc. Current fed converters have desirable features for PV or fuel cell applications. In [6], a wide zero voltage switching (ZVS) L-L type active clamp current fed converter is proposed. Even though it has wide ZVS, the input ripple is high, thus increases the input filter size. In [7], an L-L type active clamp full-bridge converter is proposed, which requires an additional auxiliary clamping circuit. As the voltage of PV or Fuel cells is low, boost converters are integrated with these converters [8], in order to increase the voltage gain and further reduce the primary conduction losses. Thus, in this paper, an interleaved boost integrated L-L type full-bridge isolated converter is proposed, which retains the benefits of using current-fed converters along with wide ZVS capability, reduced input current ripple and switching devices. Hence, well suitable for PV and Fuel cell applications. The proposed converter is simulated for 200 W, 350 V with input voltages of 22 V and 41 V at full-load and light-load conditions.

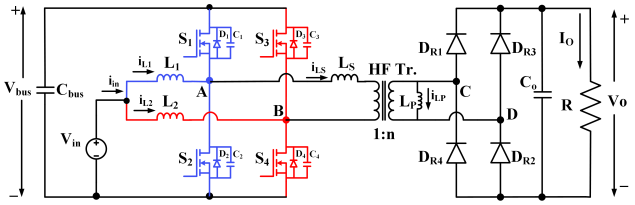

Fig. 1. Circuit diagram of the proposed configuration

II. Proposed Converter

Proposed configuration is the integration of interleaved boost converter and isolated full-bridge converter, which reduces the input current ripple along with an increase in voltage gain. The additional inductor, in parallel with the secondary winding of the transformer, aids for ZVS at light loads. Fig. 1 shows the circuit diagram of the proposed configuration. The leakage and magnetizing inductances of the transformer are included with series inductor, L_S and parallel inductor, L_P respectively. Fig. 2 shows the operating waveforms and modes of operation. The gating signals with duty cycle D of more than 50% are applied to S_2 and S_4 with a phase shift of 180° having a small overlap. The overlap angle depends upon D. The gate pulses of S_1 and S_3 are complementary to S_2 and S_4 respectively as shown in Fig. 2a. The inverter output voltage v_{AB} is a quasi square wave whose magnitude and width depends upon D. Thus, by controlling D, the output voltage can be regulated. The modes of operation are analyzed

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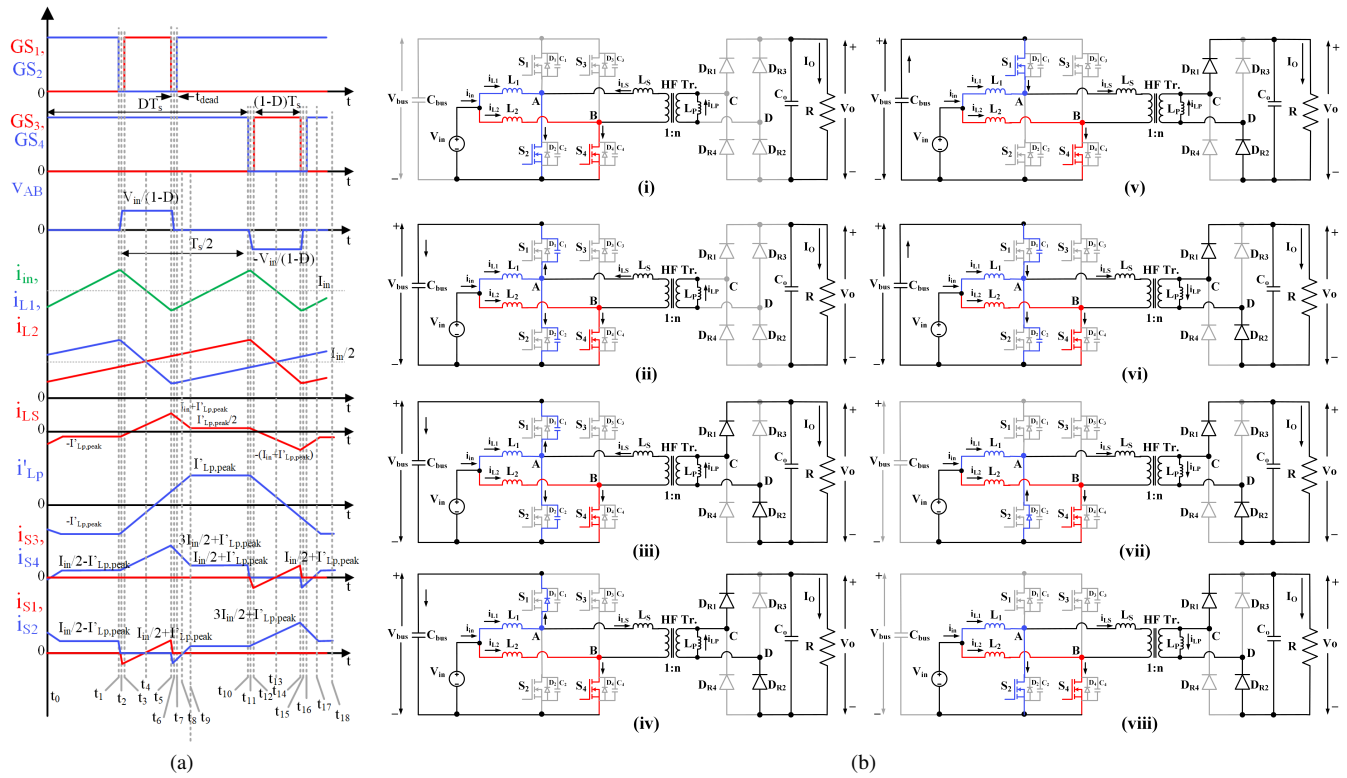


Fig. 2. (a) Model waveforms (b) Modes of operation for half-cycle

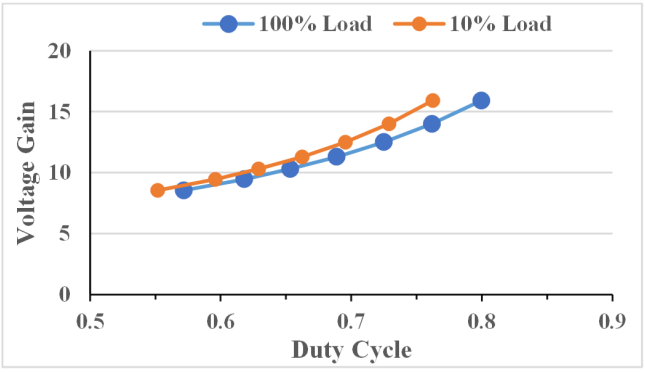


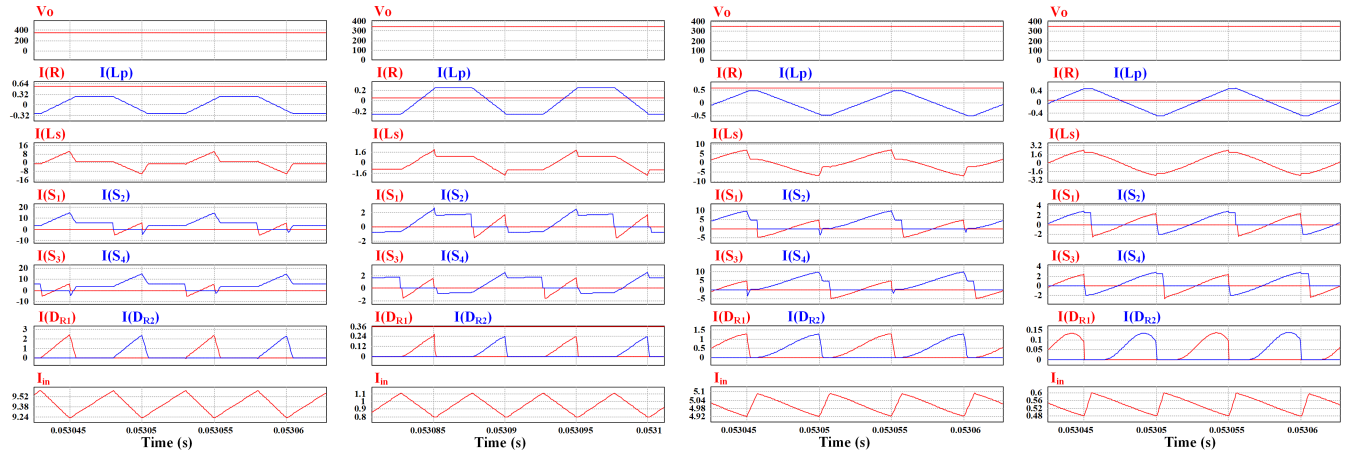
Fig. 3. Gain curve with Duty Cycle variation for 100% and 10% Loads

for one half-cycle, whereas similar analysis can be carried out for the other half-cycle with other symmetrical devices.

A. Modes of operation

In mode-1 (t_0-t_1) [Fig. 2(b)(i)], switches S_3 and S_4 are conducting. The boost inductors get magnetized. D_{R1} to D_{R4} are reverse biased and the output load is fed from output capacitor, C_o. Thus, L_P is shorted and hence, a constant current, $-I_{Lp,peak}$ flows through it and its corresponding reflected current, $-I'_{Lp,peak}$ flows through L_S.

Mode-2 (t_1-t_2) [Fig. 2(b)(ii)] starts when S_3 is turned OFF at $t = t_1$. When S_2 is turned OFF, the snubber capacitors C_1 and C_2 starts discharging and charging respectively with the current i_{L1}. i_{L1} is distributed in these capacitors in proportion to their values. At the end of this interval, $v_{S1}(t_2)$=$V_{bus} - V_o/n$ and $v_{S2}(t_2)$=V_o/n. Mode-3 (t_2-t_3) [Fig. 2(b)(iii)] starts when v_{S2} increases from V_o/n to V_{bus}. Thus, the voltage across L_S is $v_{S2} - V_o/n$, making the current increase in it. Similarly, L_P has output voltage V_o across it, thus the current in it starts increasing. When the current i_{Ls} increases more than i'_{Lp}, the rectifier diodes, D_{R1} and D_{R4} start conducting. Mode-4 (t_3-t_4) [Fig. 2(b)(iv)] starts when the capacitors C_1 and C_2 completely discharged and charged respectively. The diode, D_1 starts conducting, thus the voltage across S_1 is zero, making S_1 to turn ON with ZVS when the gate signal is provided to it. The currents i_{Ls} and i_{Lp} increase with a slope of $(V_{bus} - V_o/n)/L_s$. Mode-5 (t_4-t_5) [Fig. 2(b)(v)] starts when $i_{S4}(t_4)$ reaches I_{in}. The switch S_1 is turned ON with ZVS. i_{Ls} increases above $I_{in}/2$. Both i_{Ls} and i_{Lp} increase with the same slope as previous. Mode-6 (t_5-t_6) [Fig. 2(b)(vi)] starts when the switch S_1 is turned OFF and the current $i_{S4}(t_5)$ reaches to the maximum value, $3I_{in}/2 + I'_{Lp,peak}$. The snubber capacitors, C_1 and C_2 start charging and discharging respectively. In Mode-7 (t_6-t_7) [Fig. 2(b)(vi)] C_1 and C_2 continue to charge and discharge respectively. Mode-8 (t_7-t_8) [Fig. 2(b)(vii)]) starts when C_1 charges to its initial voltage and C_2 completely discharges. The diode D_2 starts conducting, thus the voltage across S_2 is zero, making S_2 to turn ON with ZVS when the gate signal is provided to it. The current i_{Ls} starts decreasing with a negative slope of $V_o/(nL_S)$. At the end of this mode, $i_{Ls}(t_8) = I_{in}/2$. In mode-9 (t_8-t_9) [Fig. 2(b)(viii)], the switch S_2 turned ON with ZVS and



(a) (b) (c) (d)

Fig. 4. Simulation results at (a) 22 V and full load (b) 22 V and l0% load (c) 41 V and full load (d) 41 V and 10% load.

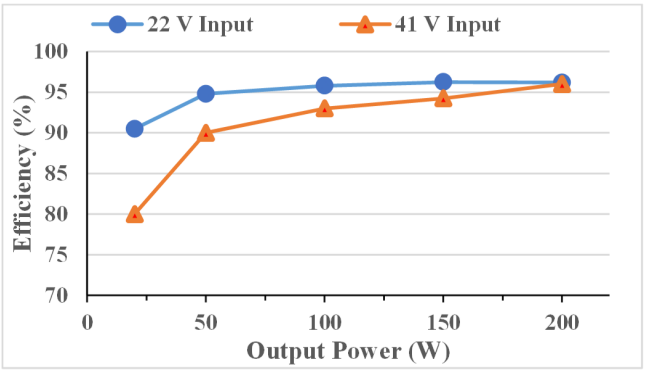


Fig. 5. Efficiency curve with load variation for input voltages of 22 V and 41 V

the current in it starts increasing. i_{Ls} starts decreasing and flows through S_2. This mode ends when $i_{Ls} = i_{Lp}$ and $i_{S2}(t_9) = I_{in}/2 - I'_{Lp,peak}$.

B. Design Procedure

The proposed converter components can be designed based on the minimum input voltage $V_{in,min}$, maximum switch voltage $V_{SW,max}$ and full-load conditions. The maximum duty cycle D_{max} is expressed as $D_{max} = 1-(V_{in,min}/V_{SW,max})$. Optimal values are chosen for L'_P/L_S and $n = N_S/N_P$ with respect to ZVS range and high efficiency where $L'_P = L_P/n^2$. Thus, the inductance value of L_S is given by

$$L_s = \frac{R_L}{f_s}\left[\frac{(V_{in,min}/V_o)^2}{(1+(L_S/L'_P))} - \frac{(V_{in,min}/V_o)(1-D_{max})}{n}\right] \quad (1)$$

The boost inductor values are expressed as $L_1 = L_2 = (V_{in,min}D_{max})/[\Delta I_{in} f_s]$ where ΔI_{in} is the inductor ripple current chosen.

III. Simulation Analysis

For simulation, V_{in} of 22 V & 41 V for a load of 200 W, 350 V and a switching frequency f_s of 100 kHz are considered. The parameters obtained based on the design procedure are: n = 4, $L_S = 4\ \mu H$, $L_P = 1.61\ mH$, $L_1 = L_2 = 352\ \mu H$, $C_{bus} = 1\ \mu F$, $C_o = 2\ \mu F$. Fig. 3 shows the voltage gain curve with respect to duty cycle control for full load and 10% load. The duty cycle is well within the limits of 0.551 to 0.799. The proposed configuration is simulated in PSIM software, with input voltages of 22 V and 41 V at 100% and 10% full-load conditions. The corresponding results are shown in Fig. 4. It can be observed that the peak current of i_{Lp} increases as the voltage increases, aiding for the ZVS turn ON. Thus, ZVS turn ON of S_1 to S_4 can be observed along with ZCS turn OFF of D_{R1} & D_{R3} in all the four cases. Also, it can be observed that the switch peak currents decrease as the input voltage increases.

IV. Efficiency Analysis and Comparative Study

The efficiency of the converter is estimated by using thermal analysis in PSim software. The efficiency at an input voltage of 41 V at full load and 10% load is 80% and 96% respectively. Similarly, the efficiency at an input voltage of 22 V at full load and 10% load is 90.5% and 96.2% respectively. Fig. 5 shows the efficiency curve with respect to load variation for the input voltages of 22 V and 41 V. It can be observed from the figure that the efficiency is high at lower, medium and high loads. But, for ultra-low loads, i.e., $< 10\%$ loads, the efficiency reduces due to the constant conduction losses. Hence, operating at these ultra lower loads is not encouraged and to handle the transients, ultra capacitors can be used.

Table I shows the comparison of proposed converter with existing wide gain soft switched converters with respect to component count, voltage gain, efficiency, etc. Compared with existing converters, the proposed converter has reduced number of switching devices. Thus, the gate driver circuits

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TABLE I
COMPARISON OF WIDE RANGE SOFT SWITCHED CONVERTERS

Structure	MOSFETs	Diodes	Inductors	Capacitors	Control	Output Rating	Input Voltage (V)	Switching Frequency	Efficiency (%)	Gain Range
Ref. [2]	8	4	1	4	PS	380 V/ 800 W	100-400	60 kHz	97.61	0.35-1.4
Ref. [3]	5	1	2	4	PWM	380 V/ 300 W	25-35	135 kHz	98.9	1.97-2.76
Ref. [4]	6	0	2	3	Double Pulse	380 V/ 300 W	25-35	140 kHz	98.61	1.73-2.43
Ref. [5]	7	3	1	4	PWM	200 V, 400 V/ 500 W	30-60	100 kHz	95.4	0.5-2
Proposed Converter	4	4	2	6	PWM	350 V/ 200 W	22-41	100 kHz	96.25 (Sim.)	8.53-15.9

required are less. Also, the input current ripple of the proposed converter is less as can be observed in the simulation results and the peak-peak input current, $i_{in,peak-peak} = 0.3746\ A$ is very less compared with $i_{in,peak-peak} = 10.99\ A$ in [7] for the worst condition. Thus, the proposed configuration has reduced switching devices, hence, less number of gate driver circuits, provides very less input current ripple, reduced switch peak currents at higher voltages, able to achieve ZVS turn ON across all the switches and ZCS turn OFF across rectifier diodes from full load to light load even with input voltage variations.

V. CONCLUSION

In this paper, a wide range soft switched interleaved boost integrated L-L type full-bridge isolated DC-DC converter is proposed. Fixed frequency duty cycle modulation is employed for voltage regulation. It provides wide ZVS across inverter switches and wide ZCS across rectifier diodes for input voltage and load power variations, reduced switch peak currents with the increased input voltage. Thus, overall efficiency is improved with reduced switch current stress. In addition, it provides a significant reduction in input current ripple which results in reduced input filter size, hence making it well suitable for PV and fuel cell applications.

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